

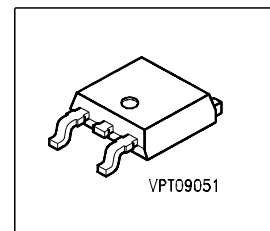
Smart Lowside Power Switch

Features

- Logic Level Input
- Input Protection (ESD)
- Thermal shutdown
- Overload protection
- Short circuit protection
- Overvoltage protection
- Current limitation
- Analog driving possible

Product Summary

Drain source voltage	V_{DS}	42	V
On-state resistance	$R_{DS(on)}$	50	m Ω
Nominal load current	$I_{D(Nom)}$	3.5	A
Clamping energy	E_{AS}	3	J

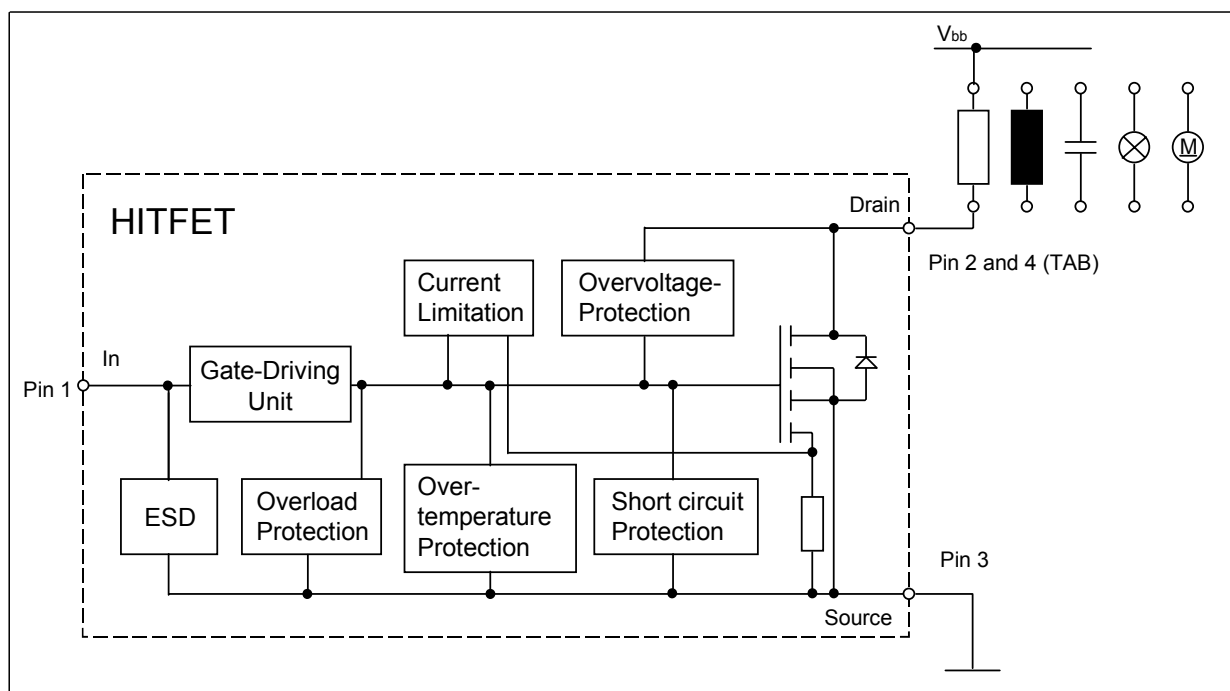


Application

- All kinds of resistive, inductive and capacitive loads in switching or linear applications
- μ C compatible power switch for 12 V DC applications
- Replaces electromechanical relays and discrete circuits

General Description

N channel vertical power FET in Smart SIPMOS® technology. Fully protected by embedded protection functions.



Maximum Ratings at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	42	V
Drain source voltage for short circuit protection $T_j = -40\dots 150^\circ\text{C}$	$V_{DS(SC)}$	30	
Continuous input current $-0.2\text{V} \leq V_{IN} \leq 10\text{V}$ $V_{IN} < -0.2\text{V}$ or $V_{IN} > 10\text{V}$	I_{IN}	no limit $ I_{IN} \leq 2$	mA
Operating temperature	T_j	-40 ... +150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 ... +150	
Power dissipation $T_C = 85^\circ\text{C}$ 6cm ² cooling area , $T_A = 85^\circ\text{C}$	P_{tot}	43 1.1	W
Unclamped single pulse inductive energy ¹⁾	E_{AS}	3	J
Load dump protection $V_{LoadDump}^{2)} = V_A + V_S$ $V_{IN} = 0$ and 10V , $t_d = 400\text{ms}$, $R_I = 2\ \Omega$, $R_L = 4.5\ \Omega$, $V_A = 13.5\text{V}$	V_{LD}	65	V
Electrostatic discharge voltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993	V_{ESD}	2	kV
DIN humidity category, DIN 40 040		E	
IEC climatic category; DIN IEC 68-1		40/150/56	

Thermal resistance

junction - case:	R_{thJC}	1.5	K/W
SMD: junction - ambient @ min. footprint	R_{thJA}	115	
@ 6 cm ² cooling area ³⁾		55	

¹ Not tested, specified by design.

² $V_{LoadDump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

³ Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB mounted vertical without blown air.

Electrical Characteristics

Parameter at $T_j = 25^\circ\text{C}$, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Drain source clamp voltage $T_j = -40 \dots +150$, $I_D = 10 \text{ mA}$	$V_{DS(AZ)}$	42	-	55	V
Off-state drain current $T_j = -40 \dots +150^\circ\text{C}$ $V_{DS} = 32 \text{ V}$, $V_{IN} = 0 \text{ V}$	I_{DSS}	-	1.5	10	μA
Input threshold voltage $I_D = 1.4 \text{ mA}$, $T_j = 25^\circ\text{C}$ $I_D = 1.4 \text{ mA}$, $T_j = 150^\circ\text{C}$	$V_{IN(th)}$	1.3 0.8	1.7 -	2.2 -	V
On state input current	$I_{IN(on)}$	-	10	30	μA
On-state resistance $V_{IN} = 5 \text{ V}$, $I_D = 3 \text{ A}$, $T_j = 25^\circ\text{C}$ $V_{IN} = 5 \text{ V}$, $I_D = 3 \text{ A}$, $T_j = 150^\circ\text{C}$	$R_{DS(on)}$	- -	45 75	60 100	$\text{m}\Omega$
On-state resistance $V_{IN} = 10 \text{ V}$, $I_D = 3 \text{ A}$, $T_j = 25^\circ\text{C}$ $V_{IN} = 10 \text{ V}$, $I_D = 3 \text{ A}$, $T_j = 150^\circ\text{C}$	$R_{DS(on)}$	- -	35 65	50 90	
Nominal load current $T_j < 150^\circ\text{C}$, $V_{IN} = 10 \text{ V}$, $T_A = 85^\circ\text{C}$, SMD 1)	$I_{D(Nom)}$	3.5	-	-	A
Nominal load current $V_{IN} = 10 \text{ V}$, $V_{DS} = 0.5 \text{ V}$, $T_C = 85^\circ\text{C}$, $T_j < 150^\circ\text{C}$	$I_{D(ISO)}$	7.1	-	-	
Current limit (active if $V_{DS} > 2.5 \text{ V}$) ²⁾ $V_{IN} = 10 \text{ V}$, $V_{DS} = 12 \text{ V}$, $t_m = 200 \mu\text{s}$	$I_{D(lim)}$	18	24	30	

 1@ 6 cm² cooling area

 2Device switched on into existing short circuit (see diagram Determination of $I_{D(lim)}$). If the device is in on condition and a short circuit occurs, these values might be exceeded for max. 50 μs .

Electrical Characteristics

Parameter at $T_j = 25^\circ\text{C}$, unless otherwise specified	Symbol	Values			Unit
		min.	typ.	max.	

Dynamic Characteristics

Turn-on time V_{IN} to 90% I_D : $R_L = 4.7 \Omega$, $V_{IN} = 0$ to 10 V, $V_{bb} = 12$ V	t_{on}	-	60	100	μs
Turn-off time V_{IN} to 10% I_D : $R_L = 4.7 \Omega$, $V_{IN} = 10$ to 0 V, $V_{bb} = 12$ V	t_{off}	-	60	100	μs
Slew rate on 70 to 50% V_{bb} : $R_L = 4.7 \Omega$, $V_{IN} = 0$ to 10 V, $V_{bb} = 12$ V	$-dV_{DS}/dt_{on}$	-	0.3	1.5	V/ μs
Slew rate off 50 to 70% V_{bb} : $R_L = 4.7 \Omega$, $V_{IN} = 10$ to 0 V, $V_{bb} = 12$ V	dV_{DS}/dt_{off}	-	0.7	1.5	V/ μs

Protection Functions¹⁾

Thermal overload trip temperature	T_{jt}	150	175	-	$^\circ\text{C}$
Input current protection mode	$I_{IN(Prot)}$	80	160	300	μA
Input current protection mode $T_j = 150^\circ\text{C}$	$I_{IN(Prot)}$	-	130	300	μA
Unclamped single pulse inductive energy ²⁾ $I_D = 3$ A, $T_j = 25^\circ\text{C}$, $V_{bb} = 12$ V	E_{AS}	3	-	-	J

Inverse Diode

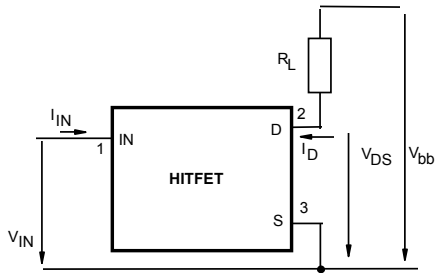
Inverse diode forward voltage $I_F = 15$ A, $t_m = 250 \mu\text{s}$, $V_{IN} = 0$ V, $t_P = 300 \mu\text{s}$	V_{SD}	-	1.0	-	V
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¹⁾ Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

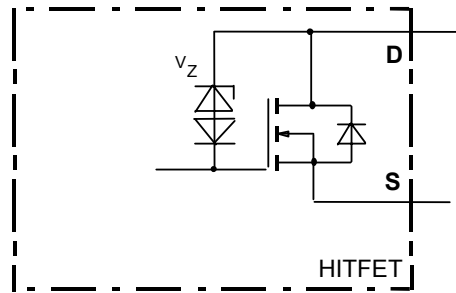
²⁾ Not tested, specified by design.

Block diagram

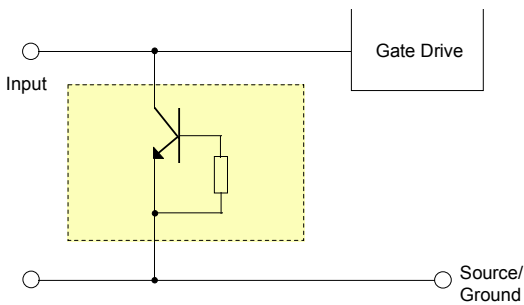
Terms



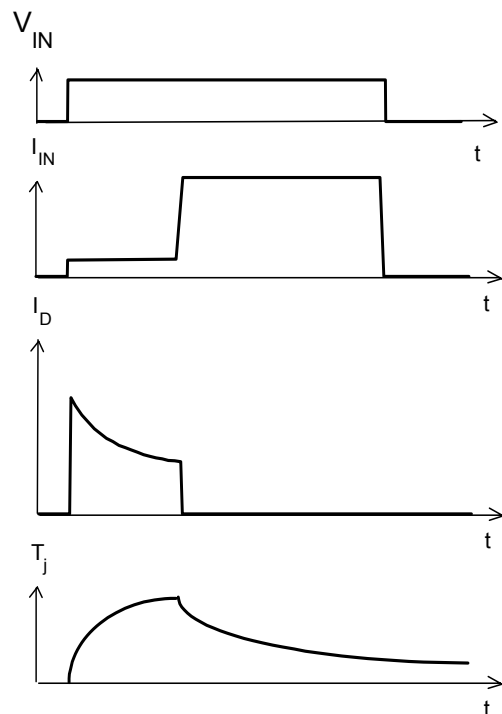
Inductive and overvoltage output clamp



Input circuit (ESD protection)



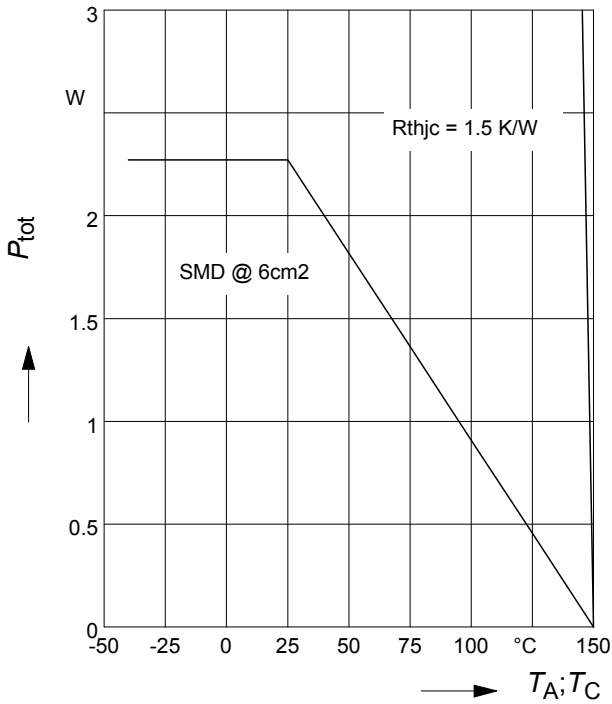
Short circuit behaviour



1 Maximum allowable power dissipation

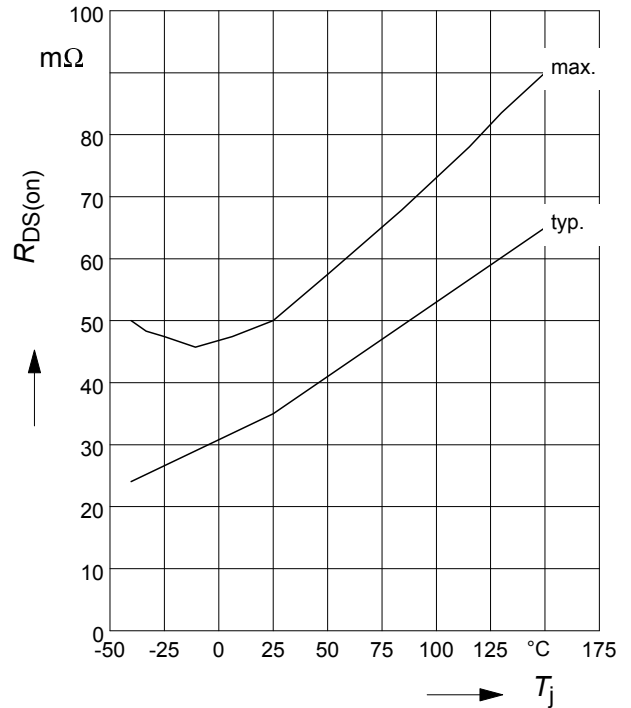
$P_{tot} = f(T_C)$ resp.

$P_{tot} = f(T_A) @ R_{thJA}=55 \text{ K/W}$



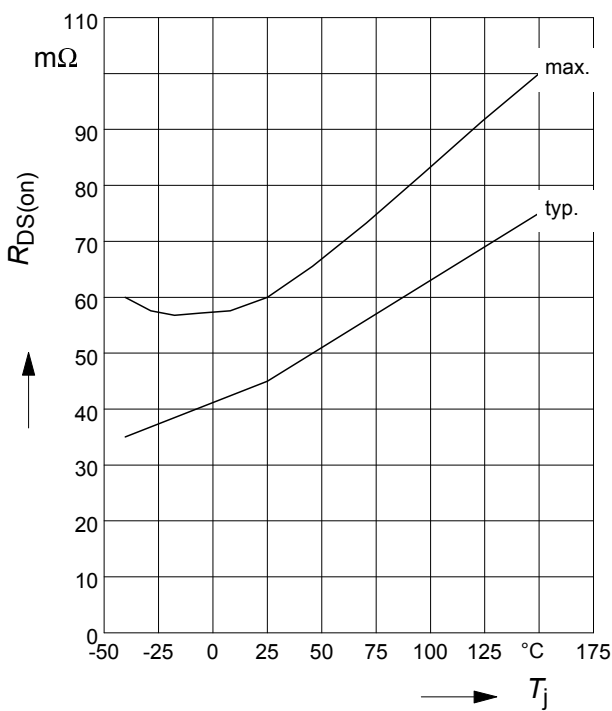
2 On-state resistance

$R_{ON}=f(T_j); I_D=3A; V_{IN}=10V$



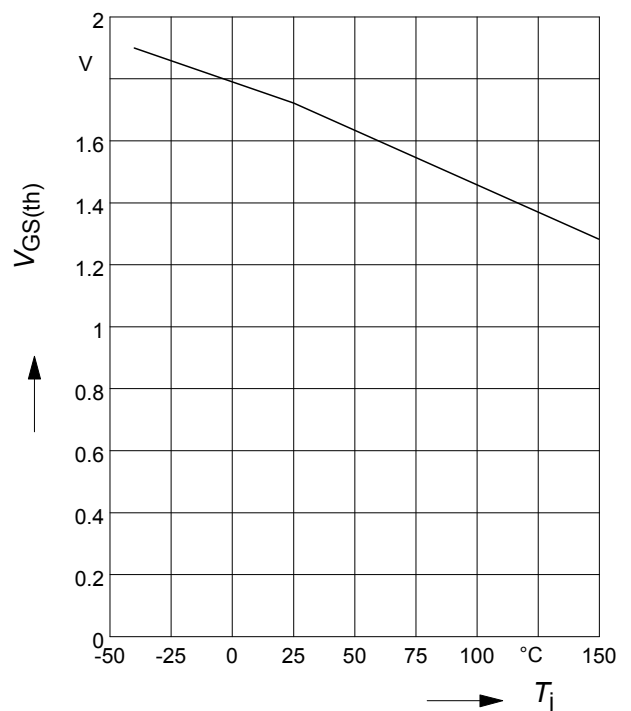
3 On-state resistance

$R_{ON}=f(T_j); I_D=3A; V_{IN}=5V$



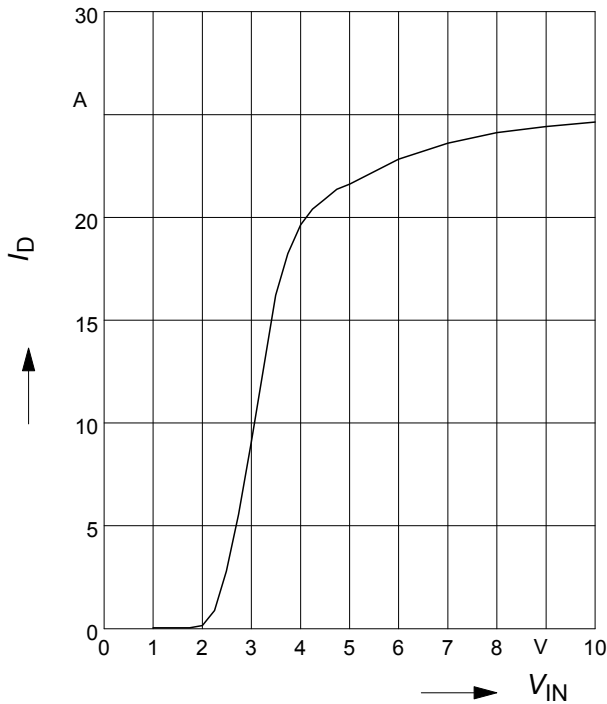
4 Typ. input threshold voltage

$V_{IN(th)} = f(T_j); I_D = 0.7 \text{ mA}; V_{DS} = 12V$



5 Typ. transfer characteristics

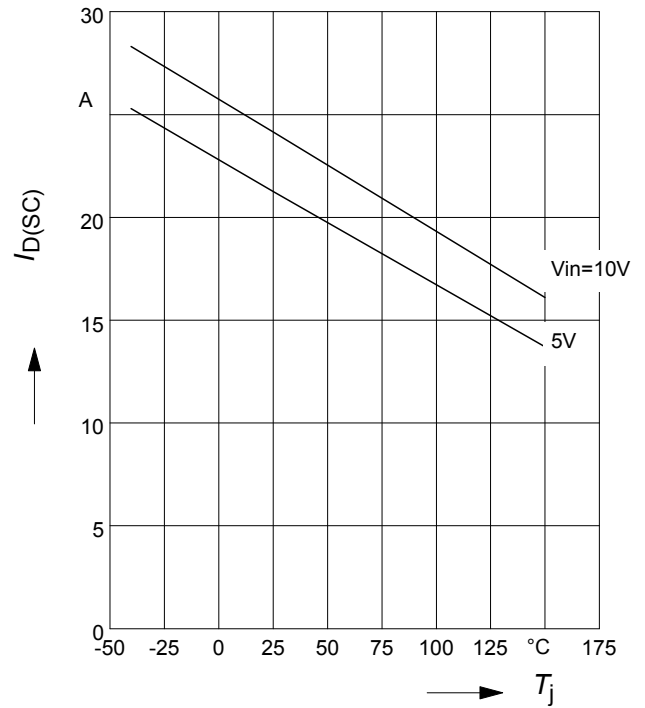
$I_D = f(V_{IN}); V_{DS} = 12V; T_{Jstart} = 25^\circ C$



6 Typ. short circuit current

$I_{D(lim)} = f(T_j); V_{DS} = 12V$

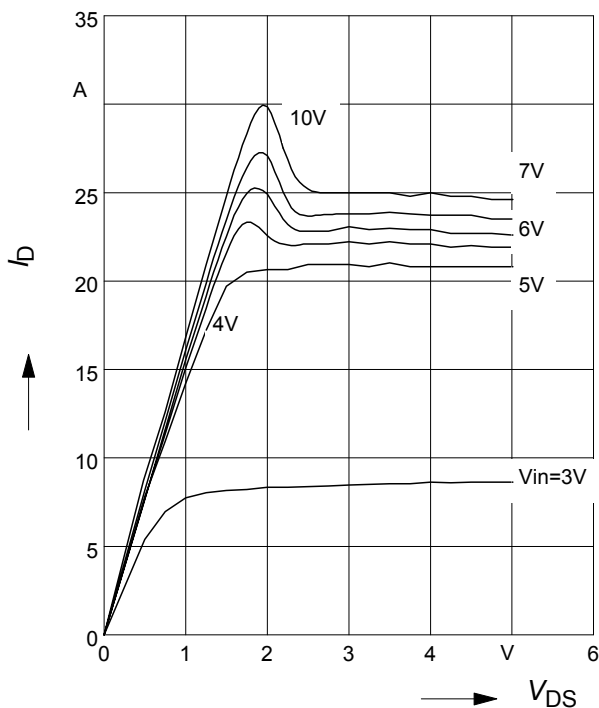
Parameter: V_{IN}



7 Typ. output characteristics

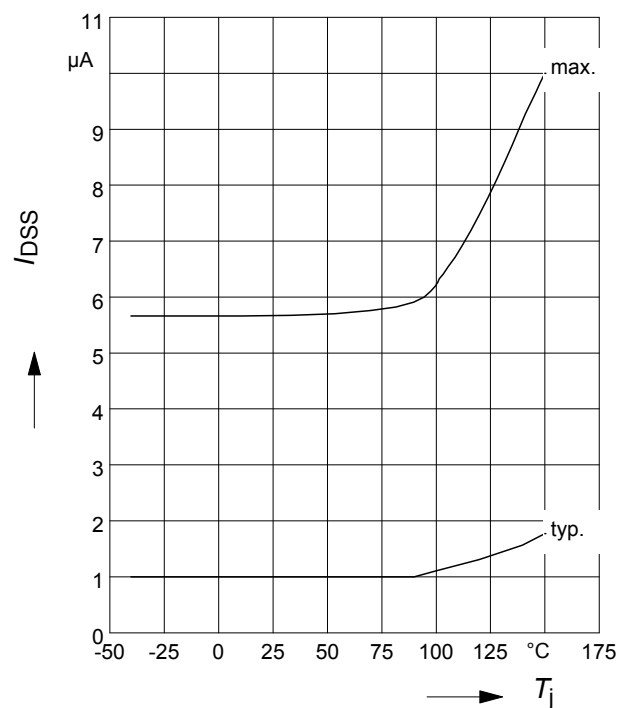
$I_D = f(V_{DS}); T_{Jstart} = 25^\circ C$

Parameter: V_{IN}



8 Typ. off-state drain current

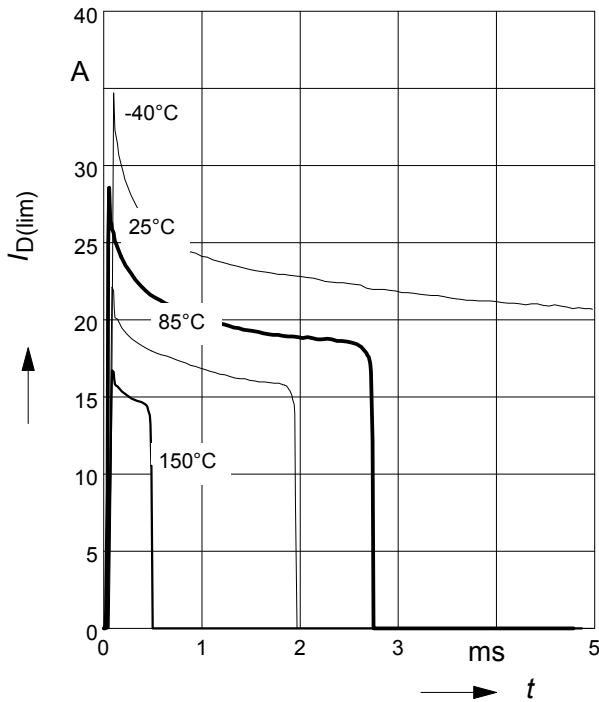
$I_{DSS} = f(T_j)$



9 Typ. overload current

$I_{D(lim)} = f(t)$, $V_{bb}=12\text{ V}$, no heatsink

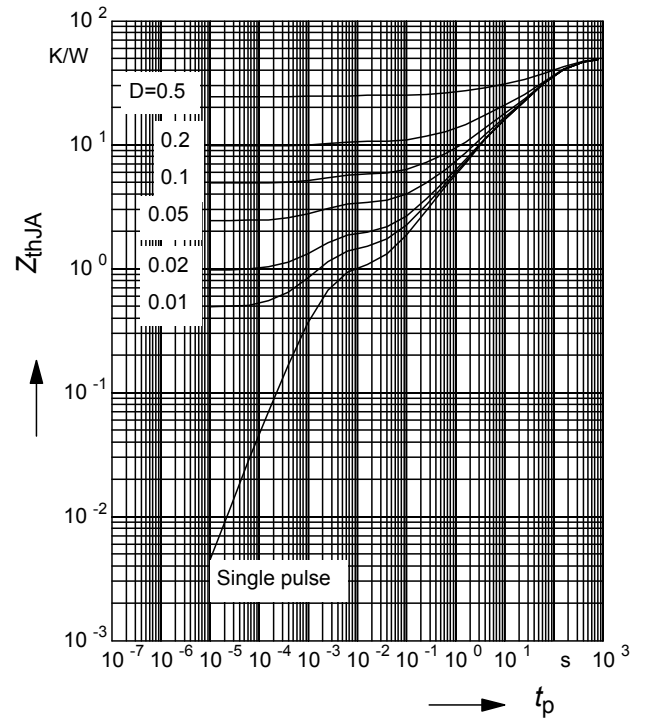
Parameter: T_{jstart}



10 Typ. transient thermal impedance

$Z_{thJA}=f(t_p)$ @ 6 cm² cooling area

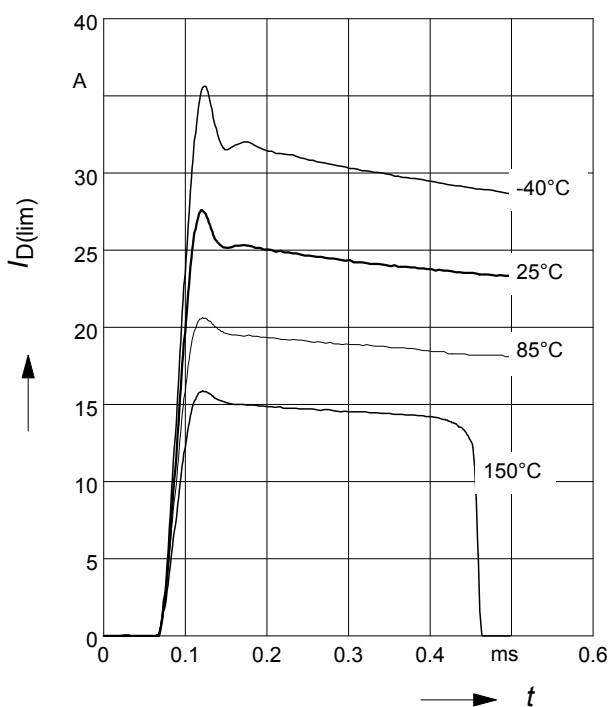
Parameter: $D=t_p/T$

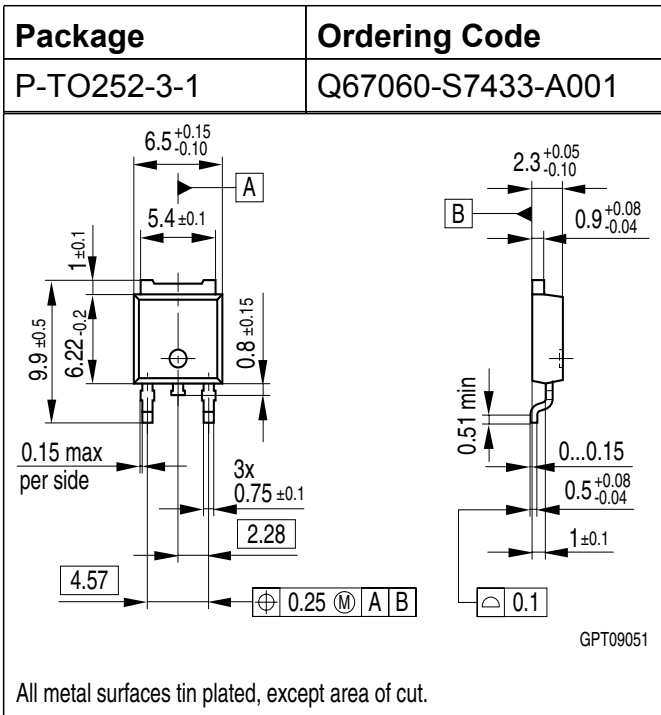


11 Determination of $I_{D(lim)}$

$I_{D(lim)} = f(t)$; $t_m = 200\mu\text{s}$

Parameter: T_{jstart}





Revision History : 2004-02-02
Previous version : 2002-09-04

Page	Subjects (major changes since last revision)
3	$V_{IN(th)}$ test conditions from $I_D=0.7mA$ to $I_D=1.4mA$

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