

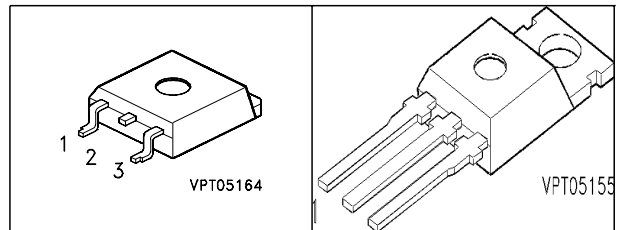
## OptiMOS™ Power-Transistor

### Features

- N-Channel
- Enhancement mode
- Avalanche rated
- $dv/dt$  rated
- 175°C operating temperature

### Product Summary

Drain source voltage	$V_{DS}$	55	V
Drain-source on-state resistance	$R_{DS(on)}$	5.1	mΩ
Continuous drain current	$I_D$	80	A



Type	Package	Ordering Code
SPP80N06S2-05	P-TO220-3-1	Q67040-S4245
SPB80N06S2-05	P-TO263-3-2	Q67040-S4255

Pin 1	PIN 2/4	PIN 3
G	D	S

### Maximum Ratings, at $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current $T_C = 25\text{ °C}$ , <sup>1)</sup> $T_C = 100\text{ °C}$	$I_D$	80 80	A
Pulsed drain current $T_C = 25\text{ °C}$	$I_{D\text{ puls}}$	320	
Avalanche energy, single pulse $I_D = 80\text{ A}$ , $V_{DD} = 25\text{ V}$ , $R_{GS} = 25\text{ Ω}$	$E_{AS}$	810	mJ
Reverse diode $dv/dt$ $I_S = 80\text{ A}$ , $V_{DS} = 44\text{ V}$ , $di/dt = 200\text{ A}/\mu\text{s}$ , $T_{j\text{max}} = 175\text{ °C}$	$dv/dt$	6	kV/ $\mu\text{s}$
Gate source voltage	$V_{GS}$	$\pm 20$	V
Power dissipation $T_C = 25\text{ °C}$	$P_{\text{tot}}$	300	W
Operating and storage temperature	$T_j, T_{\text{stg}}$	-55...+175	°C
IEC climatic category; DIN IEC 68-1		55/175/56	

<sup>1</sup>current limited by bondwire; with an  $R_{thJC} = 0.5\text{ K/W}$  the chip is able to carry  $I_D = 165\text{ A}$ .

**Thermal Characteristics**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Characteristics</b>					
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.5	K/W
Thermal resistance, junction - ambient, leaded	$R_{thJA}$	-	-	62	
SMD version, device on PCB: @ min. footprint @ 6 cm <sup>2</sup> cooling area <sup>1)</sup>	$R_{thJA}$	-	-	62 40	

**Electrical Characteristics**, at  $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Static Characteristics</b>					
Drain-source breakdown voltage $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	$V_{(BR)DSS}$	55	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D = 250\text{ }\mu\text{A}$	$V_{GS(th)}$	2.1	3	4	
Zero gate voltage drain current $V_{DS} = 55\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 25\text{ °C}$ $V_{DS} = 55\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 125\text{ °C}$	$I_{DSS}$	-	0.01 1	1 100	$\mu\text{A}$
Gate-source leakage current $V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$	$I_{GSS}$	-	1	100	
Drain-source on-state resistance $V_{GS} = 10\text{ V}$ , $I_D = 40\text{ A}$	$R_{DS(on)}$	-	3.8	5.1	$\text{m}\Omega$

<sup>1)</sup>Device on 40mm\*40mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics, at  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Dynamic Characteristics

Transconductance	$g_{fs}$	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$ , $I_D = 80\text{A}$	66	132	-	S
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$	-	5080	6350	pF
Output capacitance	$C_{oss}$		-	1290	1600	
Reverse transfer capacitance	$C_{rss}$		-	300	400	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{V}$ , $V_{GS} = 10\text{V}$ , $I_D = 80\text{A}$ , $R_G = 2.2\Omega$	-	18	27	ns
Rise time	$t_r$		-	126	190	
Turn-off delay time	$t_{d(off)}$		-	54	80	
Fall time	$t_f$		-	20	30	

### Gate Charge Characteristics

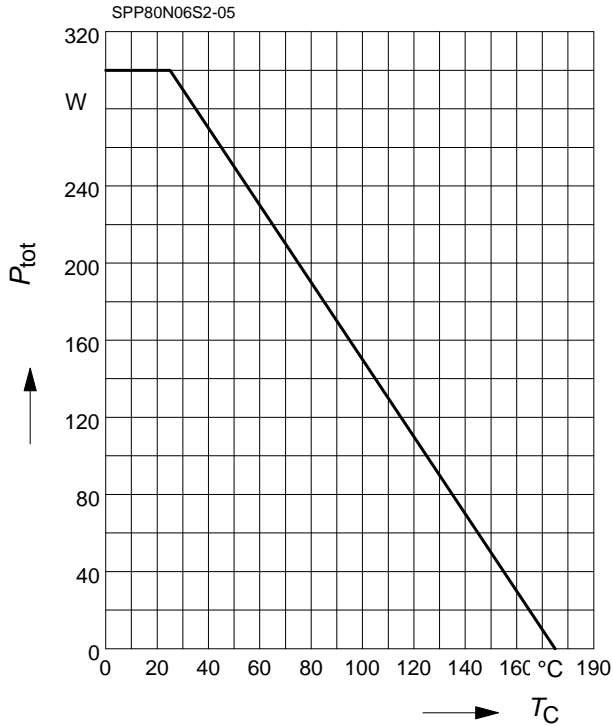
Gate to source charge	$Q_{gs}$	$V_{DD} = 44\text{V}$ , $I_D = 80\text{A}$	-	25	30	nC
Gate to drain charge	$Q_{gd}$		-	47	60	
Gate charge total	$Q_g$	$V_{DD} = 44\text{V}$ , $I_D = 80\text{A}$ , $V_{GS} = 0$ to $10\text{V}$	--	120	150	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 44\text{V}$ , $I_D = 80\text{A}$	--	5.2	--	V

### Reverse Diode

Inverse diode continuous forward current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	80	A
Inverse diode direct current, pulsed	$I_{SM}$		-	-	320	
Inverse diode forward voltage	$V_{SD}$	$V_{GS} = 0\text{V}$ , $I_F = 80\text{A}$	-	0.9	1.3	V
Reverse recovery time	$t_{rr}$	$V_R = 30\text{V}$ , $I_F = I_S$ , $di_F/dt = 100\text{A}/\mu\text{s}$	-	tbd	tbd	ns
Reverse recovery charge	$Q_{rr}$		-	tbd	tbd	nC

**Power dissipation**

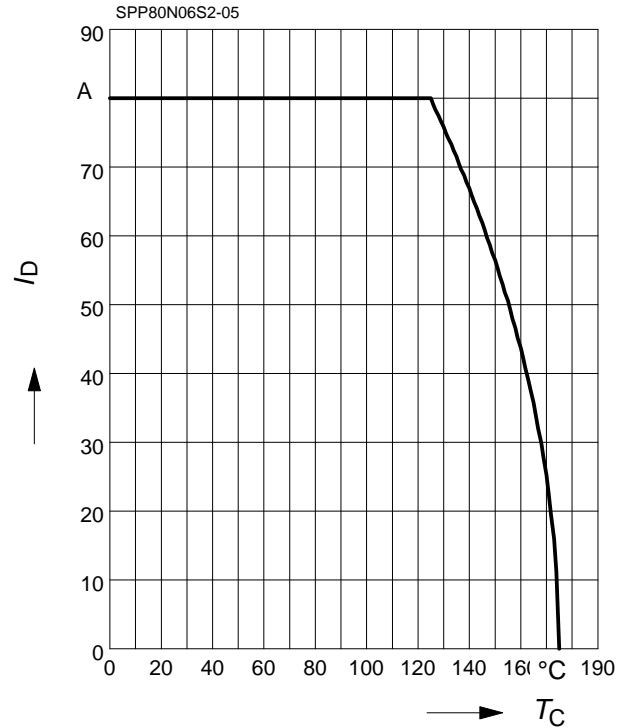
$$P_{tot} = f(T_C)$$



**Drain current**

$$I_D = f(T_C)$$

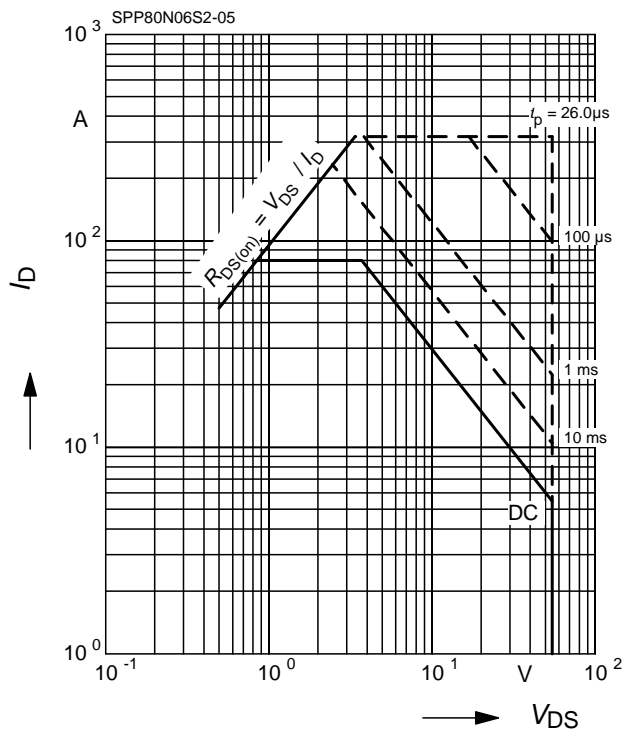
parameter:  $V_{GS} \geq 10 \text{ V}$



**Safe operating area**

$$I_D = f(V_{DS})$$

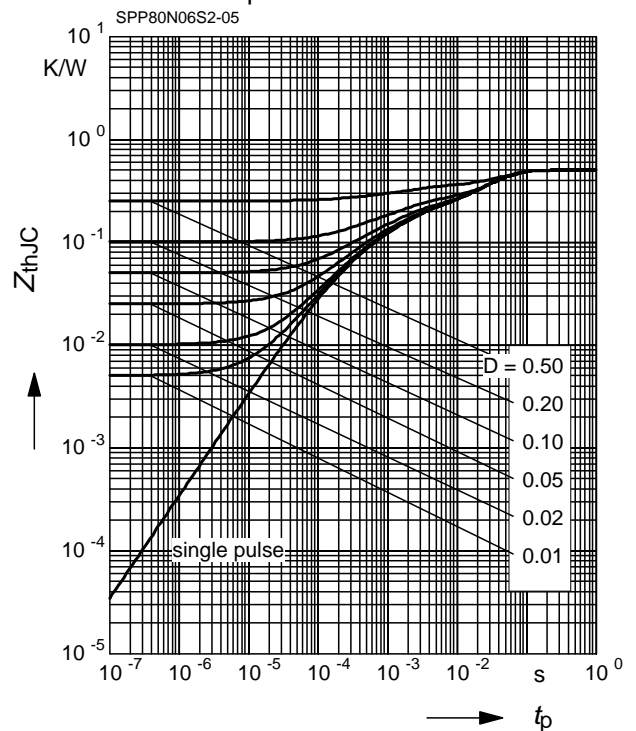
parameter:  $D = 0, T_C = 25 \text{ °C}$



**Transient thermal impedance**

$$Z_{thJC} = f(t_p)$$

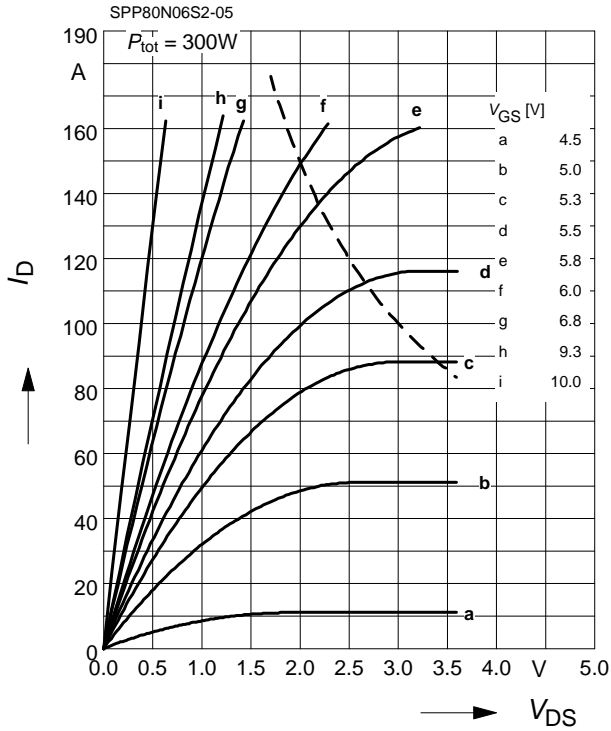
parameter:  $D = t_p/T$



**Typ. output characteristic**

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

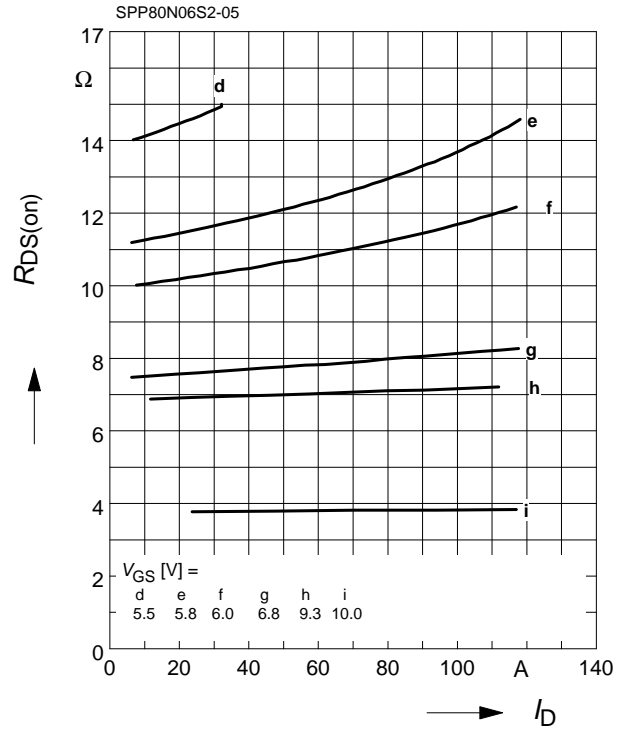
parameter:  $t_p = 80 \mu\text{s}$



**Typ. drain-source-on-resistance**

$R_{DS(on)} = f(I_D)$

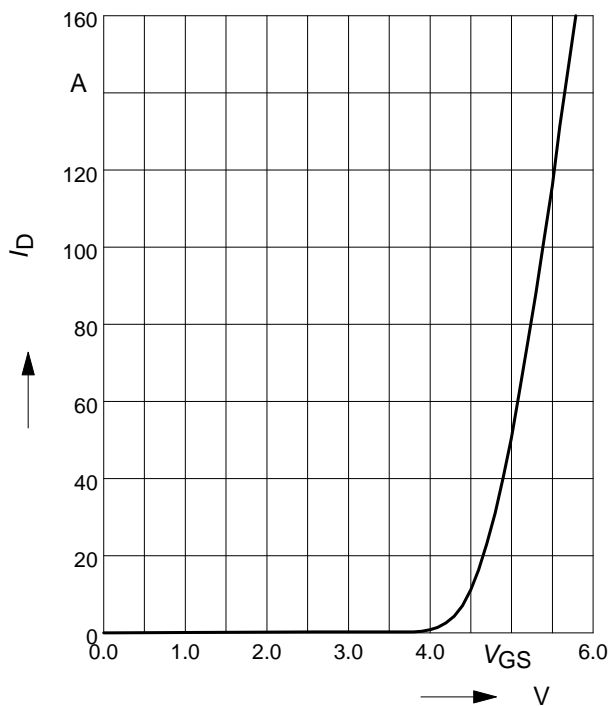
parameter:  $V_{GS}$



**Typ. transfer characteristics  $I_D = f(V_{GS})$**

$V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$

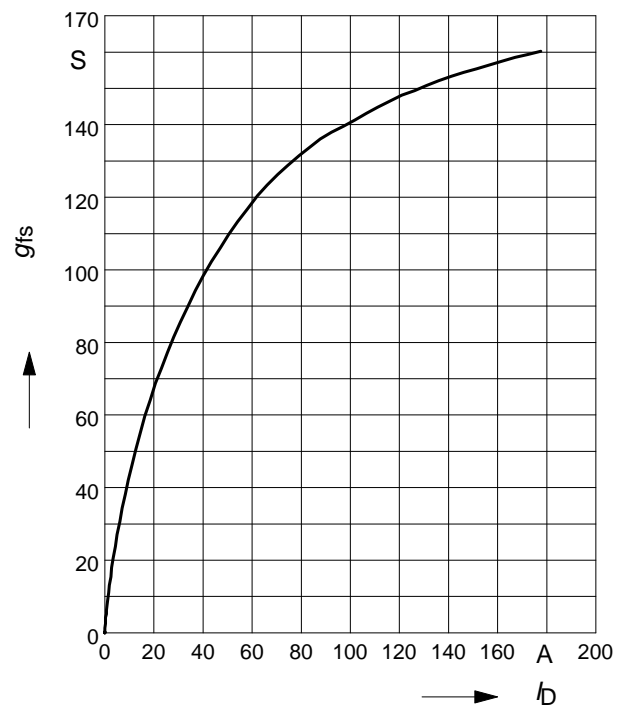
parameter:  $t_p = 80 \mu\text{s}$



**Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

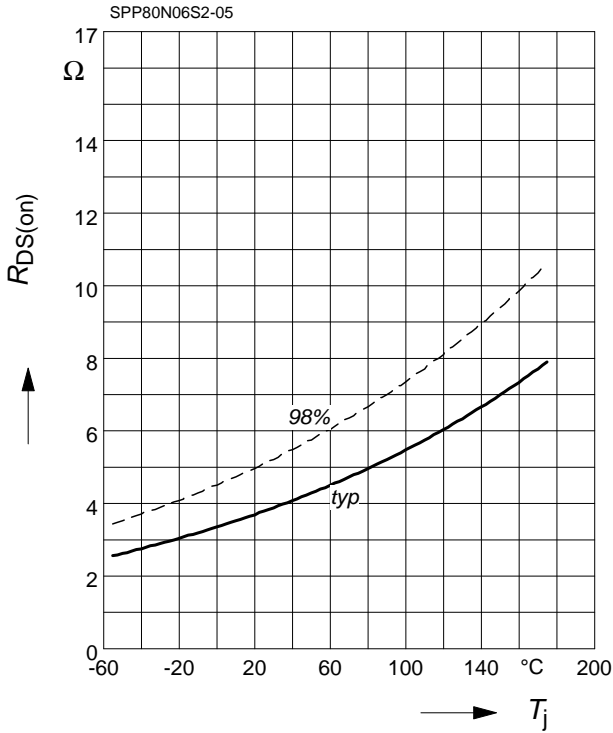
parameter:  $g_{fs}$



**Drain-source on-state resistance**

$$R_{DS(on)} = f(T_j)$$

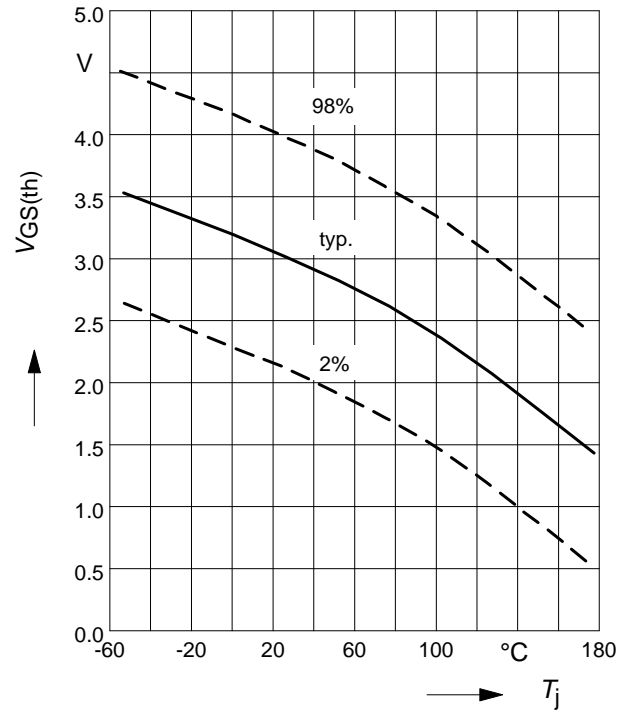
parameter :  $I_D = 40 \text{ A}$ ,  $V_{GS} = 10 \text{ V}$



**Gate threshold voltage**

$$V_{GS(th)} = f(T_j)$$

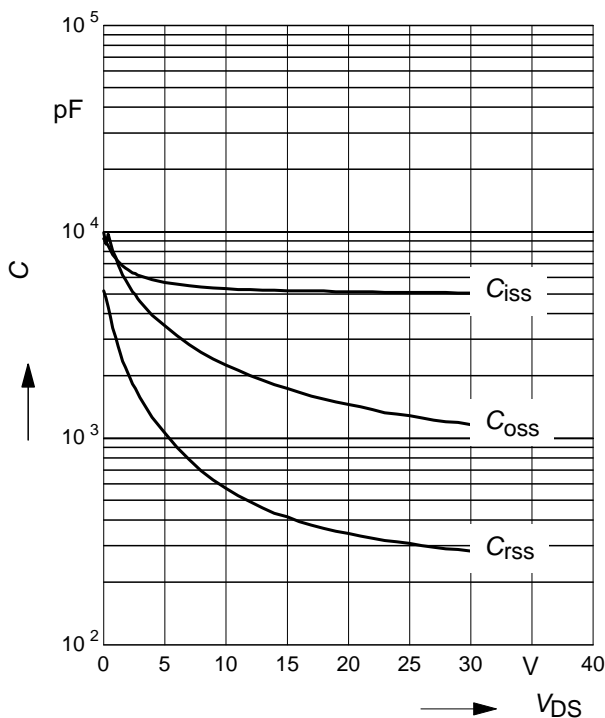
parameter:  $V_{GS} = V_{DS}$ ,  $I_D = 250 \mu\text{A}$



**Typ. capacitances**

$$C = f(V_{DS})$$

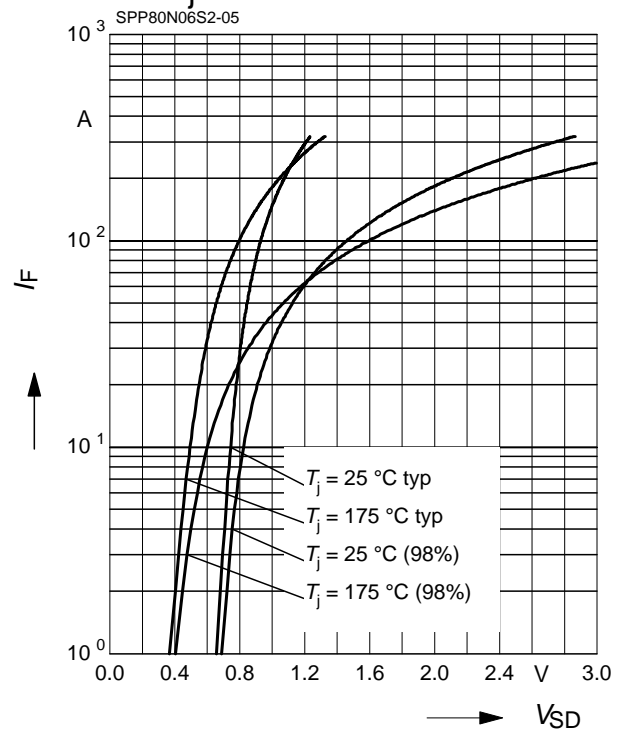
parameter:  $V_{GS}=0\text{V}$ ,  $f=1 \text{ MHz}$



**Forward characteristics of reverse diode**

$$I_F = f(V_{SD})$$

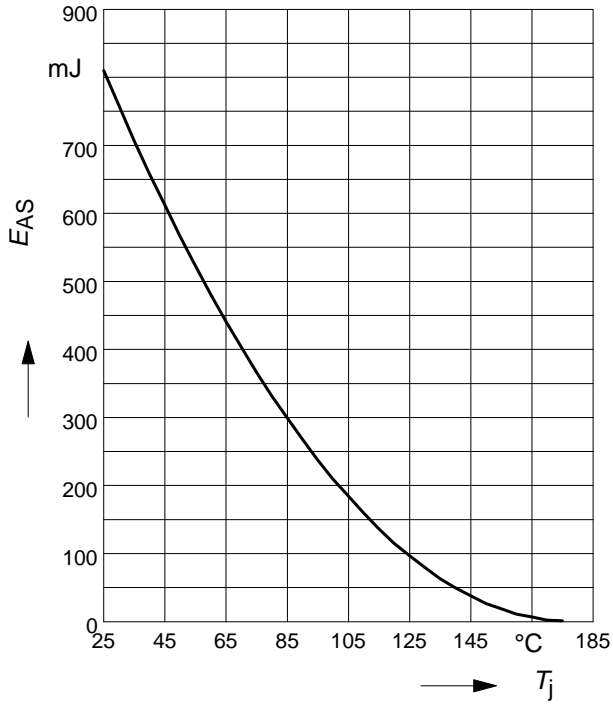
parameter:  $T_j$ ,  $t_p = 80 \mu\text{s}$



**Avalanche energy**

$$E_{AS} = f(T_j)$$

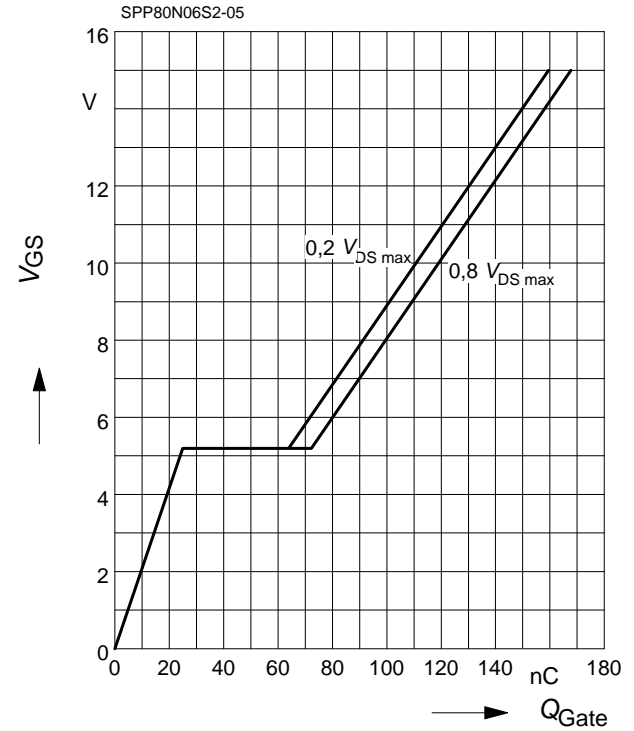
par.:  $I_D = 80\text{ A}$  ,  $V_{DD} = 25\text{ V}$  ,  $R_{GS} = 25\ \Omega$



**Typ. gate charge**

$$V_{GS} = f(Q_{Gate})$$

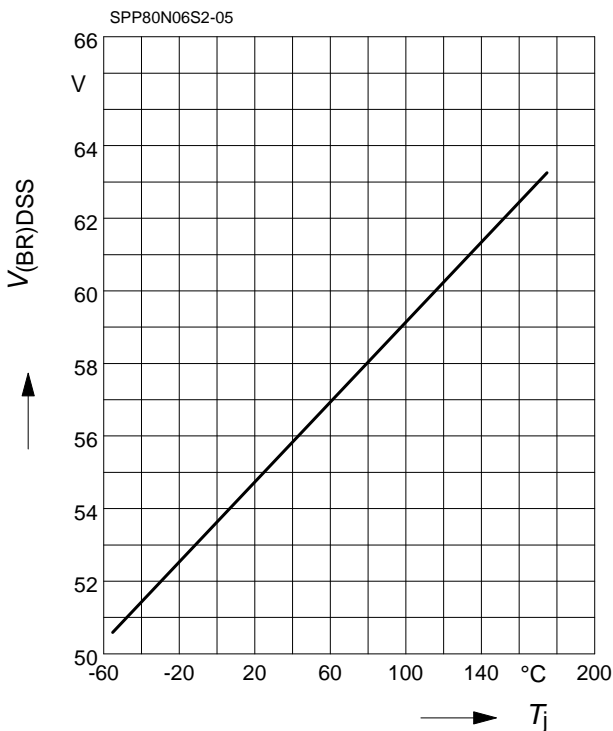
parameter:  $I_D = 80\text{ A}$  pulsed



**Drain-source breakdown voltage**

$$V_{(BR)DSS} = f(T_j)$$

parameter:  $I_D = 10\text{ mA}$



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