



74LVX373

LOW VOLTAGE CMOS OCTAL D-TYPE LATCH (3-STATE NON INV.) WITH 5V TOLERANT INPUTS

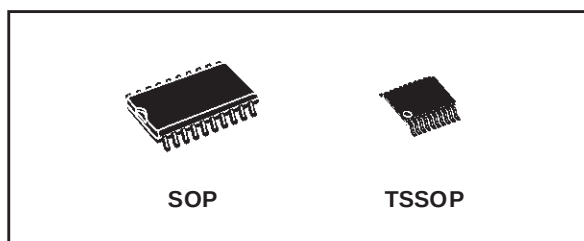
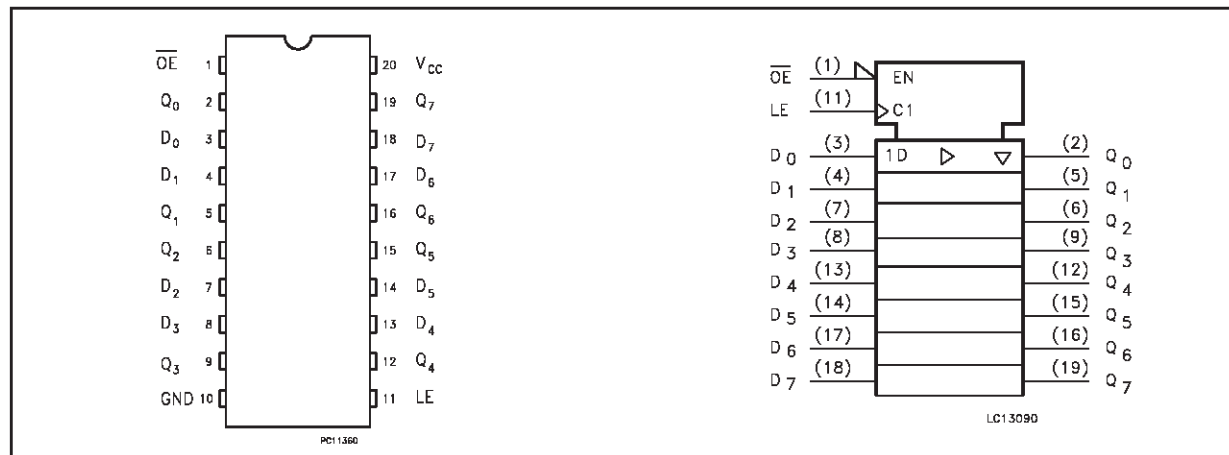
- HIGH SPEED:
 $t_{PD}=5.8ns$ (TYP.) at $V_{CC} = 3.3V$
- 5V TOLERANT INPUTS
- POWER-DOWN PROTECTION ON INPUTS
- INPUT VOLTAGE LEVEL:
 $V_{IL} = 0.8V$, $V_{IH} = 2V$ at $V_{CC} = 3V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A=25^\circ C$
- LOW NOISE:
 $V_{OLP} = 0.3V$ (TYP.) at $V_{CC} = 3.3V$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4 mA$ (MIN) at $V_{CC} = 3V$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(OPR) = 2V$ to $3.6V$ (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 373
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74LVX373 is a low voltage CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications.

This 8 bit D-Type latch is controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$). While the LE input is held at a high level, the Q outputs will follow the data input precisely.

PIN CONNECTION AND IEC LOGIC SYMBOLS



ORDER CODES

PACKAGE	TUBE	T & R
SOP	74LVX373M	74LVX373MTR
TSSOP		74LVX373TTR

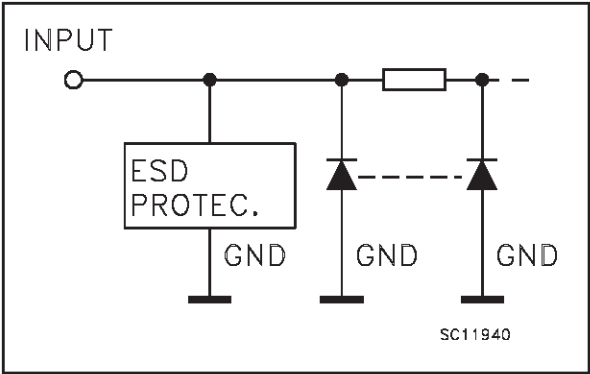
When the LE is taken low, the Q outputs will be latched precisely at the logic level of D input data. While the ($\overline{OE}$) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage.

This device can be used to interface 5V to 3V. It combines high speed performance with the true CMOS low power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

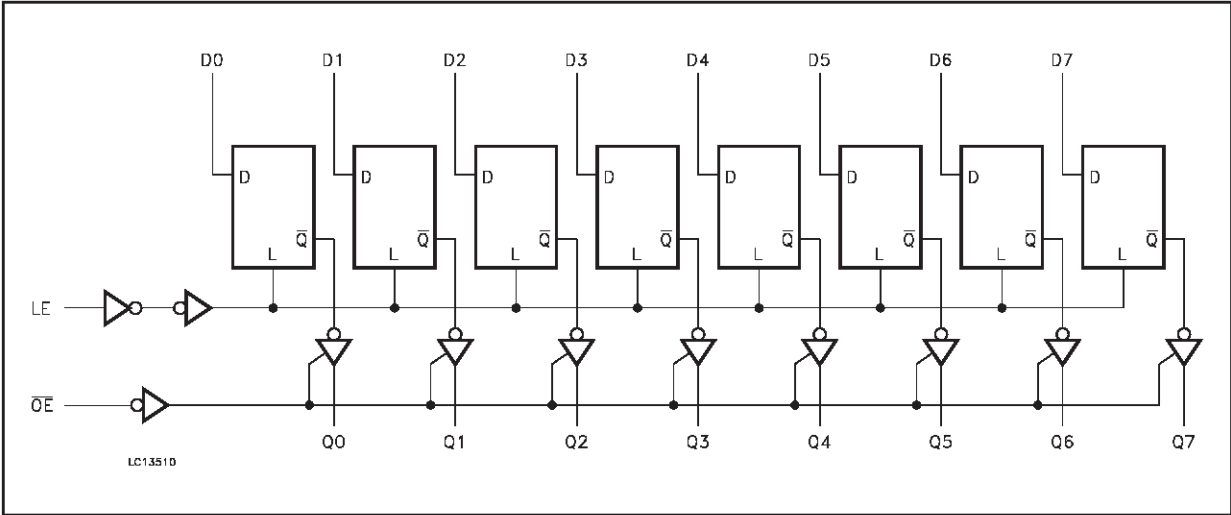
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
2, 5, 6, 9, 12, 15, 16,19	Q0 to Q7	3-State Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE*
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
* : Q Outputs are Latched at the time when the LE INPUT is taken low logic level

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2) ($V_{CC} = 3V$)	0 to 100	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0		2.0			2.0		2.0		
		3.6		2.4			2.4		2.4		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0				0.8		0.8		0.8	
		3.6				0.8		0.8		0.8	
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9		
		3.0	I _O =-4 mA	2.58			2.48		2.4		
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1	
		3.0	I _O =4 mA			0.36		0.44		0.55	
I _{OZ}	High Impedance Output Leakage Current	3.6	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.25		± 2.5		± 5	μA
I _I	Input Leakage Current	3.6	V _I = 5V or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	3.6	V _I = V _{CC} or GND			4		40		40	μA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C _L = 50 pF		0.3	0.8					V
V _{OLV}				-0.8	-0.3						
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2.0							
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition			Value							Unit
		V _{CC} (V)	C _L (pF)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time LE to Q	2.7	15			7.5	14.5	1.0	17.5	1.0	18.5	ns
		2.7	50			10.0	18.0	1.0	21.0	1.0	22.0	
		3.3 ^(*)	15			6.8	10.3	1.0	12.0	1.0	13.0	
		3.3 ^(*)	50			9.3	13.8	1.0	15.5	1.0	16.5	
t _{PLH} t _{PHL}	Propagation Delay Time D to Q	2.7	15			7.7	15.0	1.0	18.5	1.0	19.5	ns
		2.7	50			10.2	18.5	1.0	22.0	1.0	23.0	
		3.3 ^(*)	15			5.8	9.7	1.0	11.5	1.0	12.5	
		3.3 ^(*)	50			8.5	13.2	1.0	15.0	1.0	16.0	
t _{PZL} t _{PZH}	Output Enable Time	2.7	15			7.7	15.0	1.0	18.5	1.0	19.5	ns
		2.7	50			10.2	18.5	1.0	22.0	1.0	23.0	
		3.3 ^(*)	15			6.0	9.7	1.0	11.5	1.0	12.5	
		3.3 ^(*)	50			8.5	13.2	1.0	15.0	1.0	16.0	
t _{PLZ} t _{PHZ}	Output Disable Time	2.7	50			9.8	18.0	1.0	21.0	1.0	22.0	ns
		3.3 ^(*)	50			8.2	12.8	1.0	14.5	1.0	15.5	
t _W	LE pulse Width, HIGH	2.7	50				6.5		7.5		7.5	ns
		3.3 ^(*)	50				5.0		5.0		5.0	
t _S	Setup Time D to LE HIGH or LOW	2.7	50				6.0		6.0		6.0	ns
		3.3 ^(*)	50				4.0		4.0		4.0	
t _h	Hold Time D to LE HIGH or LOW	2.7	50				1.0		1.0		1.0	ns
		3.3 ^(*)	50				1.0		1.0		1.0	
t _{OSLH} t _{OSHL}	Output to Output Skew Time (note 1,2)	2.7	50			0.5	1.0		1.5		1.5	ns
		3.3 ^(*)	50			0.5	1.0		1.5		1.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

2) Parameter guaranteed by design

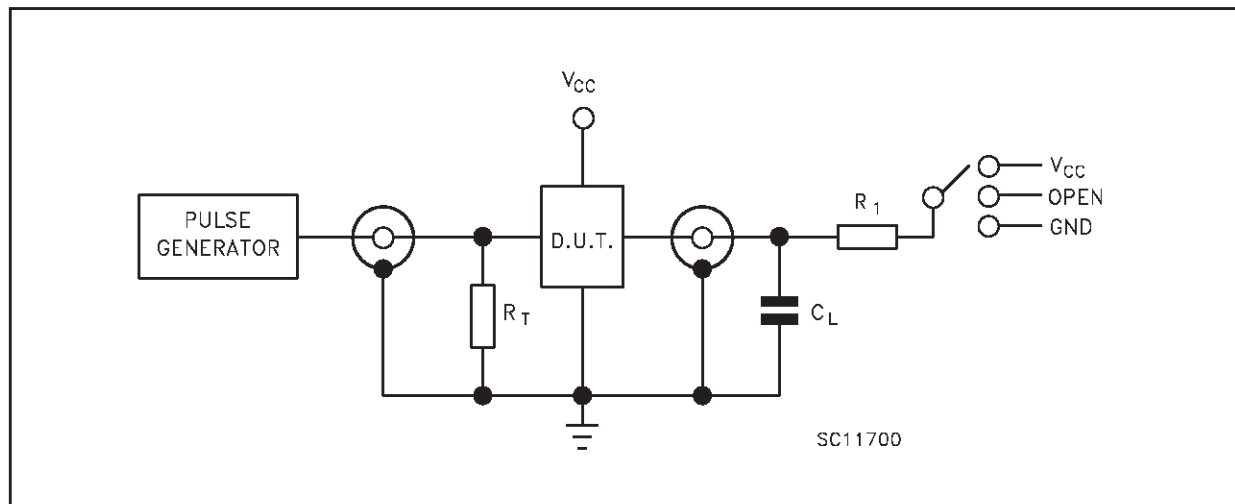
(*) Voltage range is 3.3V ± 0.3V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance	3.3			5			10		10	pF
C _{OUT}	Output Capacitance	3.3			10						pF
C _{PD}	Power Dissipation Capacitance (note 1)	3.3	f _{IN} = 10MHz		40						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per circuit)

TEST CIRCUIT



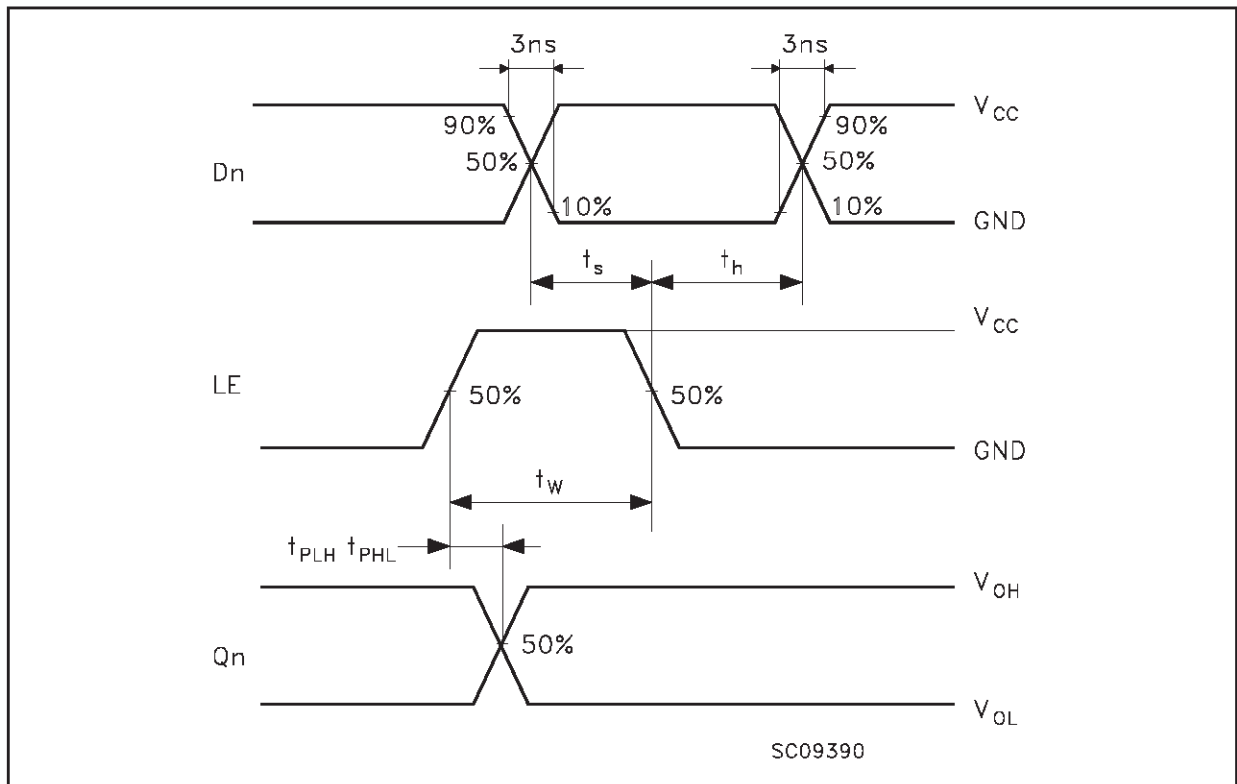
TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	V _{CC}
t _{PZH} , t _{PHZ}	GND

C_L = 15/50pF or equivalent (includes jig and probe capacitance)

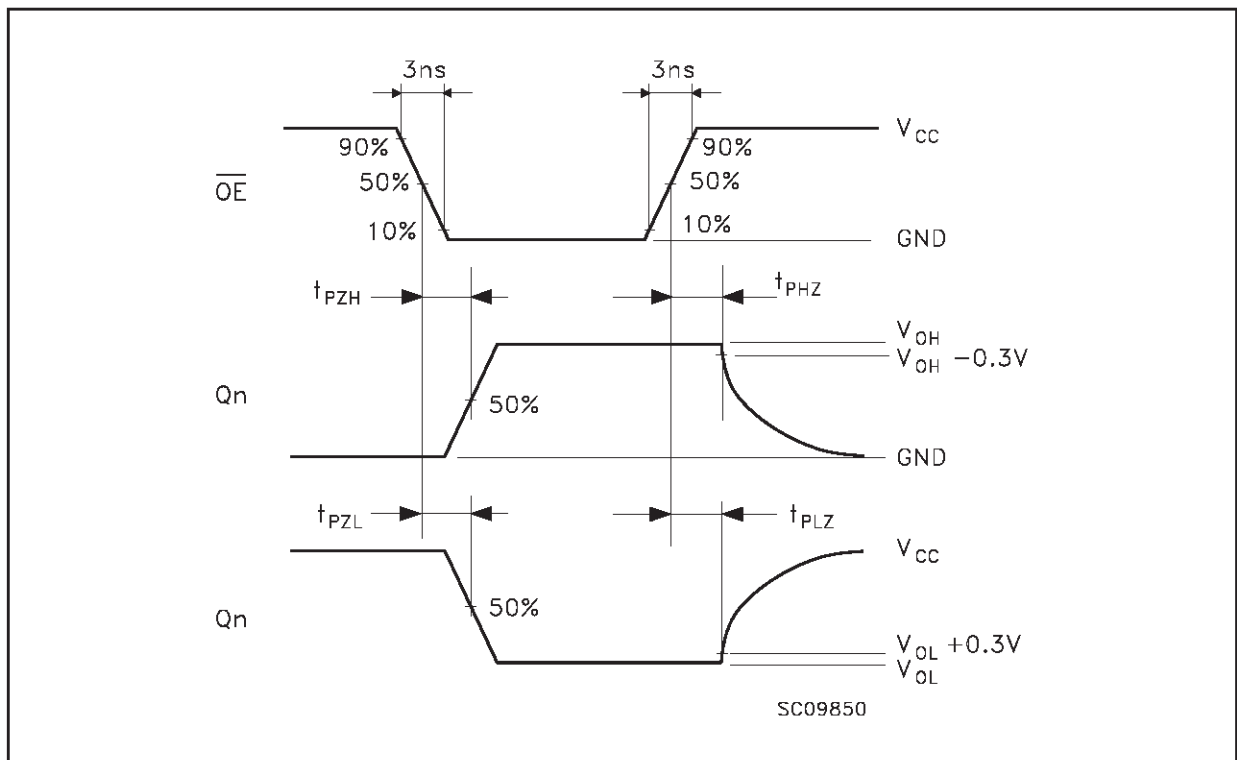
R_L = R₁ = 1KΩ or equivalent

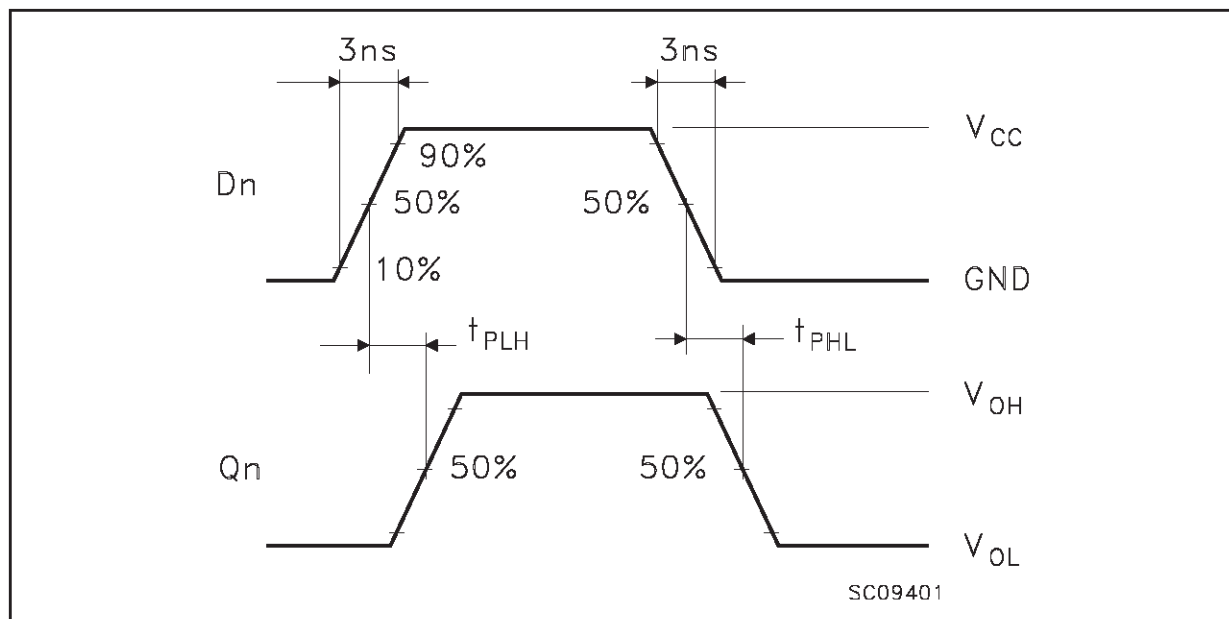
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1 : LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



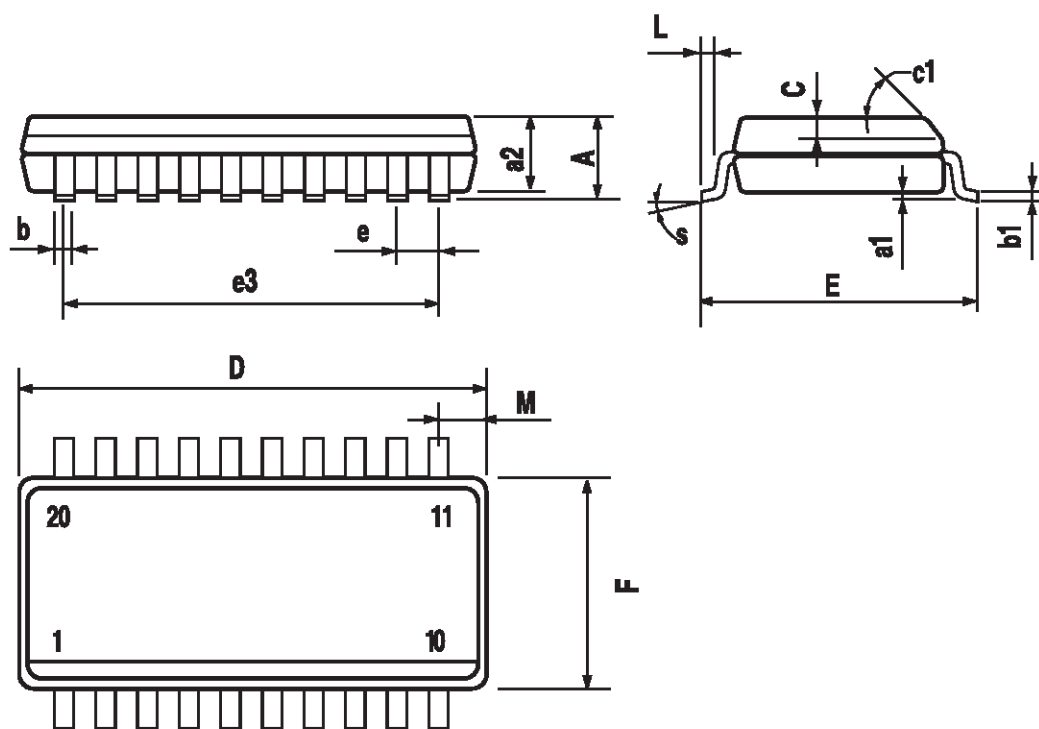
WAVEFORM 2 : OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 3 : PROPAGATION DELAY TIME ($f=1\text{MHz}$; 50% duty cycle)

SO-20 MECHANICAL DATA

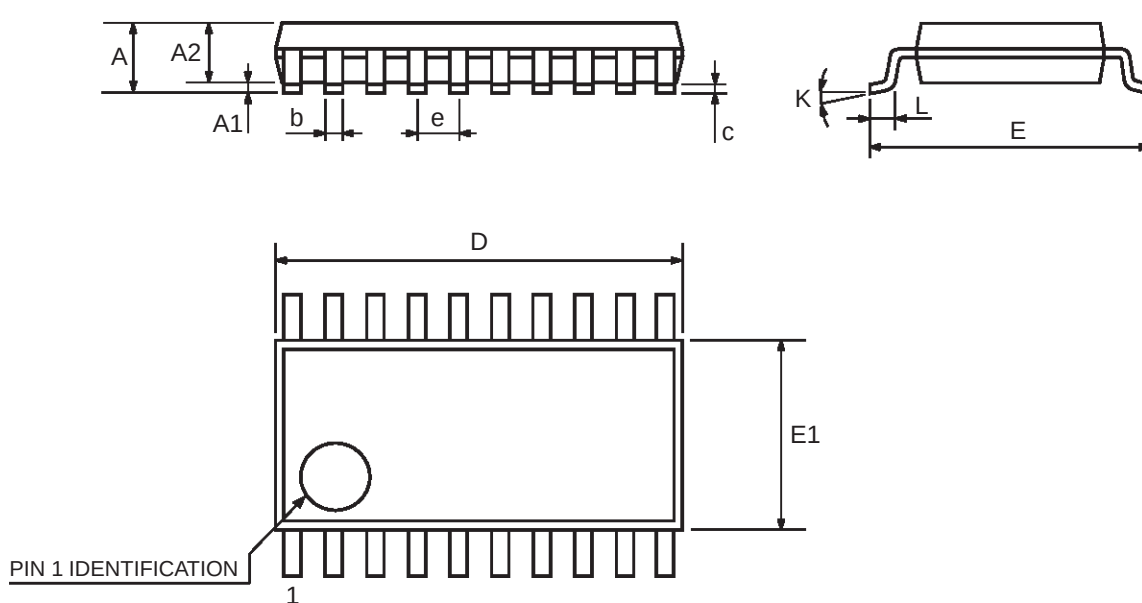
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



PO13L

TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0087225C

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>