



HOW TO MINIMIZE THE ST7 POWER CONSUMPTION

by Microcontroller Division Application Team

INTRODUCTION

The purpose of this document is to present a way of minimising the ST7 power consumption for low power applications. This note is based on the ST72311, but is applicable to all ST7 general purpose devices.

1 APPLICATION ENVIRONMENT AND CONFIGURATION

The ST7 allows four main running modes :

- Standard Run mode: $F_{CPU} = F_{OSC}/2$.
- Slow mode: $F_{CPU} = F_{OSC}/4, 8, 16$ or 32 .
- Wait mode, the CPU is stopped, The peripherals are still running.
- Halt mode, the oscillator is turned off.

For this application note, we consider the Watchdog Timer (WDG) enabled; therefore, the Halt mode can not be used as the “Halt” instruction resets the microcontroller when the WDG is enabled. The Wait mode is used, associated with the Slow mode optimum. This slow mode clock (F_{CPU}) drives the active peripherals and the CPU when it is wake-up. Of course, to improve performance, the Halt mode should be used.

In terms of applications, users usually try to optimize the power consumption during the wait loop in the main program. In this configuration the microcontroller is mostly idle, waiting for an external event, or regularly woken-up by an internal timer event. In our case, we decided to put the ST7 core in wait for interrupt, with one timer active to regularly wake up the core. This enables the core to refresh the WDG to avoid a watchdog reset. The clock driving the active peripherals and the core when it is active corresponds to the slowest clock available. It is the oscillator clock divided by 2 then divided by 16. So the peripherals and core clock (F_{CPU}) is equal to the crystal value (F_{OSC}) divided by 32.

APPLICATION ENVIRONMENT AND CONFIGURATION

To minimize the power consumption, the microcontroller is configured as described below, but of course in the application this configuration may differ, in particular the I/O port used.

- The optimum Slow mode is selected with the divided external clock factor equal to 32. This clock (F_{CPU}) drives the active peripherals (WDG and Timer B) and the core when it is active. In the Miscellaneous Register (MISCR) SMS and PSM1 & PSM0 bits must be set.
- All I/O ports are connected to an external pull-up or pull-down to avoid leakage due to floating inputs.
- The Watchdog Timer (WDG) is active with a maximum time-out period. The WDG Control Register (CR) must be loaded with the value FFh.
- One 16-bit timer is used to wake-up the core at regular intervals. The timer event period must be adjusted to maximum value to allow the core to refresh the WDG and to avoid a WDG reset. The timer clock equals $F_{CPU}/4$, in the Control Register (CR2) CC1, CC2 bits must be cleared.
- The external clock is selected on the unused 16-bit timer with a continuous level on the external clock pin. In the Control Register (CR2) CC1, CC2 bits must be set.

Note : If the timer A is used to regularly wake-up the WDG, the user only has to select the external clock on timer B. The continuous level on the timer input clock is already done internally, as there is no external I/O connected to the internal Timer B circuit.

On the contrary, if Timer B is used to wake-up the micro, the user has to select the external clock on Timer A and to fix a continuous level on the external clock pin. But be aware, on Timer A there is only one input capture and one output compare instead of two on Timer B.

- The main loop contains a Wait For Interrupt “WFI” instruction.
- Continuous low level on each PWM output (reset state)
- The A/D converter must be switched off. In the A/D Control/Status Register (CSR), the ADON bit must be cleared.
- The SPI and SCI are unused.

For the ST7 software configuration, please refer to your datasheet.

2 SOME MEASUREMENTS ON ST72E311

The measurement of current (I_{DD}) is done directly on the V_{DD} pin. The microcontroller is in Wait mode and is configured as described above, with the WDG and one 16-bit Timer active. The values given in Table 2 to Table 3 correspond to typical measured values. They are not maximum or minimum values.

The component values for the Crystal Resonator are (cf Crystal/Ceramic Resonator figure in the ST72311 datasheet, Clock System paragraph):

$$C_{OSIN} = C_{OSOUT} = 22\text{pF}$$

$$R_P = 10\text{ MOhm}$$

Table 1. I_{DD} in mA at $T = -40\text{ C}$

Crystal in MHz \ V_{DD} in V	4.5	5	5.5
4	0.32	0.40	0.48
8	0.48	0.59	0.71

Table 2. I_{DD} in mA at $T = +25\text{ C}$

Crystal in MHz \ V_{DD} in V	4.5	5	5.5
4	0.30	0.37	0.45
8	0.47	0.57	0.68

Table 3. I_{DD} in mA at $T = +125\text{ C}$

Crystal in MHz \ V_{DD} in V	4.5	5	5.5
4	0.30	0.36	0.43
8	0.46	0.56	0.65

3 CONCLUSION

The tables above show that the consumption of the ST7 MCUs is not dependant of the temperature. The Wait minimum mode (i.e. associated with the optimun slow mode) is the best way to minimize the power consumption during wait states.

CONCLUSION

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