



BTA/BTB06 Series

SNUBBERLESS™, LOGIC LEVEL & STANDARD

6A TRIACs

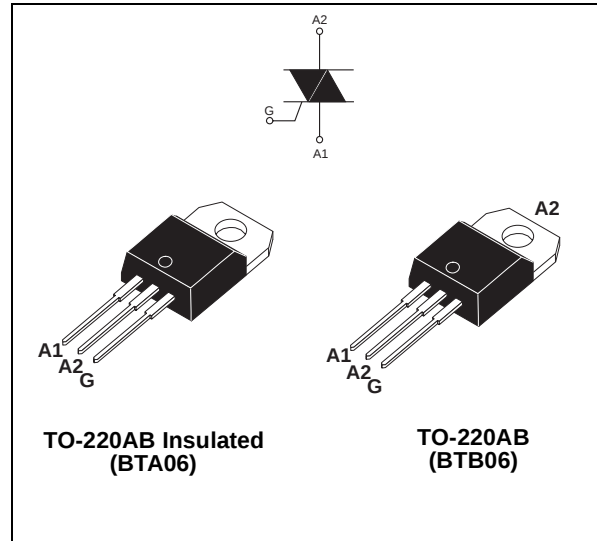
MAIN FEATURES:

Symbol	Value	Unit
$I_{T(RMS)}$	6	A
V_{DRM}/V_{RRM}	600 and 800	V
$I_G(Q_1)$	5 to 50	mA

DESCRIPTION

Suitable for AC switching operations, the BTA/BTB06 series can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits... or for phase control in light dimmers, motor speed controllers,...

The snubberless and logic level versions (BTA/BTB...W) are specially recommended for use on inductive loads, thanks to their high commutation performances. By using an internal ceramic pad, the BTA series provides voltage insulated tab (rated at 2500V RMS) complying with UL standards (File ref.: E81734)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	TO-220AB	$T_c = 110^\circ\text{C}$	6	A
		TO-220AB Ins.	$T_c = 105^\circ\text{C}$		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	F = 50 Hz	t = 20 ms	60	A
		F = 60 Hz	t = 16.7 ms	63	
I^2t	I^2t Value for fusing	tp = 10 ms		21	A^2s
di/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, tr ≤ 100 ns	F = 120 Hz	$T_j = 125^\circ\text{C}$	50	A/μs
I_{GM}	Peak gate current	tp = 20 μs	$T_j = 125^\circ\text{C}$	4	A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125^\circ\text{C}$	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125	$^\circ\text{C}$

BTA/BTB06 Series

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise specified)

■ SNUBBERLESS™ and LOGIC LEVEL (3 Quadrants)

Symbol	Test Conditions	Quadrant		BTA/BTB06				Unit
				TW	SW	CW	BW	
I _{GT} (1)	V _D = 12 V R _L = 30 Ω	I - II - III	MAX.	5	10	35	50	mA
V _{GT}		I - II - III	MAX.	1.3				V
V _{GD}	V _D = V _{DRM} R _L = 3.3 kΩ T _j = 125°C	I - II - III	MIN.	0.2				V
I _H (2)	I _T = 100 mA		MAX.	10	15	35	50	mA
I _L	I _G = 1.2 I _{GT}	I - III	MAX.	10	25	50	70	mA
		II		15	30	60	80	
dV/dt (2)	V _D = 67 %V _{DRM} gate open T _j = 125°C		MIN.	20	40	400	1000	V/μs
(dI/dt) _c (2)	(dV/dt) _c = 0.1 V/μs T _j = 125°C		MIN.	2.7	3.5	-	-	A/ms
	(dV/dt) _c = 10 V/μs T _j = 125°C			1.2	2.4	-	-	
	Without snubber T _j = 125°C			-	-	3.5	5.3	

■ STANDARD (4 Quadrants)

Symbol	Test Conditions	Quadrant		BTA/BTB06		Unit
				C	B	
I _G (1)	V _D = 12 V R _L = 30 Ω	I - II - III IV	MAX.	25 50	50 100	mA
V _{GT}		ALL	MAX.	1.3		V
V _{GD}	V _D = V _{DRM} R _L = 3.3 kΩ T _j = 125°C		MIN.	0.2		V
I _H (2)	I _T = 500 mA		MAX.	25	50	mA
I _L	I _G = 1.2 I _{GT}	I - III - IV	MAX.	40	50	mA
		II		80	100	
dV/dt (2)	V _D = 67 %V _{DRM} gate open T _j = 125°C		MIN.	200	400	V/μs
(dV/dt) _c (2)	(dI/dt) _c = 2.7 A/ms T _j = 125°C		MIN.	5	10	V/μs

STATIC CHARACTERISTICS

Symbol	Test Conditions		Value	Unit
V _T (2)	I _{TM} = 5.5 A tp = 380 μs	T _j = 25°C MAX.	1.55	V
V _{to} (2)	Threshold voltage	T _j = 125°C MAX.	0.85	V
R _d (2)	Dynamic resistance	T _j = 125°C MAX.	60	mΩ
I _{DRM}	V _{DRM} = V _{RDM}	T _j = 25°C	5	μA
I _{RDM}		T _j = 125°C	1	mA

Note 1: minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: for both polarities of A2 referenced to A1

THERMAL RESISTANCES

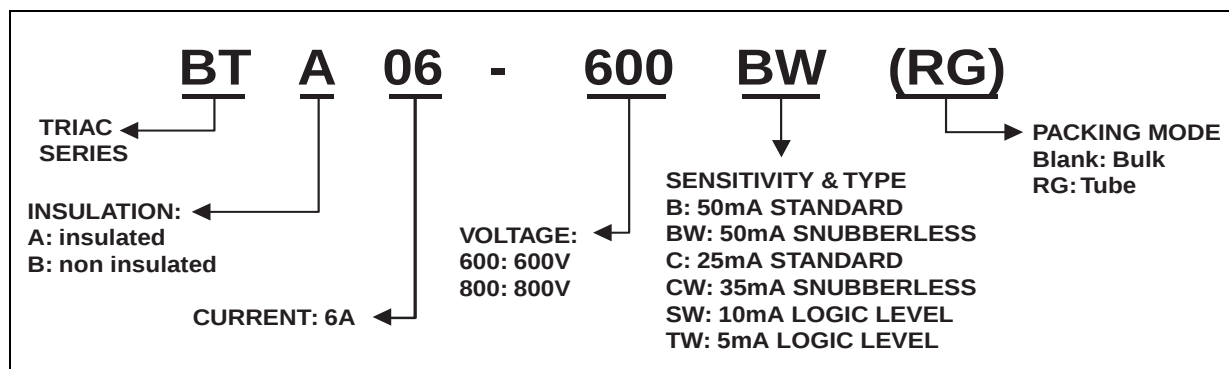
Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Junction to case (AC)	TO-220AB	°C/W
		TO-220AB Insulated	
$R_{th(j-a)}$	Junction to ambient	TO-220AB TO-220AB Insulated	°C/W

PRODUCT SELECTOR

Part Number	Voltage (xxx)		Sensitivity	Type	Package
	600 V	800 V			
BTA/BTB06-xxxB	X	X	50 mA	Standard	TO-220AB
BTA/BTB06-xxxBW	X	X	50 mA	Snubberless	TO-220AB
BTA/BTB06-xxxC	X	X	25 mA	Standard	TO-220AB
BTA/BTB06-xxxCW	X	X	35 mA	Snubberless	TO-220AB
BTA/BTB06-xxxSW	X	X	10 mA	Logic level	TO-220AB
BTA/BTB06-xxxTW	X	X	5 mA	Logic level	TO-220AB

BTB: non insulated TO-220AB package

ORDERING INFORMATION



OTHER INFORMATION

Part Number	Marking	Weight	Base quantity	Packing mode
BTA/BTB06-xxxxyz	BTA/BTB06-xxxxyz	2.3 g	250	Bulk
BTA/BTB06-xxxxyzRG	BTA/BTB06-xxxxyz	2.3 g	50	Tube

Note: xxx = voltage, y = sensitivity, z = type

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

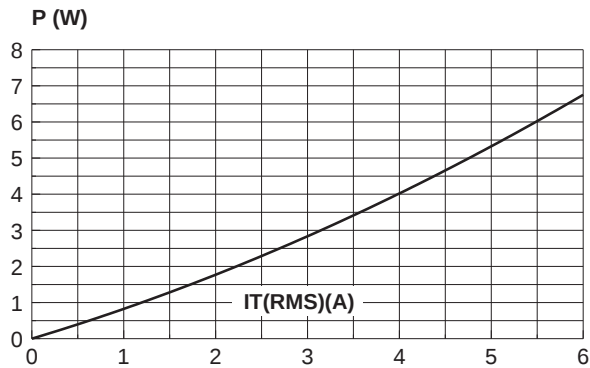


Fig. 3: Relative variation of thermal impedance versus pulse duration.

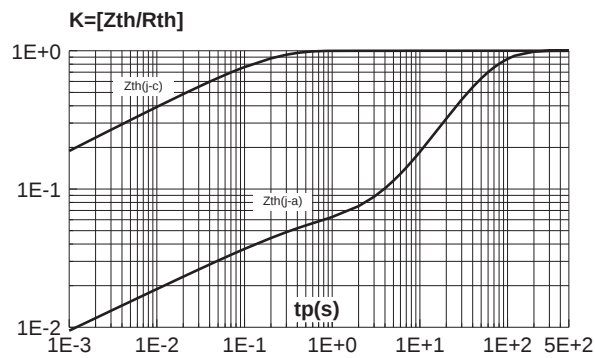


Fig. 5: Surge peak on-state current versus number of cycles.

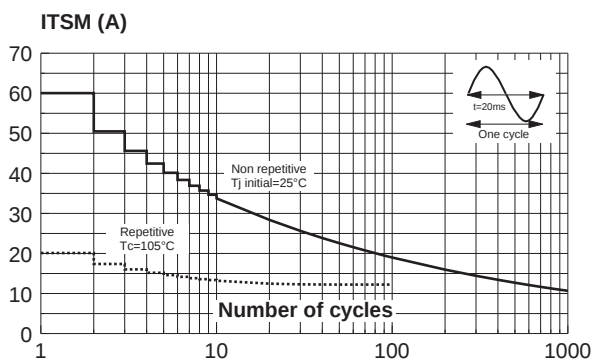


Fig. 2: RMS on-state current versus case temperature (full cycle).

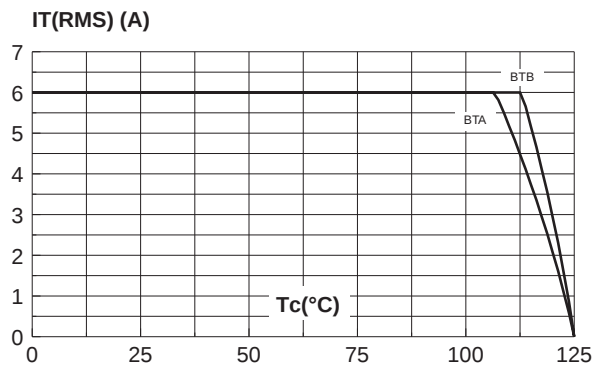


Fig. 4: On-state characteristics (maximum values).

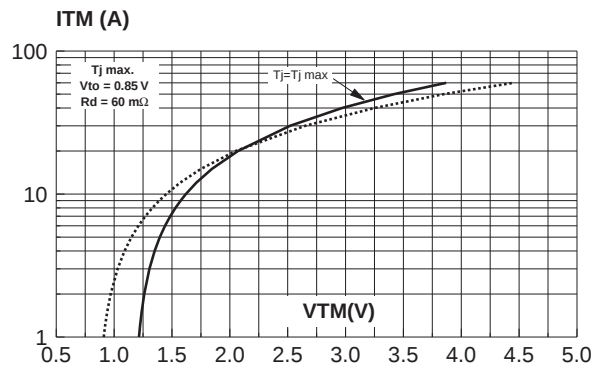


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ms}$, and corresponding value of I^2t .

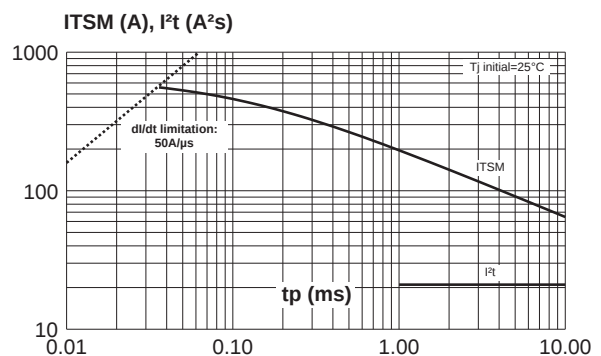


Fig. 7: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).

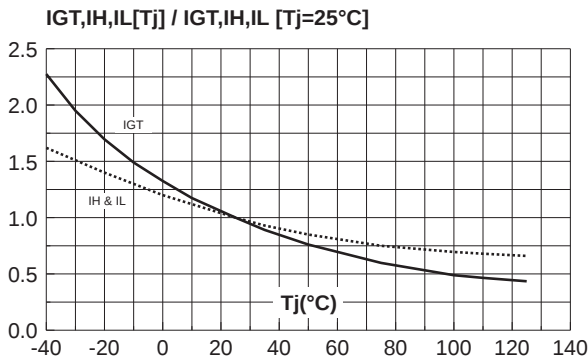


Fig. 8-1: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values). Snubberless & Logic Level Types

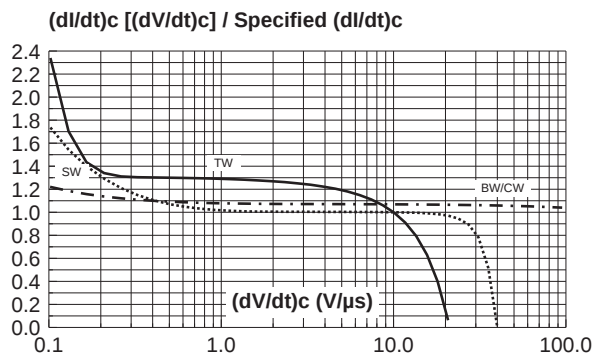


Fig. 8-2: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values). Standard Types

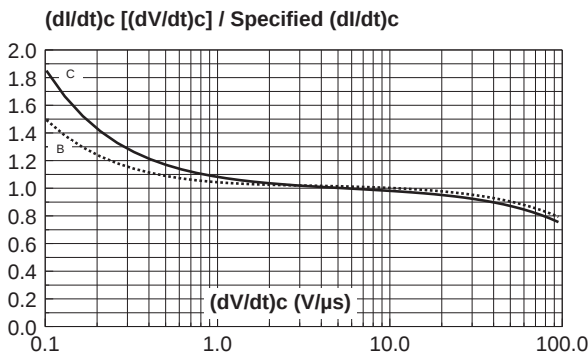
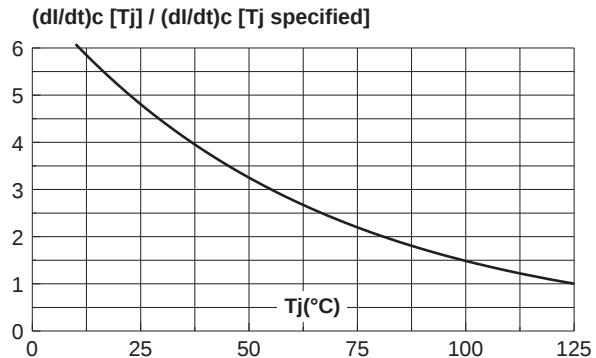


Fig. 9: Relative variation of critical rate of decrease of main current versus junction temperature.



PACKAGE MECHANICAL DATA

TO-220AB / TO-220AB Ins.

REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.20		15.90	0.598		0.625
a1		3.75			0.147	
a2	13.00		14.00	0.511		0.551
B	10.00		10.40	0.393		0.409
b1	0.61		0.88	0.024		0.034
b2	1.23		1.32	0.048		0.051
C	4.40		4.60	0.173		0.181
c1	0.49		0.70	0.019		0.027
c2	2.40		2.72	0.094		0.107
e	2.40		2.70	0.094		0.106
F	6.20		6.60	0.244		0.259
I	3.75		3.85	0.147		0.151
I4	15.80	16.40	16.80	0.622	0.646	0.661
L	2.65		2.95	0.104		0.116
I2	1.14		1.70	0.044		0.066
I3	1.14		1.70	0.044		0.066
M		2.60			0.102	

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES
 Australia - Brazil - Canada - China - Finland - France - Germany
 Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore
 Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>