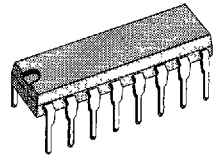
SGS-THOMSON MICROELECTRONICS

M145026
M145027 - M145028

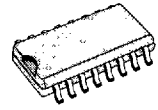
REMOTE CONTROL ENCODER/DECODER CIRCUITS

- M145026 ENCODER
- M145027/M145028 DECODERS
- MAY BE ADDRESSED IN EITHER BINARY OR TRINARY
- TRINARY ADDRESSING MAXIMIZES NUMBER OF CODES
- INTERFACES WITH RF, ULTRASONIC, OR INFRARED TRANSMISSION MEDIAS
- DOUBLE TRANSMISSIONS FOR ERROR CHECKING
- 4.5V TO 18V OPERATION
- ON-CHIP R/C OSCILLATOR, NO CRYSTAL REQUIRED
- HIGH EXTERNAL COMPONENT TOLERANCE, CAN USE 5% COMPONENTS
- STANDARD CMOS B-SERIES INPUT AND OUTPUT CHARACTERISTICS
- APPLICATIONS INCLUDE GARAGE DOOR OPENERS, REMOTE CONTROLLED TOYS, SECURITY MONITORING, ANTITHEFT SYSTEMS, LOW END DATA TRANSMISSIONS WIRE LESS TELEPHONES



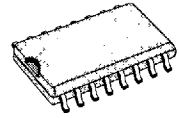
DIP16 (0.25")
(Plastic package)

ORDER CODES :
M145026B1
M145027B1
M145028 B1



SO16 Narrow (0.15")
(Plastic package)

ORDER CODE : M145026D



SO16 Large (0.3")
(Plastic package)

ORDER CODE : M145028D

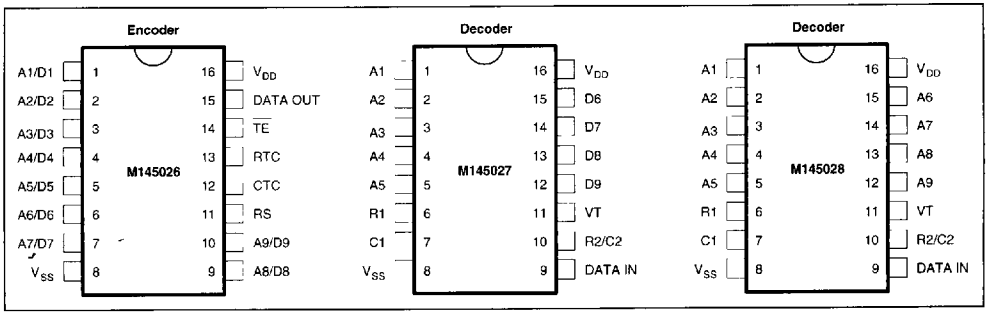
DESCRIPTION

The M145026 encodes nine bits of information and serially transmits this information upon receipt of a transmit enable, $\overline{TE}$, (active low) signal. Nine inputs may be encoded with tnnary data (0,1, open) to allow 3^9 (19.683) different codes.

Two decoders are presently available. Both use the same transmitter - the M145026. The decoders will receive the 9-bit word and will interpret some of the bits as address codes and some as data. The M145027 interprets the first five transmitted bits as address and the last four bits as data. The M145028 treats all nine bits as address. If no errors are received, the M145027 outputs the four data bits when the transmitter sends address codes that match that of the receiver. A valid transmission output goes high on both decoders when they recognize an address that matches that of the decoder. Other receivers can be produced with different address/data ratios.

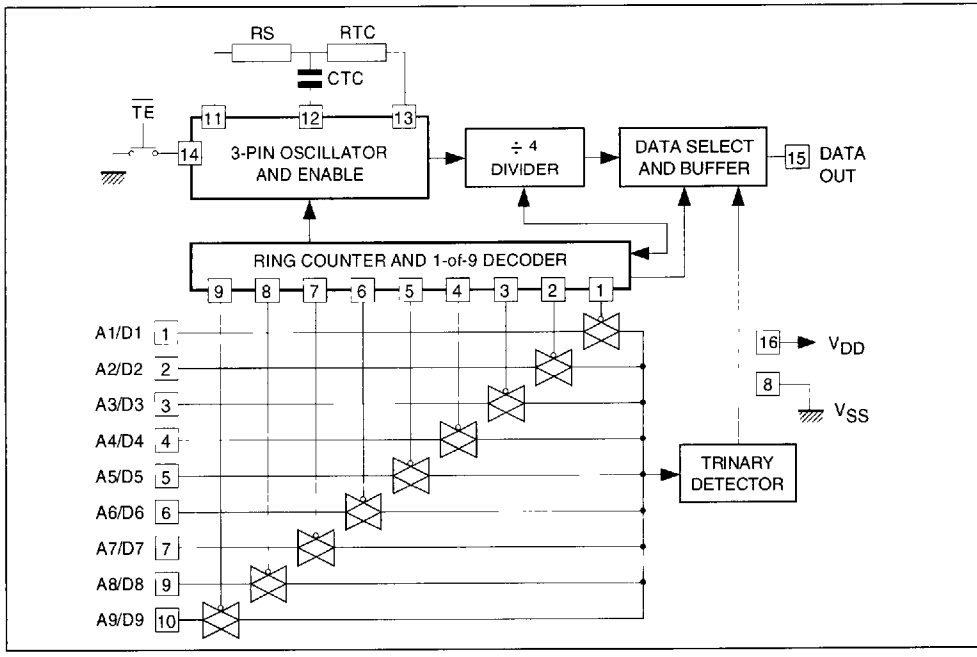
All the devices are available in 16 lead plastic package. The M145026 is available in SO16 plastic package (narrow) and the M145028 is available in SO16 plastic package (large).

PIN CONNECTIONS



BLOCK DIAGRAMS

Figure 1 : Encoder M145026



BLOCK DIAGRAMS (continued)

Figure 2 : Decoder M145027

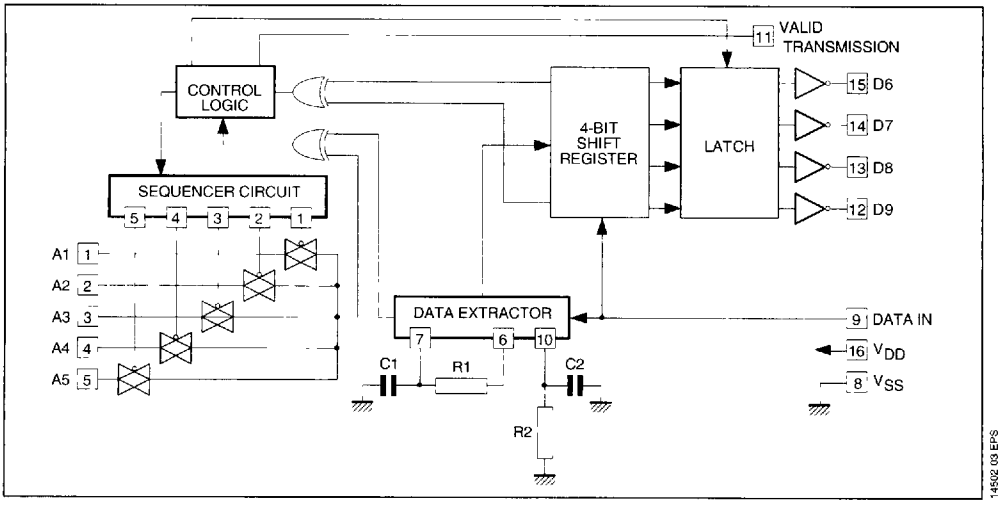
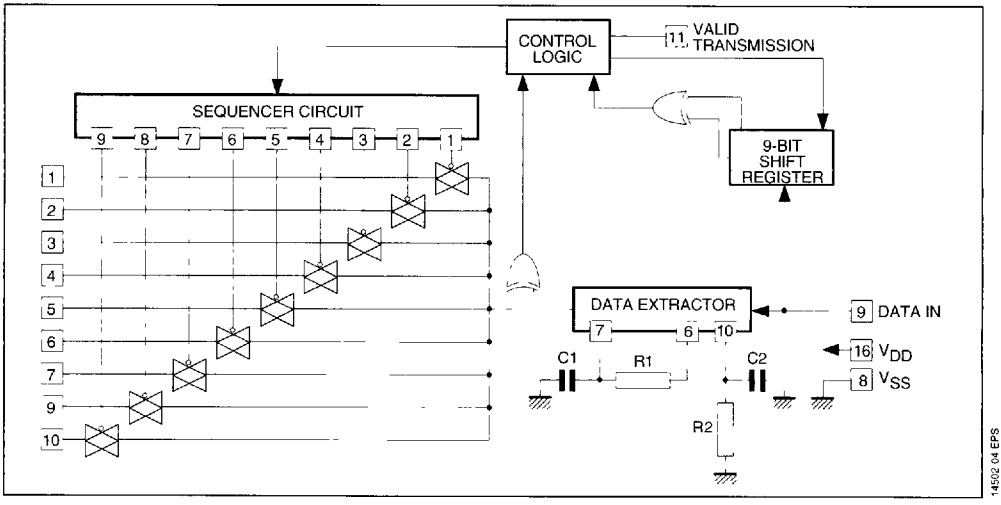


Figure 3 : Decoder M145028



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	− 0 5 to + 18	V
V_i	Input Voltage, All Inputs	− 0 5 to V_{DD} + 0.5	V
I_I	DC Current Drain Per Pin	10	mA
T_{stg}	Storage Temperature Range	− 65, + 150	°C
T_{op}	Operating Temperature Range	− 40, + 85	°C

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Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device This is a stress rating only and functional operation of the device at thses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

SWITCHING CHARACTERISTICS (C_L = 50pF, T_{amb} = 25°C)

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit
t_{TLH} t_{THL}	Output Rise and Fall Time	5 10 15		100 50 40	200 100 80	ns ns ns
t_{TLH} t_{THL}	Data in Rise and Fall Time (M145027 - M145028)	5 10 15			15 15 15	ms ms ms
f_{CL}	Encoder Clock Frequency	5 10 15	0 0 0		2 5 5	MHz MHz MHz
t_{WL}	Maximum Decoder Frequency (referenced to encoder clock) (see Figure 9)	5 10 15			240 410 450	kHz kHz kHz
	$\overline{TE}$ Pulse Width	5 10 15	65 30 20			ns ns ns
	System Propagation Delay ($\overline{TE}$ to valid transmission)			182		Clock Cycles
	Tolerance on Timing Components $\Delta RTC + \Delta CTC + \Delta R1 + \Delta C1$ $\Delta R2 + \Delta C2$				±25 ±25	% %

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ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{DD} (V)	-40°C		25°C			+85°C		Unit
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OL}	Output Low Level Voltage (V_I = V_{DD} or 0, "0" Level)	5 10 15		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V V V
V_{OH}	Output High Level Voltage (V_I = V_{DD} or 0, "1" Level)	5 10 15	4.95 9.95 14.95		4.95 9.95 14.95			4.95 9.95 14.95		V V V
V_{IL}	Input Low Level Voltage ("0" Level) V_O = 4.5 or 0.5V V_O = 0.9 or 1V V_O = 13.5 or 1.5V	 5 10 15		 1.5 3 4		 2.25 4.50 6.25	 1.5 3 4		 1.5 3 4	 V V V
V_{IH}	Input High Level Voltage ("1" Level) V_O = 4.5 or 0.5V V_O = 0.9 or 1V V_O = 13.5 or 1.5V	 5 10 15	 3.5 7 11		 3.5 7 11	 2.75 5.50 8.25		 3.5 7 11		 V V V
I_{OH}	Output Drive Source Current V_{OH} = 2.5V V_{OH} = 4.6V V_{OH} = 9.5V V_{OH} = 13.5V	 5 5 10 15	 -2.5 -0.52 -1.3 -3.6		 -2.1 -0.44 -1.1 -3	 -4.2 -0.88 -2.25 -8.8		 -1.7 -0.36 -0.9 -2.4		 mA mA mA mA
I_{OL}	Output Drive Sink Current V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V	 5 10 15	 0.52 1.3 3.6		 0.44 1.1 3	 0.88 2.25 8.8		 0.36 0.9 2.4		 mA mA mA
I_I	Input Current $\overline{TE}$ (M145026, pull up devide)	5 10 15			3 16 35	4 20 45	7 26 55			µA µA µA
I_I	Input Current RS (M145026) Data In (M145027 - M145028)	15		±0.3		±0.00001	±0.3		±1.0	µA
I_I	Input Current A1/D1-A9/D9 (M145026) A1-A5 (M145027) A1-A9 (M145028)	 5 10 15				 ±55 ±300 ±650	 ±80 ±340 ±725			 µA µA µA
C_I	Input Capacitance (V_I = 0)					5	7.5			pF

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ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	V_{DD} (V)	-40°C		25°C			+85°C		Unit
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
C_I	Input Capacitance (V_I = 0)					5	7.5			pF
I_{DD}	Quiescent Current (M145026)	5 10 15				0.0050 0.0100 0.0150	0.10 0.20 0 30			µA µA µA
I_{DD}	Quiescent Current (M145027 - M145028)	5 10 15				30 60 90	50 100 150			µA µA µA
I_T	Total Supply Current (f_{CL} = 20kHz) (M145026)	5 10 15				100 200 300	200 400 600			µA µA µA
I_T	Total Supply Current (f_{CL} = 20kHz) (M145027 - M145028)	5 10 15				200 400 600	400 800 1200			µA µA µA

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OPERATING CHARACTERISTICS

M145026

The encoder will serially transmit nine bits of trinary data as defined by the state of the A1/D1-A9/D9 input pins. These pins can be in either of three states (0,1, open) allowing 3^9 = 19683 possible codes. The transmit sequence will be initiated by a low level of the $\overline{TE}$ input pin. Each time the $\overline{TE}$ input is forced low the encoder will output two identical data words. This redundant information is used by the receiver to reduce errors. If the $\overline{TE}$ input is kept low, the encoder will continuously transmit the data words. The transmitted words are self-completing (two words will be transmitted for each $\overline{TE}$ pulse).

Each transmitted data bit is encoded into two data pulses. A logic zero will be encoded as two consecutive short pulses, a logic one by two consecutive long pulses, and an open as a long pulse followed by a short pulse. The input state is determined by using a weak output device to try to force each input first low, then high. If only a high state results from the two tests, the input is assumed to be hard wired to V_{DD}. If only a low state is obtained, the input is assumed to be hard wired to V_{SS}. If both a high and a low can be forced at an input, it is assumed to be open and is encoded as such.

The transmit sequence is enabled by a logic zero on the $\overline{TE}$ input. This input has an internal pullup device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high the encoder is completely disabled, the oscillator is inhibited and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started, and an internal reset is generated to initialize the transmit sequence. Each input is then sequentially selected and a determination is made as to input logic state. This information is serially transmitted via the Data Out output pin.

M145027

The decoder will receive the serial data from the encoder, check it for errors and output data if valid. The transmitted data consisting of two identical data words is examined bit by bit as it is received. The first five bits are assumed to be address bits and must be encoded to match the address inputs at the receiver. If the address bits match, the next four (data) bits are stored and compared to the last valid data stored. if this data matches, the VT pin will go high on the 2nd rising edge of the 9th bit of the first word. Between the two data words no signal is sent for three data bit times. As the second encoded word is received, the address must again match, and if it does, the data bits are checked against the previously stored data bits. If the two words of data (four bits each) match, the data is transferred to the output data latches and will remain until new data replaces it. At the same time, the Valid Transmission output pin is brought high and will remain high until an error is received or until no input signal is received for four data bit times.

Although the address information is encoded in trinary fashion, the data information must be either a one or a zero. A trinary (open) will be decoded as a logic one.

M145028

This receiver operates in the same manner as the M145027 except that nine address bits are used and no data output is available. The Valid Transmission output is used to indicate that a valid signal has been received.

Although address information normally is encoded in trinary, the designer should be aware that, for the M145028, the ninth address bit (A9) must be either a one or a zero. This part, therefore, can accept only 2 x 3^8 = 13.122 different codes. A trinary (open) A9 will be interpreted as a logic 1. However if the trans-

mitter sends a trinary (or logic 1) and the receiver address is a logic 1 (or trinary) respectively, the valid transmission output will be shortened to the R1 x C1 time constant.

DOUBLE TRANSMISSION DECODING

Although the encoder sends two words fo error checking, a decoder does not necessarily wait for two transmitted words to be received before issuing a valid transmission output. Refer to the flowcharts in Figures 7 and 8.

PIN DESCRIPTION

M145026 ENCODER

A1/D1-A9/D9. These inputs will be encoded and the data serially output form the encoder.

V_{SS}. The most negative supply (usually ground).

RS, CTC, RTC. These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator it should be connected to the RS input and the RTC and CTC pins should be left open.

$\overline{TE}$. This Transmit-Enable (active low) input will initiate transmission when forced low. A pullup device will keep this input high normally.

DATA OUT. This is the output of the encoder that will present the serially encoded signals.

V_{DD}. The most positive supply.

M145027/M145028 DECODERS

A1-A5 (M145027) / A1-A9 (M145028). These are the address inputs that must match the encoder inputs A1/D1-A5/D5 in the case of M145027 or A1/D1-A0/D9 in the case of M145028, in order for the decoder to output data.

D6-D9 (M145027). These outputs will give the information that is presented to the encoder inputs A6/D6-A9/D9.

Note: Only binary data will be acknowledged, a trinary open will be decoded as logic one.

R1, C1. These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant R1 x C1 should be set to 1.72 transmit clock periods. R1C1 = 3.95 RTC x CTC.

R2/C2. This pin accepts a resistor to V_{SS} and a capacitor to V_{SS} that are used to detect both the end of an encoded word and the end of transmission. The time constant R2 x C2 should be 33.5 transmit clock periods (four data bit periods). This time constant is used to determine that the Data In input has remained low for four data bit times (end of transmission). A separate comparator looks at a voltage equivalent two data bit times (0.4 R2C2) to detect the dead time between transmitted words. R2C2 = 77 x RTC x CTC.

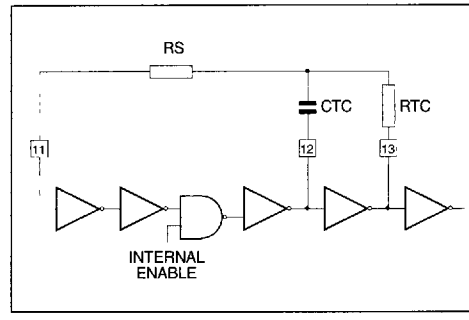
VALID TRANSMISSION, VT. This output will go high when the following conditions are satisfied:

1. the transmitted address matches the receiver address, and
2. the transmitted data matches the last valid data received (M145028 only).

VT will remain high until either a mismatch is received, or no input signal is received for four data data bit times.

V_{DD}. The most positive supply.
V_{SS}. The most negative supply (usually ground).

Figure 4 : Encoder Oscillator Information



This oscillator will operate at a frequency determined by the external RC network; i.e..

$$f \approx \frac{1}{2.3 \cdot RTC \cdot CTC} \text{ (Hz) for 1 kHz} \leq f \leq 400 \text{ kHz}$$

where: CTC = CTC + C layout + 12 pF
RS ≈ 2 RTC
RS ≥ 20 k
RTC ≥ 10 k
400pF < CTC < µF

The value for RS should be chosen to be about 2 times RTC. This range will ensure that current through RS is insignificant compared to current through RTC. The upper limit for RS must ensure that RS x 5 pF (input capacitance) is small compared to RTC x CTC. For frequencies outside the indicated range, the formula will be less accurate. The actual oscillation range of this circuit is from less than 1Hz to over 1MHz.

Figure 5 : Encoder/Decoder Timing Diagram

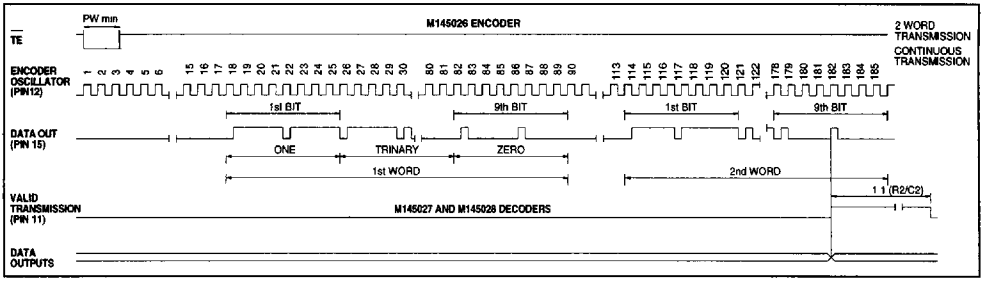


Figure 6 : Encoder Data Waveforms (M145026)

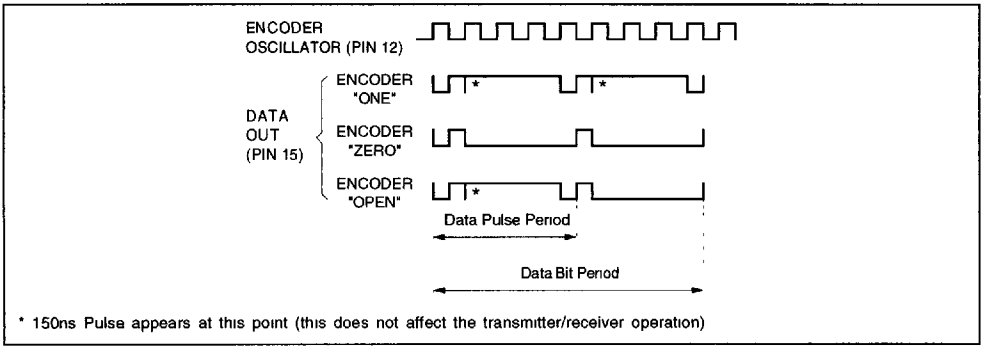


Figure 7 : M145027 Flowchart

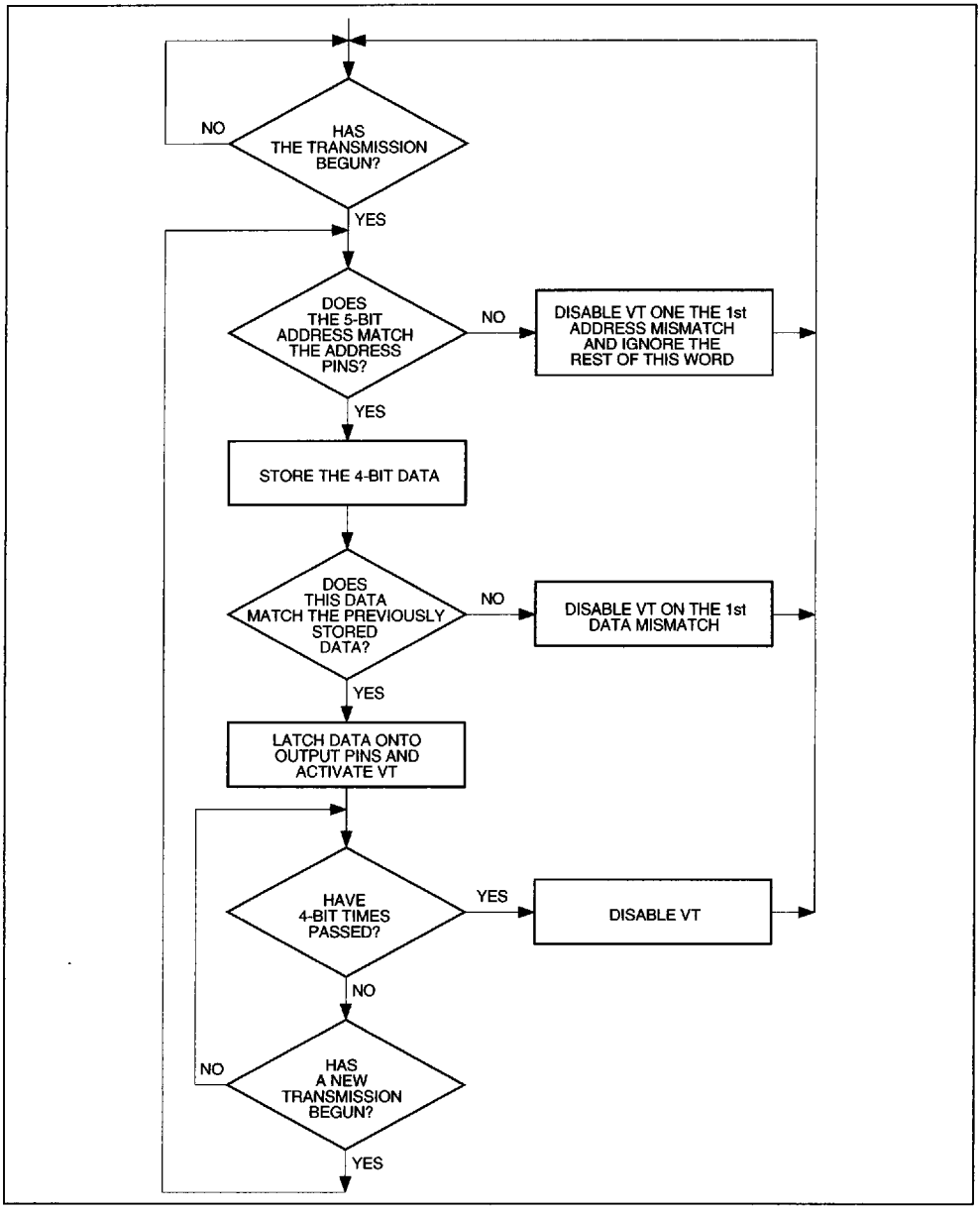


Figure 8 : M145028 Flowchart

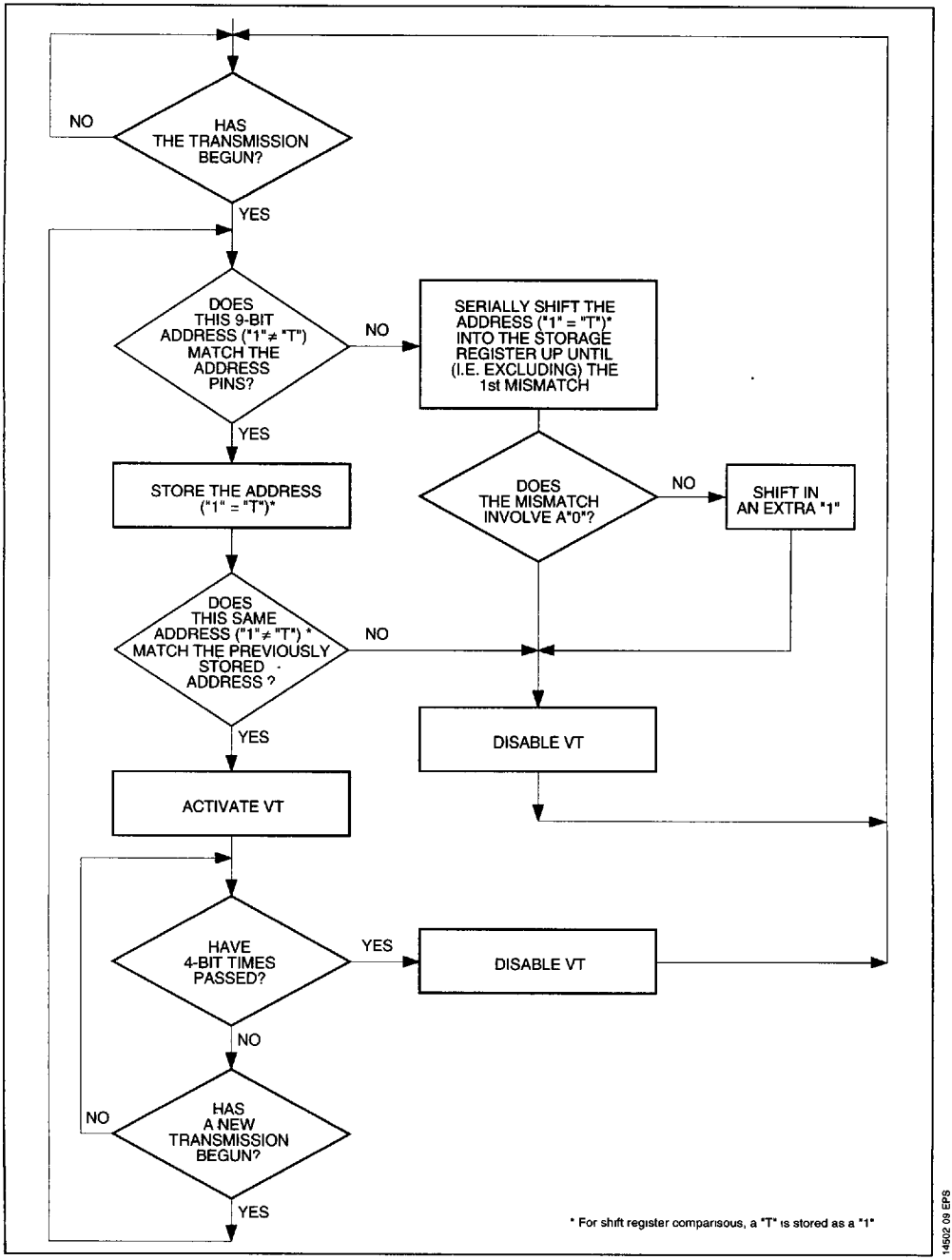


Figure 9 : M145027/M145028 (f_{max} vs. C_{layout})

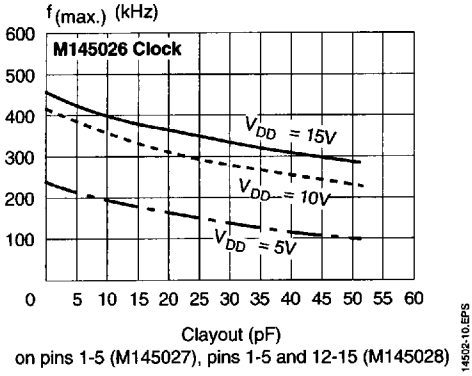
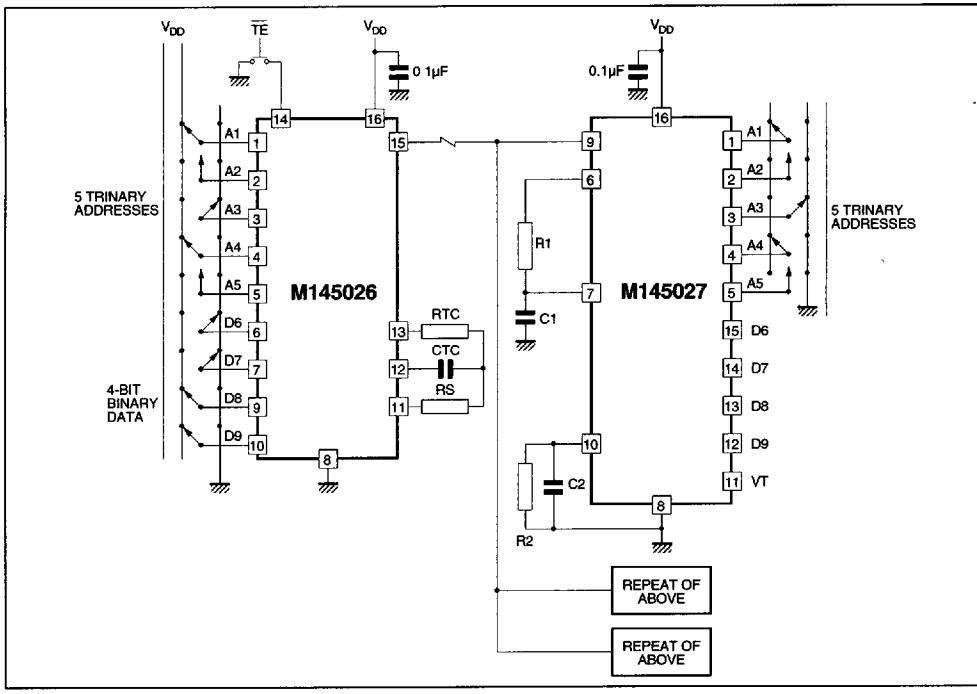


Figure 10 : Typical Application



Example R/C Values (all resistors and capacitors are ± 5 %) (CTC' = CTC + 20pF)

f_{osc} (kHz)	RTC	CTC'	RS	R1	C1	R2	C2
362	10k	120pF	20k	10k	470pF	100k	910pF
181	10k	240pF	20k	10k	910pF	100k	1800pF
88.7	10k	490pF	20k	10k	2000pF	100k	3900pF
42.6	10k	1020pF	20k	10k	3900pF	100k	7500pF
21.5	10k	2020pF	20k	10k	8200pF	100k	0.015µF
8.53	10k	5100pF	20k	10k	0.02µF	200k	0.02µF
1.71	50k	5100pF	100k	50k	0.02µF	200k	0.1µF

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