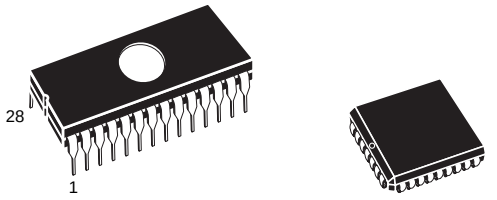
# M27C64A

## 64 Kbit (8Kb x8) UV EPROM and OTP EPROM

- 5V ± 10% SUPPLY VOLTAGE in READ OPERATION
- ACCESS TIME: 150ns
- LOW POWER “CMOS” CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.5V ± 0.25V
- HIGH SPEED PROGRAMMING (less than 1 minute)
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 9Bh
  - Device Code: 08h




FDIP28W (F)



PLCC32 (C)

### DESCRIPTION

The M27C64A is a 64Kbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large programs and is organized as 8,192 by 8 bits.

The FDIP28W (window ceramic frit-seal package) has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only on time and erasure is not required, the M27C64A is offered in PLCC32 package.

**Figure 1. Logic Diagram**

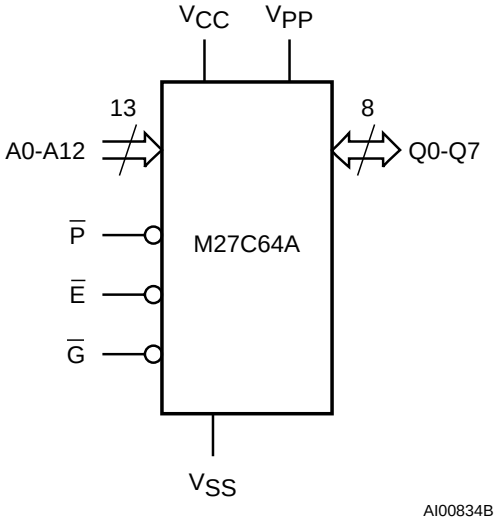


**Figure 2A. DIP Connections**

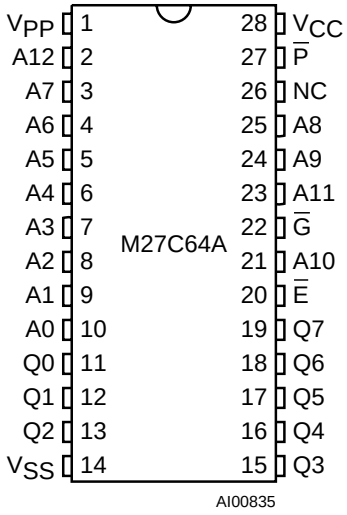



**Figure 2B. Pin Connections**

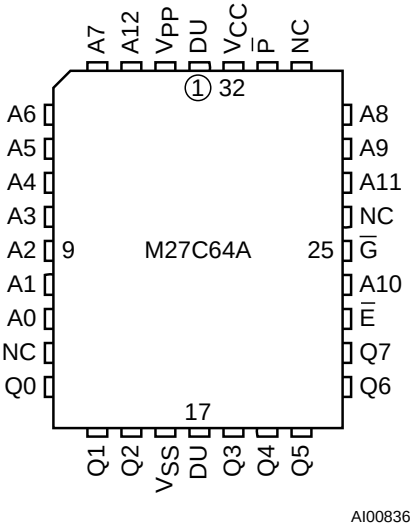



**Table 1. Signal Names**

| | |
|---|---|
| A0-A12 | Address Inputs |
| Q0-Q7 | Data Outputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{P}$ | Program |
| $V_{PP}$ | Program Supply |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |
| NC | Not Connected Internally |
| DU | Don't Use |

## DEVICE OPERATION

The modes of operation of the M27C64A are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for $V_{PP}$ and 12V on A9 for Electronic Signature.

### Read Mode

The M27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time ($t_{AVQV}$) is equal to the delay from $\overline{E}$ to output ($t_{ELQV}$). Data is available at the output after a delay of $t_{GLQV}$ from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least $t_{AVQV}$-$t_{GLQV}$.

**Table 2. Absolute Maximum Ratings (1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature (3) | –40 to 125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –50 to 125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to 150 | °C |
| $V_{IO}$ (2) | Input or Output Voltage (except A9) | –2 to 7 | V |
| $V_{CC}$ | Supply Voltage | –2 to 7 | V |
| $V_{A9}$ (2) | A9 Voltage | –2 to 13.5 | V |
| $V_{PP}$ | Program Supply Voltage | –2 to 14 | V |

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is $V_{CC}$ +0.5V with possible overshoot to $V_{CC}$ +2V for a period less than 20ns.
3. Depends on range.

**Table 3. Operating Modes**

| Mode | $\overline{E}$ | $\overline{G}$ | $\overline{P}$ | A9 | $V_{PP}$ | Q70-Q0 |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $V_{CC}$ | Data Out |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | $V_{CC}$ | Hi-Z |
| Program | $V_{IL}$ | X | $V_{IL}$ Pulse | X | $V_{PP}$ | Data Input |
| Verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | $V_{PP}$ | Data Output |
| Program Inhibit | $V_{IH}$ | X | X | X | $V_{PP}$ | Hi-Z |
| Standby | $V_{IH}$ | X | X | X | $V_{CC}$ | Hi-Z |
| Electronic Signature | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{ID}$ | $V_{CC}$ | Codes |

Note: X = $V_{IH}$ or $V_{IL}$, $V_{ID}$ = 12V ± 0.5V.

**Table 4. Electronic Signature**

| Identifier | A0 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer's Code | $V_{IL}$ | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 9Bh |
| Device Code | $V_{IH}$ | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08h |

**Table 5. AC Measurement Conditions**

| | |
|---|---|
| Input Rise and Fall Times | ≤ 20ns |
| Input Pulse Voltages | 0.4V to 2.4V |
| Input and Output Timing Ref. Voltages | 0.8 to 2.0V |

Note that Output Hi-Z is defined as the point where data is no longer driven.

**Figure 3. AC Testing Input Output Waveform**

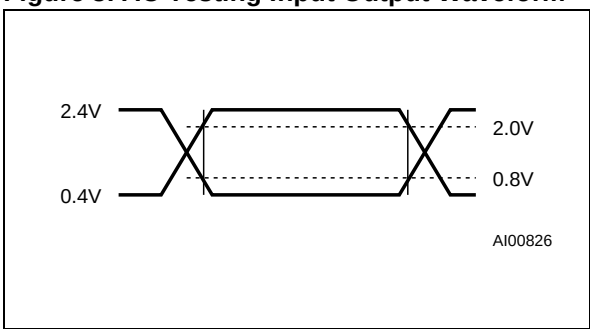



**Figure 4. AC Testing Load Circuit**

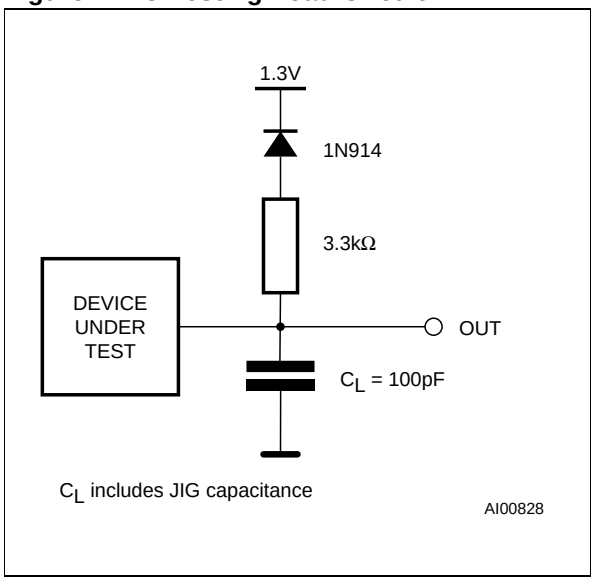



**Table 6. Capacitance (1)** ($T_A$ = 25 °C, f = 1 MHz)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 12 | pF |

Note: 1. Sampled only, not 100% tested.

### Standby Mode

The M27C64A has a standby mode which reduces the active current from 30mA to 100µA. The M27C64A is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

### Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

**Table 7. Read Mode DC Characteristics (1)**
($T_A$ = 0 to 70 °C or –40 to 85 °C: $V_{CC}$ = 5V ± 10%; $V_{PP}$ = $V_{CC}$)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | ±10 | µA |
| $I_{LO}$ | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | | ±10 | µA |
| $I_{CC}$ | Supply Current | $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $I_{OUT}$ = 0mA, f = 5MHz | | 30 | mA |
| $I_{CC1}$ | Supply Current (Standby) TTL | $\overline{E} = V_{IH}$ | | 1 | mA |
| $I_{CC2}$ | Supply Current (Standby) CMOS | $\overline{E} > V_{CC} - 0.2V$ | | 100 | µA |
| $I_{PP}$ | Program Current | $V_{PP} = V_{CC}$ | | 100 | µA |
| $V_{IL}$ | Input Low Voltage | | –0.3 | 0.8 | V |
| $V_{IH}$ (2) | Input High Voltage | | 2 | $V_{CC}$ + 1 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage TTL | $I_{OH}$ = –400µA | 2.4 | | V |
| | Output High Voltage CMOS | $I_{OH}$ = –100µA | $V_{CC}$ – 0.7V | | |

Note: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Maximum DC voltage on Output is $V_{CC}$ +0.5V.

## System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, $I_{CC}$, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between $V_{CC}$ and $V_{SS}$. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between $V_{CC}$ and $V_{SS}$ for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

**Table 8. Read Mode AC Characteristics (1)**
($T_A$ = 0 to 70 °C or –40 to 85 °C: $V_{CC}$ = 5V ± 10%; $V_{PP}$ = $V_{CC}$)

| Symbol | Alt | Parameter | Test Condition | M27C64A | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | -15 | | -20 | | -25 | | -30 | | |
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | | 150 | | 200 | | 250 | | 300 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | $\overline{G}$ = $V_{IL}$ | | 150 | | 200 | | 250 | | 300 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | $\overline{E}$ = $V_{IL}$ | | 75 | | 80 | | 100 | | 120 | ns |
| $t_{EHQZ}$(2) | $t_{DF}$ | Chip Enable High to Output Hi-Z | $\overline{G}$ = $V_{IL}$ | 0 | 50 | 0 | 50 | 0 | 60 | 0 | 105 | ns |
| $t_{GHQZ}$(2) | $t_{DF}$ | Output Enable High to Output Hi-Z | $\overline{E}$ = $V_{IL}$ | 0 | 50 | 0 | 50 | 0 | 60 | 0 | 105 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Address Transition to Output Transition | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | 0 | | 0 | | 0 | | 0 | | ns |

Note: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Sampled only, not 100% tested.

**Figure 5. Read Mode AC Waveforms**

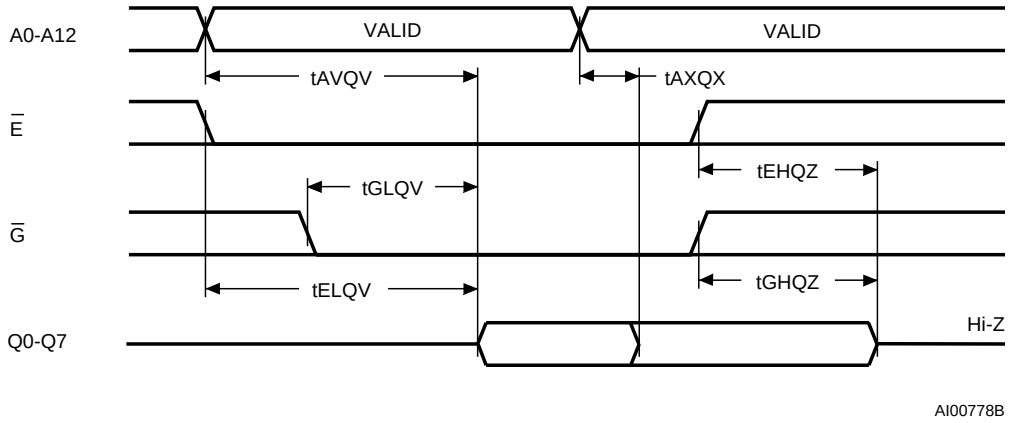


**Table 9. Programming Mode DC Characteristics (1)**
($T_A$ = 25 °C; $V_{CC}$ = 6V ± 0.25V; $V_{PP}$ = 12.5V ± 0.25V)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IL} \le V_{IN} \le V_{IH}$ | | ±10 | µA |
| $I_{CC}$ | Supply Current | | | 30 | mA |
| $I_{PP}$ | Program Current | $\overline{E} = V_{IL}$ | | 30 | mA |
| $V_{IL}$ | Input Low Voltage | | –0.3 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage TTL | $I_{OH}$ = –400µA | 2.4 | | V |
| $V_{ID}$ | A9 Voltage | | 11.5 | 12.5 | V |

Note: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.

**Table 10. Programming Mode AC Characteristics (1)**
($T_A$ = 25 °C; $V_{CC}$ = 6V ± 0.25V; $V_{PP}$ = 12.5V ± 0.25V)

| Symbol | Alt | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{AVPL}$ | $t_{AS}$ | Address Valid to Program Low | | 2 | | µs |
| $t_{QVPL}$ | $t_{DS}$ | Input Valid to Program Low | | 2 | | µs |
| $t_{VPHPL}$ | $t_{VPS}$ | $V_{PP}$ High to Program Low | | 2 | | µs |
| $t_{VCHPL}$ | $t_{VCS}$ | $V_{CC}$ High to Program Low | | 2 | | µs |
| $t_{ELPL}$ | $t_{CES}$ | Chip Enable Low to Program Low | | 2 | | µs |
| $t_{PLPH}$ | $t_{PW}$ | Program Pulse Width (Initial) | | 0.95 | 1.05 | ms |
| | | Program Pulse Width (Over Program) | | 2.85 | 78.75 | ms |
| $t_{PHQX}$ | $t_{DH}$ | Program High to Input Transition | | 2 | | µs |
| $t_{QXGL}$ | $t_{OES}$ | Input Transition to Output Enable Low | | 2 | | µs |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | | | 100 | ns |
| $t_{GHQZ}$ (2) | $t_{DFP}$ | Output Enable High to Output Hi-Z | | 0 | 130 | ns |
| $t_{GHAX}$ | $t_{AH}$ | Output Enable High to Address Transition | | 0 | | ns |

Note: 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Sampled only, not 100% tested.

## Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C64A are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C64A is in the programming mode when $V_{PP}$ input is at 12.5V, $\overline{E}$ is at $V_{IL}$ and $\overline{P}$ is pulsed to $V_{IL}$. The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. $V_{CC}$ is specified to be 6V ± 0.25V.

**Figure 6. Programming and Verify Modes AC Waveforms**

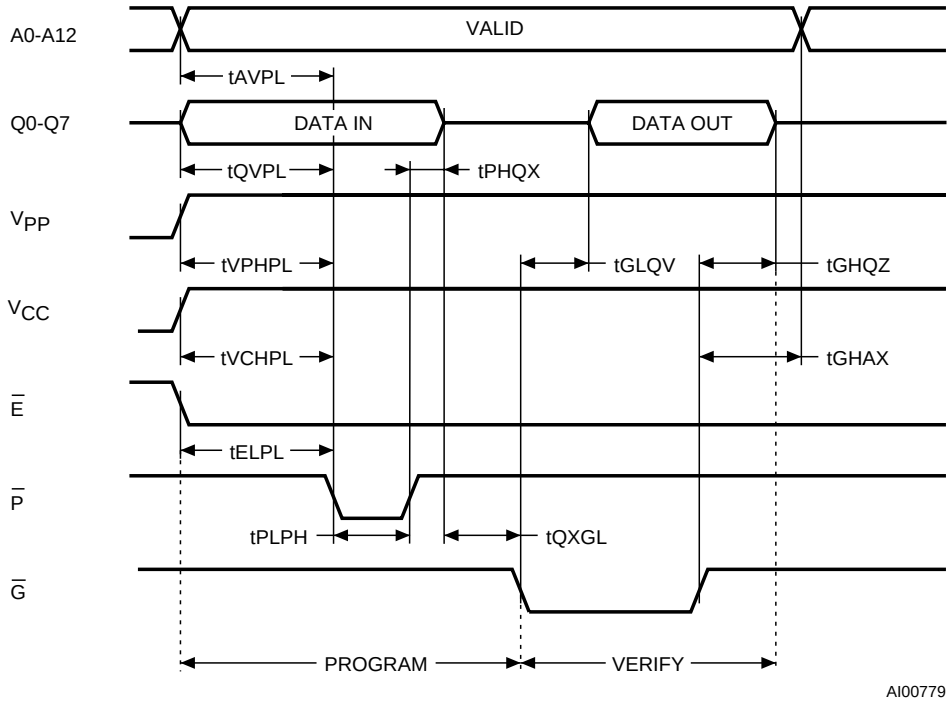
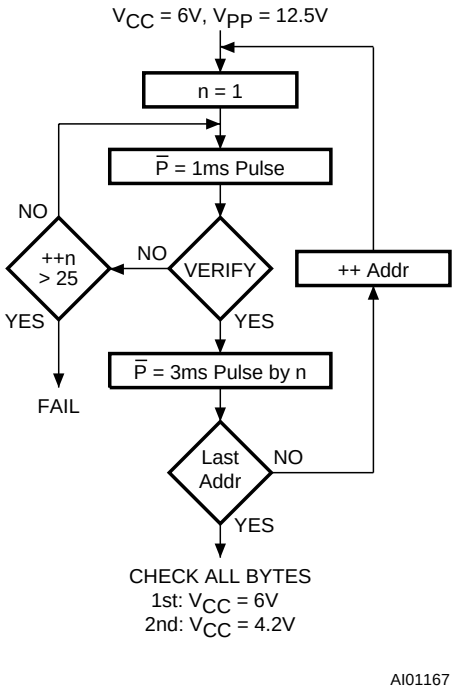



**Figure 7. Programming Flowchart**




### High Speed Programming

The high speed programming algorithm, described in the flowchart, rapidly programs the M27C64A using an efficient and reliable method, particularly suited to the production programming environment. An individual device will take around 1 minute to program.

### Program Inhibit

Programming of multiple M27C64A in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27C64A may be common. A TTL low level pulse applied to a M27C64A $\overline{P}$ input, with $\overline{E}$ low and $V_{PP}$ at 12.5V, will program that M27C64A. A high level $\overline{E}$ input inhibits the other M27C64A from being programmed.

### Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{E}$ and $\overline{G}$ at $V_{IL}$, $\overline{P}$ at $V_{IH}$, $V_{PP}$ at 12.5V and $V_{CC}$ at 6V.

### Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C64A. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C64A, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from $V_{IL}$ to $V_{IH}$. All other address lines must be held at $V_{IL}$ during Electronic Signature mode.

Byte 0 (A0 = $V_{IL}$) represents the manufacturer code and byte 1 (A0=$V_{IH}$) the device identifier code. For the STMicroelectronics M27C64A, these two identifier bytes are given in Table 4 and can be read-out on outputs Q7 to Q0.

### ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C64A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C64A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C64A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C64A window to prevent unintentional erasure. The recommended erasure procedure for the M27C64A is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm$^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm$^2$ power rating. The M27C64A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

**Table 11. Ordering Information Scheme**

Example: M27C64A -15 C 1 TR

**Device Type**
M27

**Supply Voltage**
C = 5V ±10%

**Device Function**
64A = 64 Kbit (8Kb x8)

**Speed**
-15 = 150 ns
-20 = 200 ns
-25 = 250 ns
-30 = 300 ns

**Package**
F = FDIP28W
C = PLCC32

**Temperature Range**
1 = 0 to 70 °C
6 = –40 to 85 °C

**Options**
X = Additional Burn-in
TR = Tape & Reel Packing

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

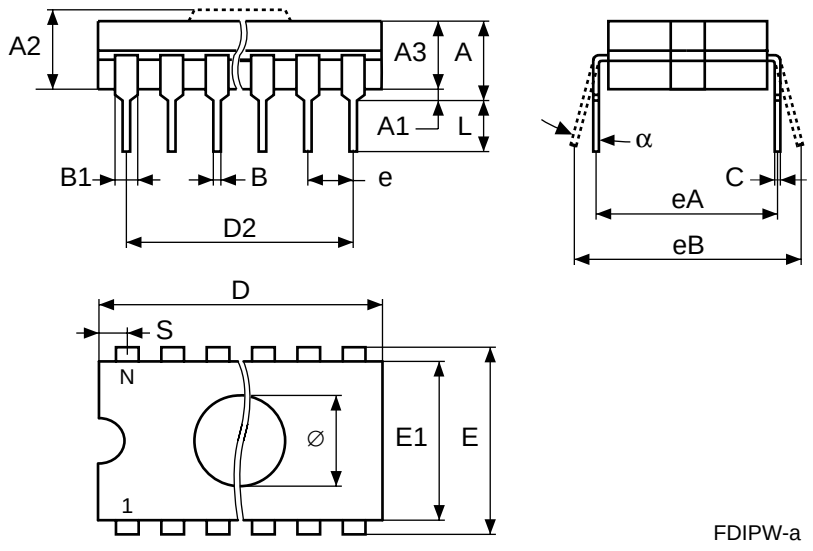
**Table 12. Revision History**

| Date | Revision Details |
|---|---|
| March 1998 | First Issue |
| 09/25/00 | AN620 Reference removed |

**Table 13. FDIP28W - 28 pin Ceramic Frit-seal DIP, with window, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 5.72 | | | 0.225 |
| A1 | | 0.51 | 1.40 | | 0.020 | 0.055 |
| A2 | | 3.91 | 4.57 | | 0.154 | 0.180 |
| A3 | | 3.89 | 4.50 | | 0.153 | 0.177 |
| B | | 0.41 | 0.56 | | 0.016 | 0.022 |
| B1 | 1.45 | – | – | 0.057 | – | – |
| C | | 0.23 | 0.30 | | 0.009 | 0.012 |
| D | | 36.50 | 37.34 | | 1.437 | 1.470 |
| D2 | 33.02 | – | – | 1.300 | – | – |
| E | 15.24 | – | – | 0.600 | – | – |
| E1 | | 13.06 | 13.36 | | 0.514 | 0.526 |
| e | 2.54 | – | – | 0.100 | – | – |
| eA | 14.99 | – | – | 0.590 | – | – |
| eB | | 16.18 | 18.03 | | 0.637 | 0.710 |
| L | | 3.18 | | | 0.125 | |
| S | | 1.52 | 2.49 | | 0.060 | 0.098 |
| ∅ | 7.11 | – | – | 0.280 | – | – |
| α | | 4° | 11° | | 4° | 11° |
| N | 28 | | | 28 | | |

**Figure 8. FDIP28W - 28 pin Ceramic Frit-seal DIP, with window, Package Outline**

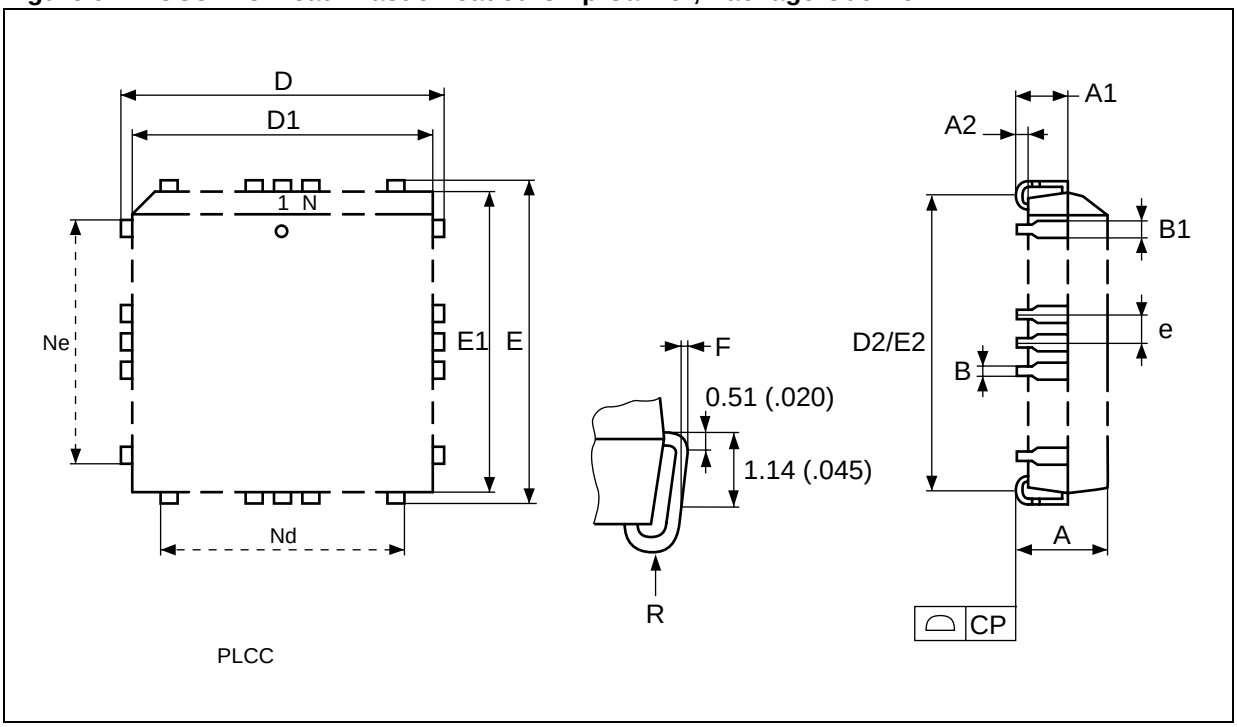



Drawing is not to scale.

**Table 14. PLCC32 - 32 lead Plastic Leaded Chip Carrier, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 2.54 | 3.56 | | 0.100 | 0.140 |
| A1 | | 1.52 | 2.41 | | 0.060 | 0.095 |
| A2 | | 0.38 | | | 0.015 | |
| B | | 0.33 | 0.53 | | 0.013 | 0.021 |
| B1 | | 0.66 | 0.81 | | 0.026 | 0.032 |
| D | | 12.32 | 12.57 | | 0.485 | 0.495 |
| D1 | | 11.35 | 11.56 | | 0.447 | 0.455 |
| D2 | | 9.91 | 10.92 | | 0.390 | 0.430 |
| e | 1.27 | | | 0.050 | | |
| E | | 14.86 | 15.11 | | 0.585 | 0.595 |
| E1 | | 13.89 | 14.10 | | 0.547 | 0.555 |
| E2 | | 12.45 | 13.46 | | 0.490 | 0.530 |
| F | | 0.00 | 0.25 | | 0.000 | 0.010 |
| R | 0.89 | | | 0.035 | | |
| N | 32 | | | 32 | | |
| Nd | 7 | | | 7 | | |
| Ne | 9 | | | 9 | | |
| CP | | | 0.10 | | | 0.004 |

**Figure 9. PLCC32 - 32 lead Plastic Leaded Chip Carrier, Package Outline**




Drawing is not to scale.