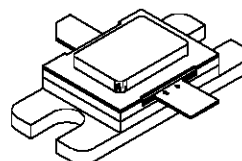


RF & MICROWAVE TRANSISTORS AVIONICS APPLICATIONS

- DESIGNED FOR HIGH POWER PULSED IFF APPLICATIONS
- 450 WATTS (min.) IFF 1030/1090 MHz
- 7.0 dB MIN. GAIN
- REFRACTORY GOLD METALLIZATION
- BALLASTING AND LOW THERMAL RESISTANCE FOR RELIABILITY AND RUGGEDNESS
- 30:1 LOAD VSWR CAPABILITY AT SPECIFIED OPERATING CONDITIONS
- INPUT MATCHED, COMMON BASE CONFIGURATION



.400 x .500 2LFL (M112)
hermetically sealed

ORDER CODE

SD1541-09

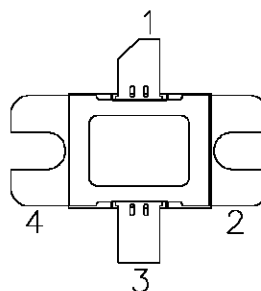
BRANDING

1541-9

DESCRIPTION

The SD1541-09 is a gold metallized silicon NPN planar transistor. The SD1541-09 is designed for applications requiring high peak and low duty cycles such as IFF. The SD1541-09 is packaged in a metal/ceramic package with internal input matching, resulting in improved broadband performance and a low thermal resistance.

PIN CONNECTION



1. Collector

2. Base

3. Emitter

4. Base

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$)

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	65	V
V_{CEO}	Collector-Emitter Voltage	65	V
V_{EBO}	Emitter-Base Voltage	3.5	V
I_C	Device Current	22	A
P_{DISS}	Power Dissipation	1458	W
T_J	Junction Temperature	+200	$^{\circ}C$
T_{STG}	Storage Temperature	- 65 to +150	$^{\circ}C$

THERMAL DATA

$R_{TH(j-c)}$	Junction-Case Thermal Resistance	0.12	$^{\circ}C/W$
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SD1541-09

ELECTRICAL SPECIFICATIONS ($T_{\text{case}} = 25^{\circ}\text{C}$)

STATIC

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
BV_{CBO}	$I_C = 25\text{mA}$ $I_E = 0\text{mA}$	65	—	—	V
BV_{CES}	$I_C = 50\text{mA}$ $I_B = 0\text{mA}$	65	—	—	V
BV_{EBO}	$I_E = 10\text{mA}$ $I_C = 0\text{mA}$	3.5	—	—	V
I_{CES}	$V_{CE} = 50\text{V}$ $I_E = 0\text{mA}$	—	—	25	mA
h_{FE}	$V_{CE} = 5\text{V}$ $I_C = .25\text{A}$	5	—	200	—

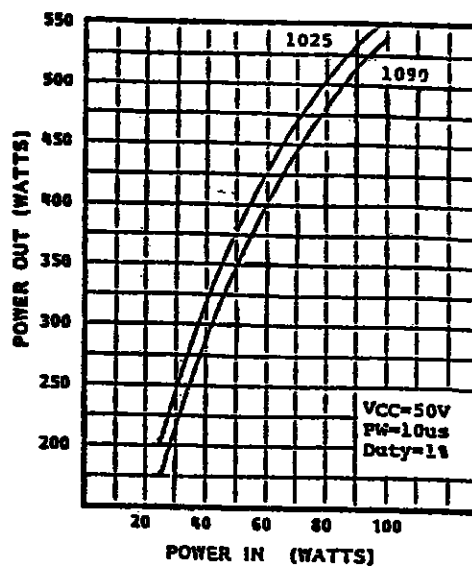
DYNAMIC

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
P_{OUT}	$f = 1090\text{ MHz}$ $P_{IN} = 90\text{ W}$ $V_{CE} = 50\text{ V}$	450	—	—	W
G_P	$f = 1090\text{ MHz}$ $P_{IN} = 90\text{ W}$ $V_{CE} = 50\text{ V}$	7.0	—	—	dB

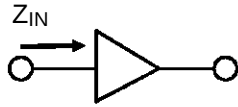
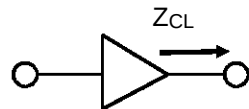
Note: Pulse Width = $10\mu\text{Sec}$, Duty Cycle = 1%

TYPICAL PERFORMANCE

POWER OUTPUT vs POWER INPUT

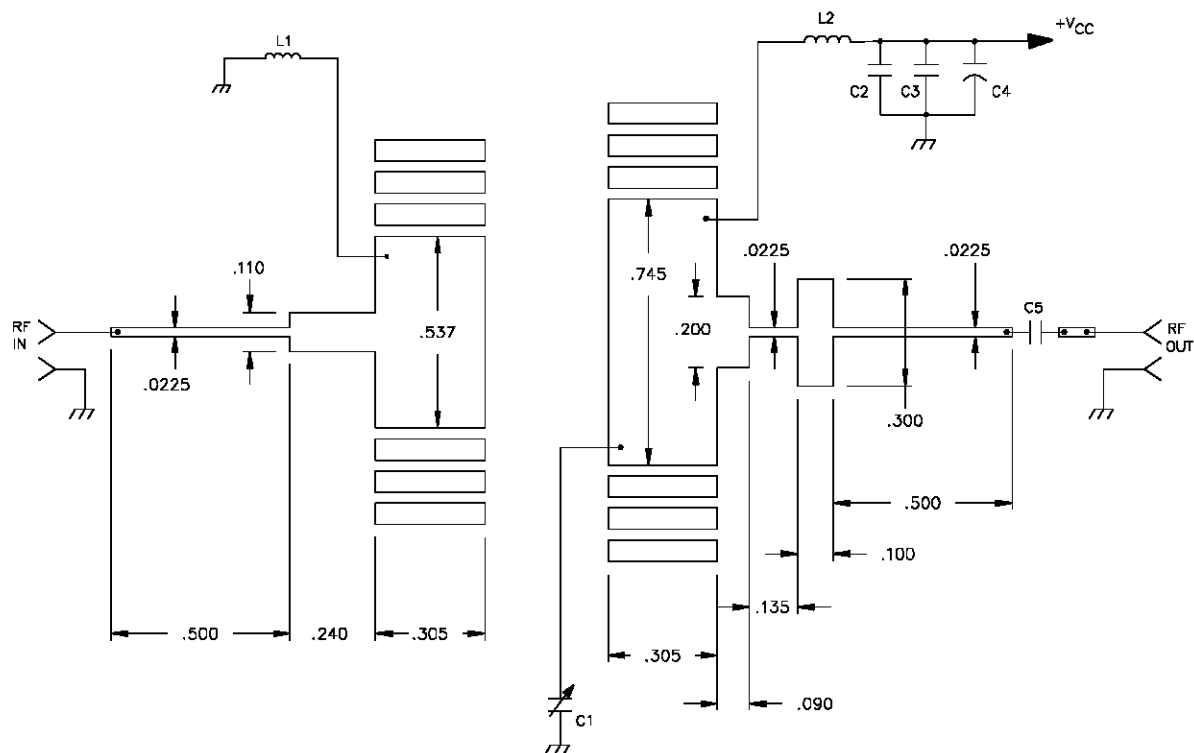


IMPEDANCE DATA

TYPICAL INPUT
IMPEDANCETYPICAL COLLECTOR
LOAD IMPEDANCE

FREQ.	$Z_{IN} (\Omega)$	$Z_{CL} (\Omega)$
1030 MHz	$1.6 + j 5.1$	$1.1 - j 2.0$
1090 MHz	$2.5 + j 4.7$	$1.2 - j 1.2$

TEST CIRCUIT LAYOUT



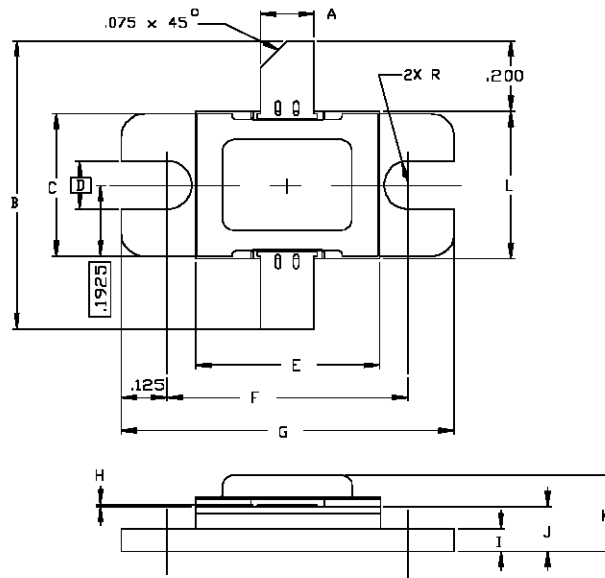
- C1 : .4 - 2.5pF Johanson Gigatrim
 C2 : 100pF Chip Capacitor
 C3 : .01μF CK05BX103K
 C4 : 1000μF Electrolytic 63V
 C5 : 100pF Chip Capacitor

- L1 : 1/2 Turn .026" Diameter Wire
 Loop = .170" Width x .320" Height
 L2 : 1 Turn .026" Diameter Wire I.D. .130"

All Dimensions are in Inches
 Board Er = 10.2, Height .025"

PACKAGE MECHANICAL DATA

Ref.: Dwg. No.12-0112



SGS-THOMSON MICROELECTRONICS		
	MINIMUM Inches/mm	MAXIMUM Inches/mm
A	.145/3,68	.155/3,93
B	.750/19,05	
C	.380/9,65	.390/9,91
D	.130/3,30	
E	.495/12,57	.507/12,88
F	.640/16,26	.655/16,64
G	.890/22,61	.910/23,11
H	.002/0,05	.006/0,15
I	.055/1,40	.065/1,65
J	.115/2,92	.135/3,43
K		.230/5,84
L	.395/10,03	.407/10,34

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