



# STB5NB80

## N - CHANNEL 800V - 1.8Ω - 5A - D<sup>2</sup>PAK PowerMESH™ MOSFET

| TYPE     | V <sub>DSS</sub> | R <sub>DS(on)</sub> | I <sub>D</sub> |
|----------|------------------|---------------------|----------------|
| STB5NB80 | 800 V            | < 2.2 Ω             | 5 A            |

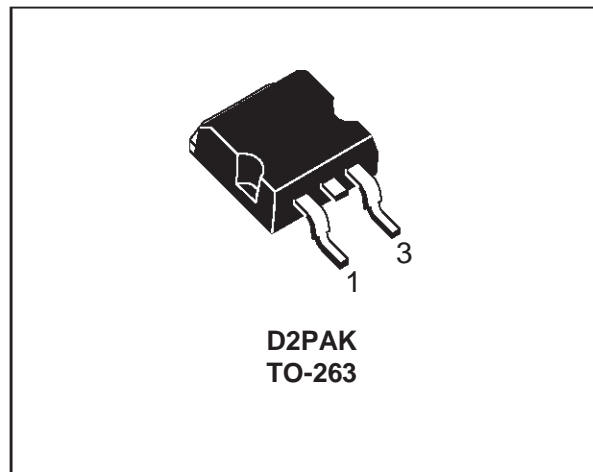
- TYPICAL R<sub>DS(on)</sub> = 1.8 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

### DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R<sub>DS(on)</sub> per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- DC-AC CONVERTERS FOR WELDING
- EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE



### ABSOLUTE MAXIMUM RATINGS

| Symbol              | Parameter   | Value      | Unit |
|---------------------|---|------------|------|
| V <sub>DS</sub>     | Drain-source Voltage (V <sub>GS</sub> = 0)            | 800        | V    |
| V <sub>DGR</sub>    | Drain- gate Voltage (R <sub>GS</sub> = 20 kΩ)         | 800        | V    |
| V <sub>GS</sub>     | Gate-source Voltage                                   | ± 30       | V    |
| I <sub>D</sub>      | Drain Current (continuous) at T <sub>c</sub> = 25 °C  | 5          | A    |
| I <sub>D</sub>      | Drain Current (continuous) at T <sub>c</sub> = 100 °C | 3.2        | A    |
| I <sub>DM</sub> (•) | Drain Current (pulsed)                                | 20         | A    |
| P <sub>tot</sub>    | Total Dissipation at T <sub>c</sub> = 25 °C           | 110        | W    |
|                     | Derating Factor                                       | 0.88       | W/°C |
| dv/dt(1)            | Peak Diode Recovery voltage slope                     | 4          | V/ns |
| T <sub>stg</sub>    | Storage Temperature                                   | -65 to 150 | °C   |
| T <sub>j</sub>      | Max. Operating Junction Temperature                   | 150        | °C   |

(\*) Limited only by maximum temperature allowed

(1) I<sub>sd</sub> ≤ 5A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

## STB5NB80

### THERMAL DATA

|                       |  |     |      |      |
|-----------------------|--|-----|------|------|
| R <sub>thj-case</sub> | Thermal Resistance Junction-case               | Max | 1.13 | °C/W |
| R <sub>thj-amb</sub>  | Thermal Resistance Junction-ambient            | Max | 62.5 | °C/W |
| R <sub>thc-sink</sub> | Thermal Resistance Case-sink                   | Typ | 0.5  | °C/W |
| T <sub>l</sub>        | Maximum Lead Temperature For Soldering Purpose |     | 300  | °C   |

### AVALANCHE CHARACTERISTICS

| Symbol          | Parameter  | Min. Value | Max. Value | Unit |
|-----------------|--|------------|------------|------|
| I <sub>AR</sub> | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)                                |            | 5          | A    |
| E <sub>AS</sub> | Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V) |            | 300        | mJ   |

### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

OFF

| Symbol               | Parameter   | Test Conditions  | Min. | Typ. | Max.    | Unit     |
|----------------------|---|--|------|------|---------|----------|
| V <sub>(BR)DSS</sub> | Drain-source Breakdown Voltage                        | I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0  | 800  |      |         | V        |
| I <sub>DSS</sub>     | Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0) | V <sub>DS</sub> = Max Rating<br>V <sub>DS</sub> = Max Rating T <sub>c</sub> = 125 °C |      |      | 1<br>50 | μA<br>μA |
| I <sub>GSS</sub>     | Gate-body Leakage Current (V <sub>DS</sub> = 0)       | V <sub>GS</sub> = ± 30 V   |      |      | ± 100   | nA       |

ON (\*)

| Symbol              | Parameter                         | Test Conditions   | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------------|---|------|------|------|------|
| V <sub>GS(th)</sub> | Gate Threshold Voltage            | V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA                               | 3    | 4    | 5    | V    |
| R <sub>DS(on)</sub> | Static Drain-source On Resistance | V <sub>GS</sub> = 10V I <sub>D</sub> = 2.5 A  |      | 1.8  | 2.2  | Ω    |
| I <sub>D(on)</sub>  | On State Drain Current            | V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub><br>V <sub>GS</sub> = 10 V | 5    |      |      | A    |

### DYNAMIC

| Symbol              | Parameter                    | Test Conditions  | Min. | Typ. | Max. | Unit |
|---------------------|------------------------------|--|------|------|------|------|
| g <sub>fs</sub> (*) | Forward Transconductance     | V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> I <sub>D</sub> = 2.5 A | 1.5  | 4    |      | S    |
| C <sub>iss</sub>    | Input Capacitance            | V <sub>DS</sub> = 25 V f = 1 MHz V <sub>GS</sub> = 0                                 |      | 1050 |      | pF   |
| C <sub>oss</sub>    | Output Capacitance           |  |      | 135  |      | pF   |
| C <sub>rss</sub>    | Reverse Transfer Capacitance |  |      |      | 15   |      |

**ELECTRICAL CHARACTERISTICS** (continued)

**SWITCHING ON**

| Symbol      | Parameter          | Test Conditions  | Min. | Typ. | Max. | Unit |
|-------------|--------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay Time | $V_{DD} = 400\text{ V}$ $I_D = 3\text{ A}$                                 |      | 18   |      | ns   |
| $t_r$       | Rise Time          | $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$<br>(see test circuit, figure 3) |      | 9    |      | ns   |
| $Q_g$       | Total Gate Charge  | $V_{DD} = 480\text{ V}$ $I_D = 5.6\text{ A}$ $V_{GS} = 10\text{ V}$        |      | 30   | 42   | nC   |
| $Q_{gs}$    | Gate-Source Charge |  |      | 9    |      | nC   |
| $Q_{gd}$    | Gate-Drain Charge  |  |      | 14   |      | nC   |

**SWITCHING OFF**

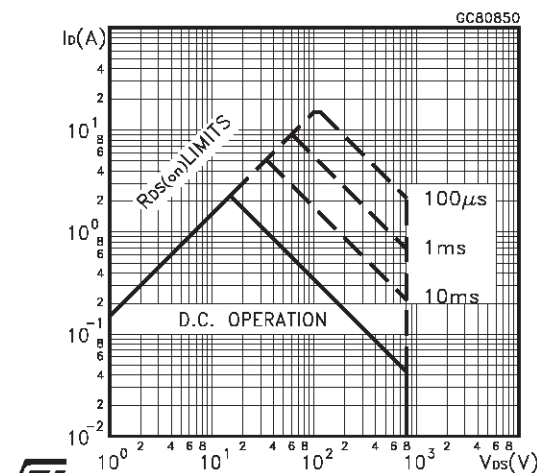
| Symbol        | Parameter             | Test Conditions  | Min. | Typ. | Max. | Unit |
|---------------|-----------------------|--|------|------|------|------|
| $t_{r(Voff)}$ | Off-voltage Rise Time | $V_{DD} = 640\text{ V}$ $I_D = 5.6\text{ A}$                               |      | 14   |      | ns   |
| $t_f$         | Fall Time             | $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$<br>(see test circuit, figure 5) |      | 14   |      | ns   |
| $t_c$         | Cross-over Time       |  |      | 21   |      | ns   |

**SOURCE DRAIN DIODE**

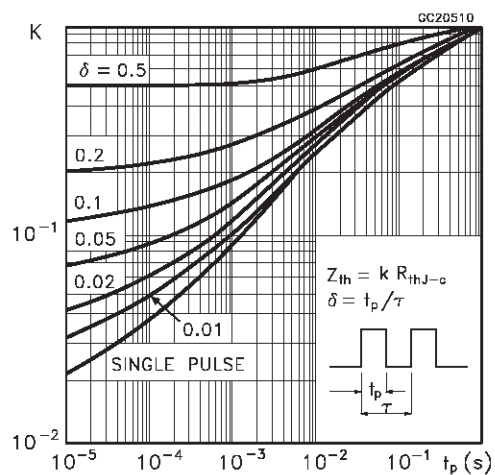
| Symbol             | Parameter                     | Test Conditions   | Min. | Typ. | Max. | Unit          |
|--------------------|-------------------------------|---|------|------|------|---------------|
| $I_{SD}$           | Source-drain Current          |   |      |      | 5    | A             |
| $I_{SDM}(\bullet)$ | Source-drain Current (pulsed) |   |      |      | 20   | A             |
| $V_{SD}(\ast)$     | Forward On Voltage            | $I_{SD} = 5\text{ A}$ $V_{GS} = 0$  |      |      | 1.6  | V             |
| $t_{rr}$           | Reverse Recovery Time         | $I_{SD} = 5.6\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$<br>$V_{DD} = 100\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$<br>(see test circuit, figure 5) |      | 700  |      | ns            |
| $Q_{rr}$           | Reverse Recovery Charge       |   |      | 5    |      | $\mu\text{C}$ |
| $I_{RRM}$          | Reverse Recovery Current      |   |      | 14   |      | A             |

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %  
 (•) Pulse width limited by safe operating area

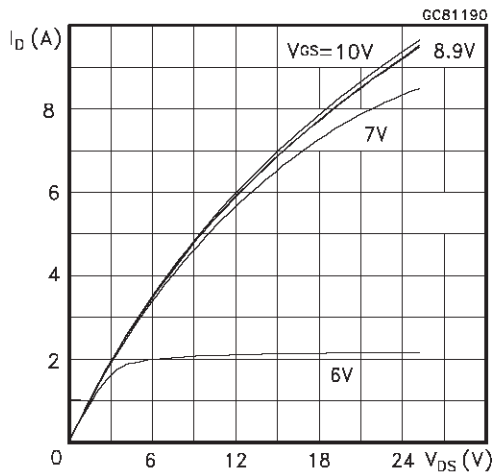
**Safe Operating Area**



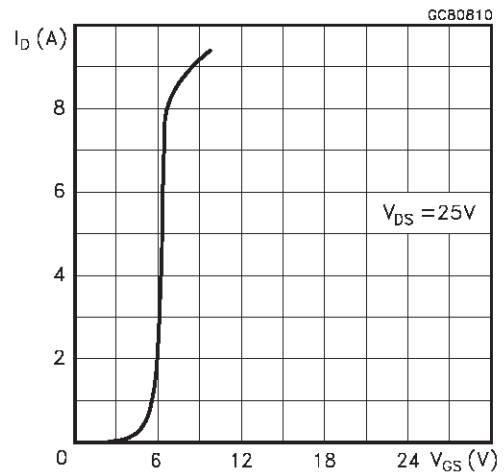
**Thermal Impedance**



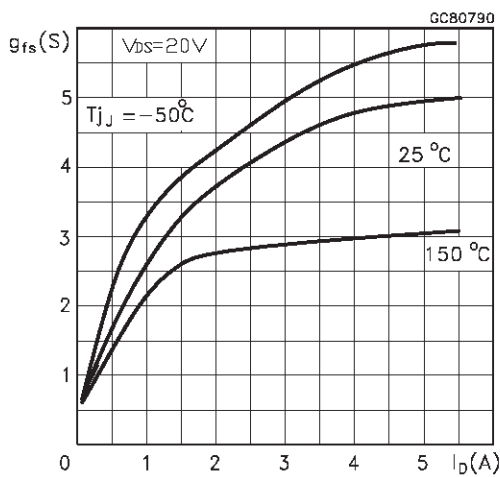
Output Characteristics



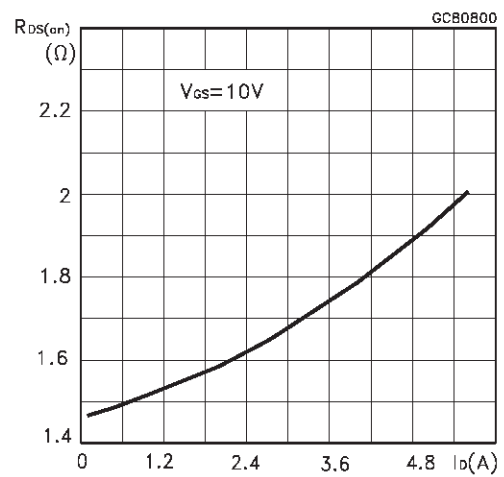
Transfer Characteristics



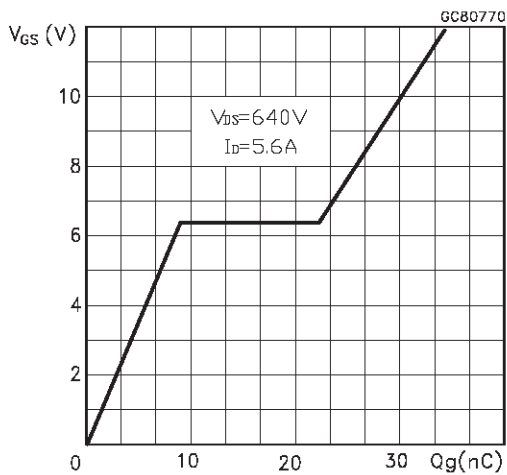
Transconductance



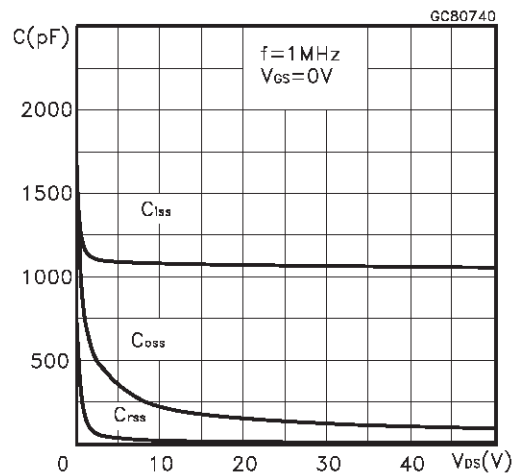
Static Drain-source On Resistance



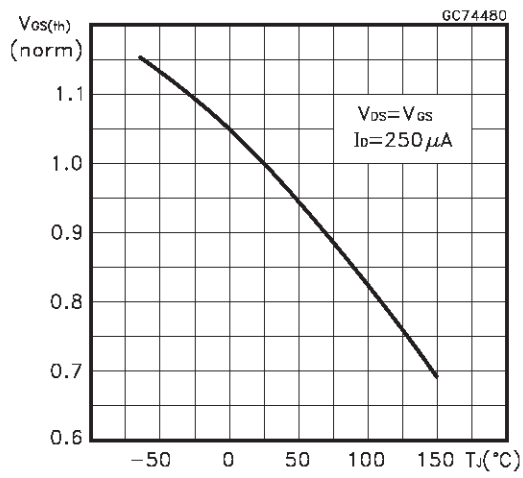
Gate Charge vs Gate-source Voltage



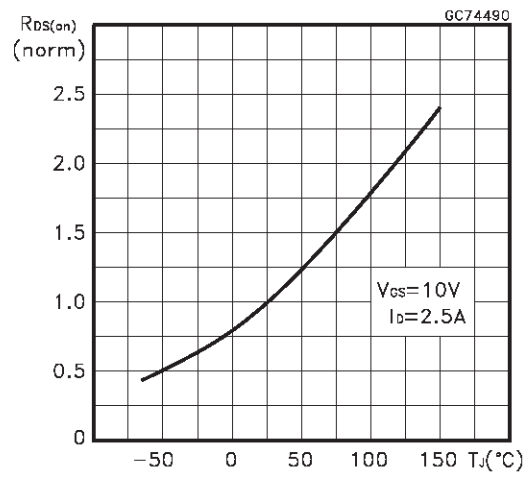
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

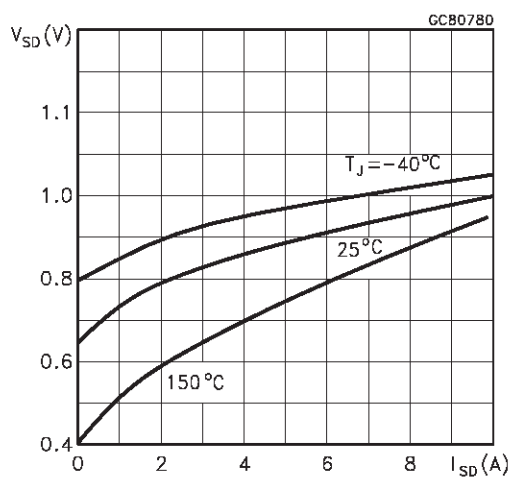


Fig. 1: Unclamped Inductive Load Test Circuit

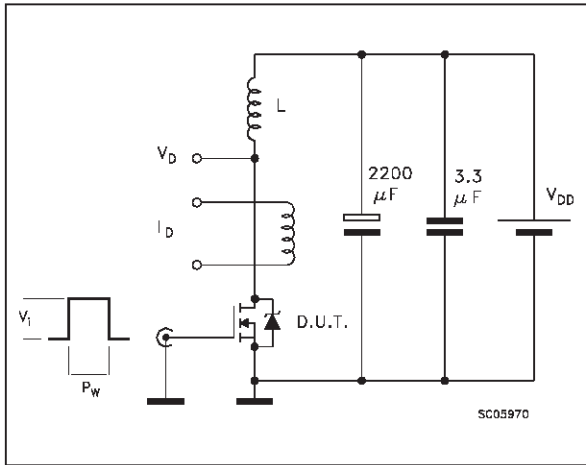


Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuits For Resistive Load

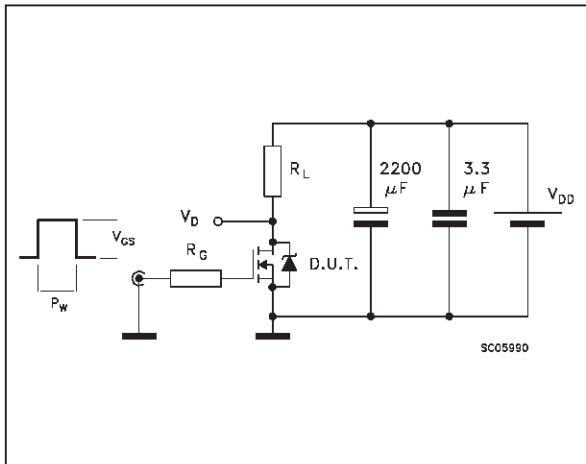


Fig. 4: Gate Charge test Circuit

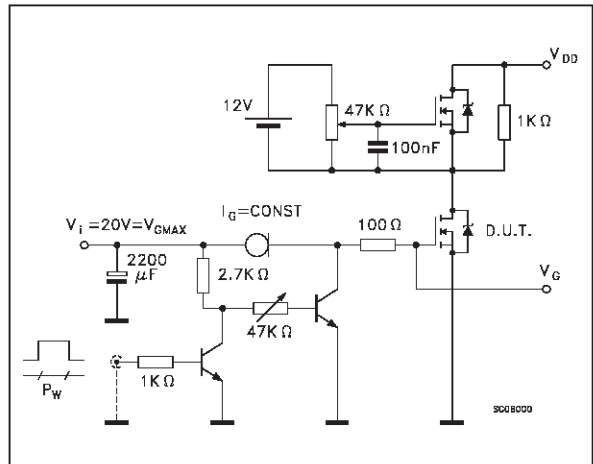
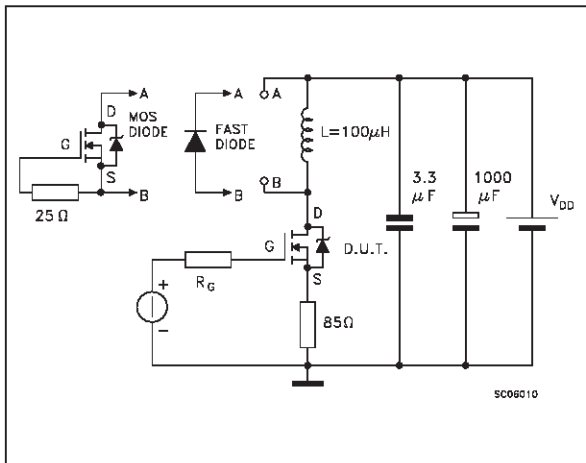
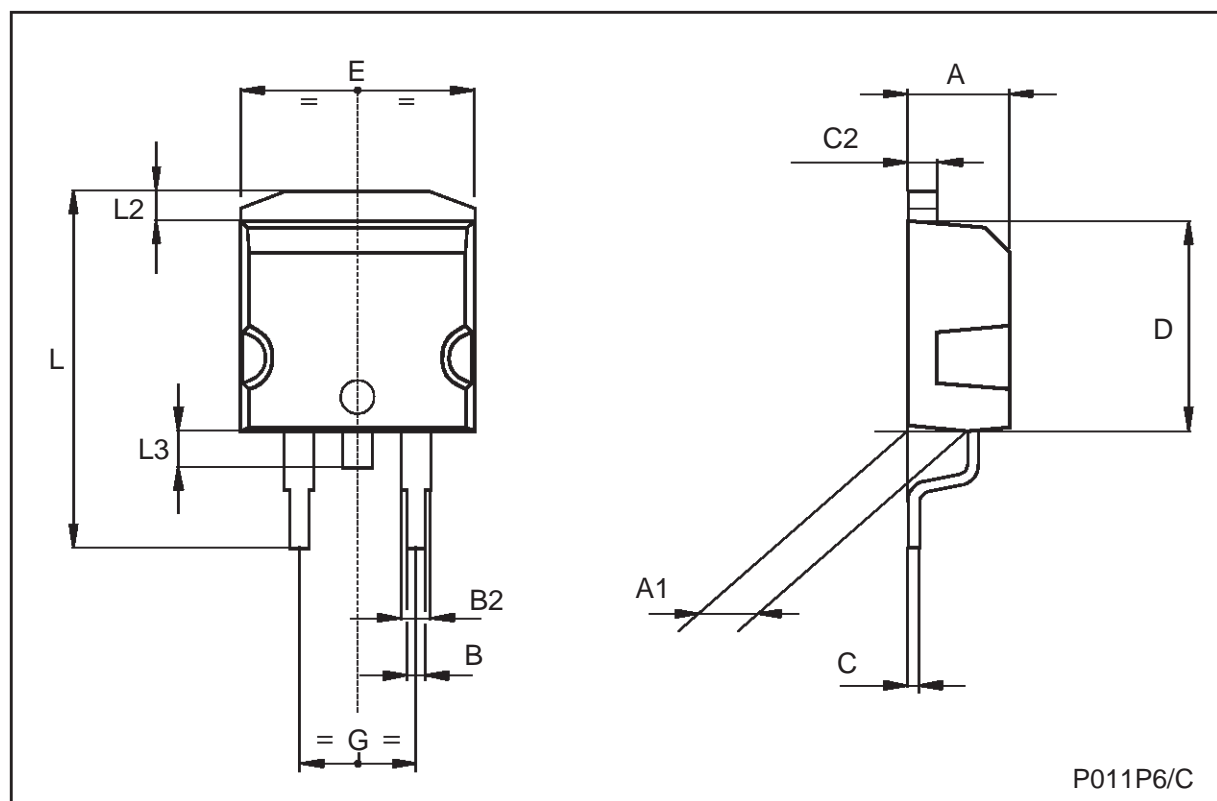


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-263 (D<sup>2</sup>PAK) MECHANICAL DATA

| DIM. | mm   |      |       | inch  |      |       |
|------|------|------|-------|-------|------|-------|
|      | MIN. | TYP. | MAX.  | MIN.  | TYP. | MAX.  |
| A    | 4.3  |      | 4.6   | 0.169 |      | 0.181 |
| A1   | 2.49 |      | 2.69  | 0.098 |      | 0.106 |
| B    | 0.7  |      | 0.93  | 0.027 |      | 0.036 |
| B2   | 1.25 |      | 1.4   | 0.049 |      | 0.055 |
| C    | 0.45 |      | 0.6   | 0.017 |      | 0.023 |
| C2   | 1.21 |      | 1.36  | 0.047 |      | 0.053 |
| D    | 8.95 |      | 9.35  | 0.352 |      | 0.368 |
| E    | 10   |      | 10.28 | 0.393 |      | 0.404 |
| G    | 4.88 |      | 5.28  | 0.192 |      | 0.208 |
| L    | 15   |      | 15.85 | 0.590 |      | 0.624 |
| L2   | 1.27 |      | 1.4   | 0.050 |      | 0.055 |
| L3   | 1.4  |      | 1.75  | 0.055 |      | 0.068 |



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