



STP8NC70Z - STP8NC70ZFP STB8NC70Z-1

N-CHANNEL 700V - 0.90Ω - 6.8A TO-220/TO-220FP/I²PAK
Zener-Protected PowerMESH™ III MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP8NC70Z/FP	700V	< 1.2 Ω	6.8 A
STB8NC70Z-1	700V	< 1.2 Ω	6.8 A

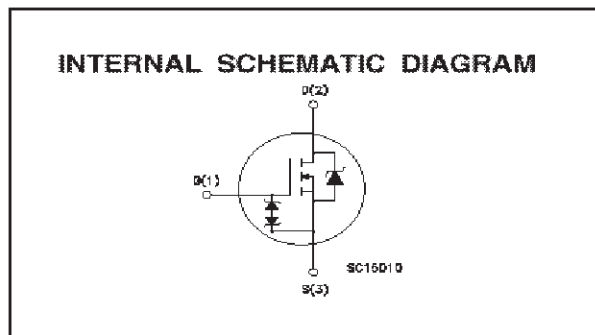
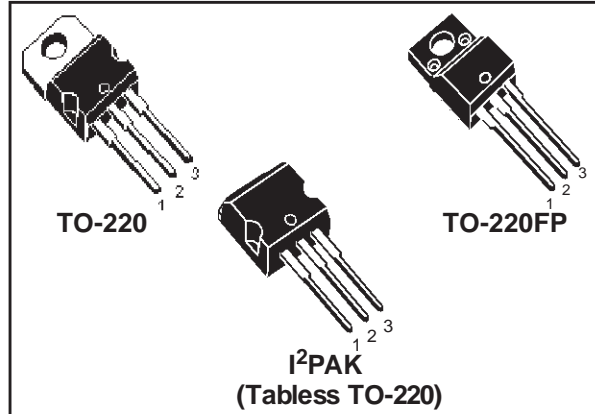
- TYPICAL R_{DS(on)} = 0.9 Ω
- EXTREMELY HIGH dv/dt AND CAPABILITY
GATE-TO- SOURCE ZENER DIODES
- 100% AVALANCHE TESTED
- VERY LOW GATE INPUT RESISTANCE
- GATE CHARGE MINIMIZED

DESCRIPTION

The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications.

APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS,
COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP(B)8NC70Z(-1)	STP8NC70ZFP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	700		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	700		V
V _{GS}	Gate- source Voltage	± 25		V
I _D	Drain Current (continuous) at T _C = 25°C	6.8	6.8(*)	A
I _D	Drain Current (continuous) at T _C = 100°C	4.3	4.3(*)	A
I _{DM} (●)	Drain Current (pulsed)	27	27(*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	135	40	W
	Derating Factor	1.08	0.32	W/°C
I _{GS}	Gate-source Current (DC)	±50		mA
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=15KΩ)	3		KV
dv/dt(1)	Peak Diode Recovery voltage slope	3		V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	--	2000	V
T _{stg}	Storage Temperature	-65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(●)Pulse width limited by safe operating area

(1)I_{SD} ≤ 6.8A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

(*)Pulse width Limited by maximum temperature allowed 1/11

March 2001

STP8NC70Z/FP/STB8NC70Z-1

THERMAL DATA

		TO-220 / I ² PAK	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	0.93	3.13	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	0.1		°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	6.8	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	354	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	700			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = 1 mA, V _{GS} = 0		0.8		V/°C
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±10	μA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 3.75 A		0.90	1.2	Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{DS(on)max} , V _{GS} = 10V	6.8			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 3.75A		6		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2350		pF
C _{oss}	Output Capacitance			180		pF
C _{rss}	Reverse Transfer Capacitance			22		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 350\text{ V}$, $I_D = 37.5\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		30		ns
t_r	Rise Time			10		ns
Q_g	Total Gate Charge	$V_{DD} = 560\text{ V}$, $I_D = 7.5\text{ A}$, $V_{GS} = 10\text{ V}$		55	77	nC
Q_{gs}	Gate-Source Charge			14		nC
Q_{gd}	Gate-Drain Charge			21		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 560\text{ V}$, $I_D = 7.5\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 5)		15		ns
t_f	Fall Time			12		ns
t_c	Cross-over Time			20		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				6.8	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				27	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 6.8\text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 7.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 30\text{ V}$, $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		680		ns
Q_{rr}	Reverse Recovery Charge			7.1		μC
I_{RRM}	Reverse Recovery Current			21		A

GATE-SOURCE ZENER DIODE

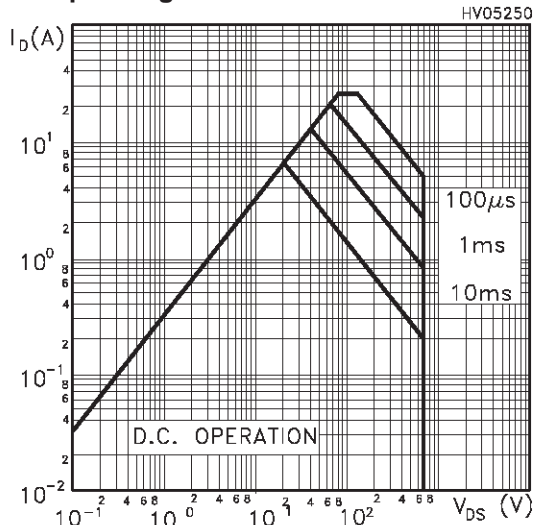
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{ mA}$ (Open Drain)	25			V
α_T	Voltage Thermal Coefficient	$T = 25^\circ\text{C}$ Note(3)		1.3		$10^{-4}/^\circ\text{C}$
R_z	Dynamic Resistance	$I_D = 50\text{ mA}$,		90		Ω

- Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.
 3. $\Delta V_{BV} = \alpha_T (25^\circ - T) BV_{GSO}(25^\circ)$

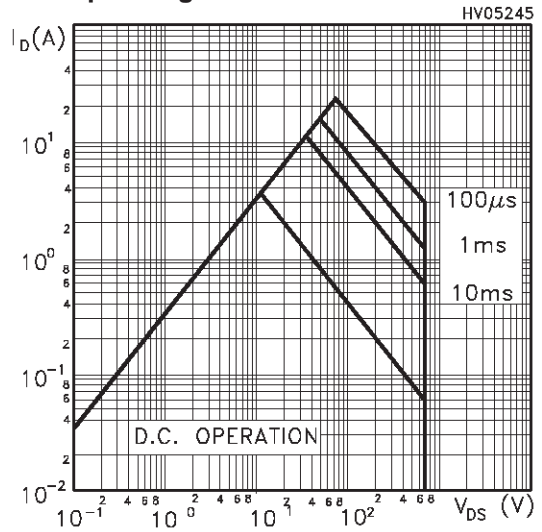
PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the 25V Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

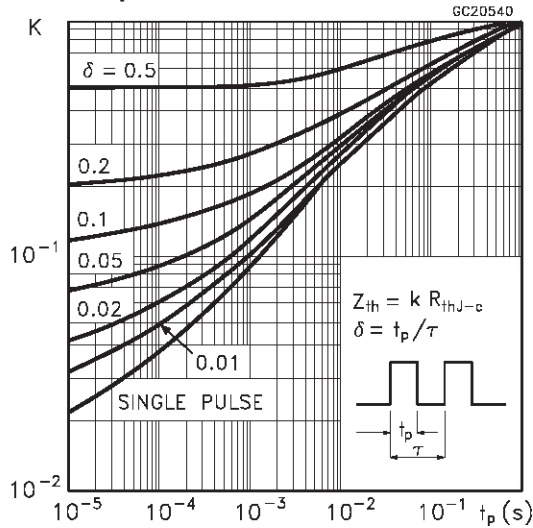
Safe Operating Area For TO-220 / I PAK



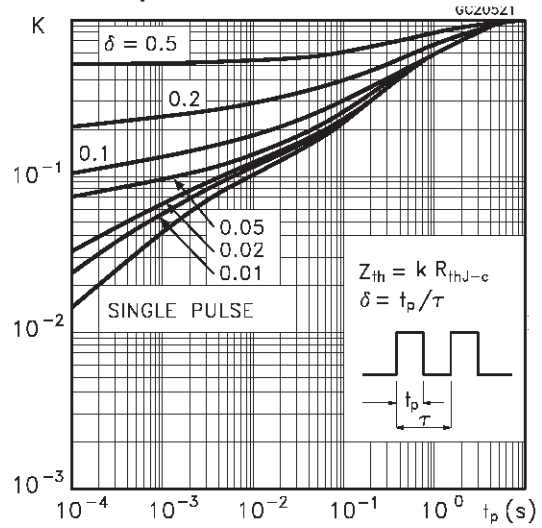
Safe Operating Area For TO-220FP



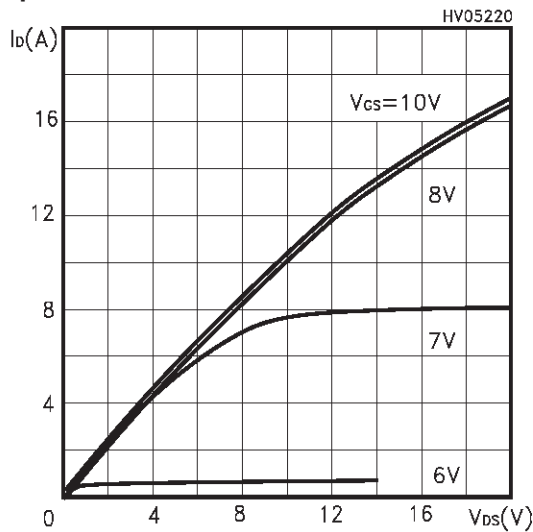
Thermal Impedance For TO-220 / I PAK



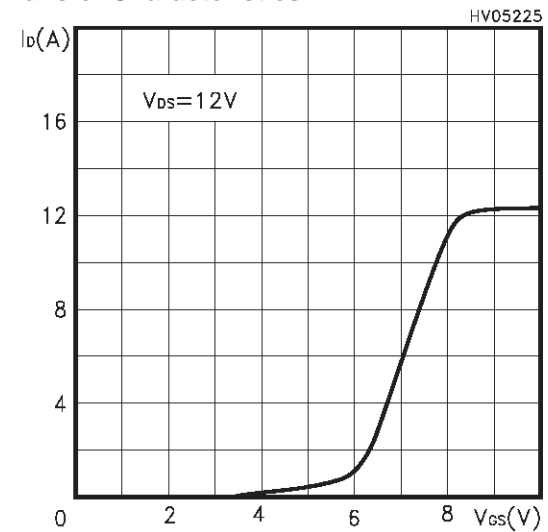
Thermal Impedance For TO-220FP



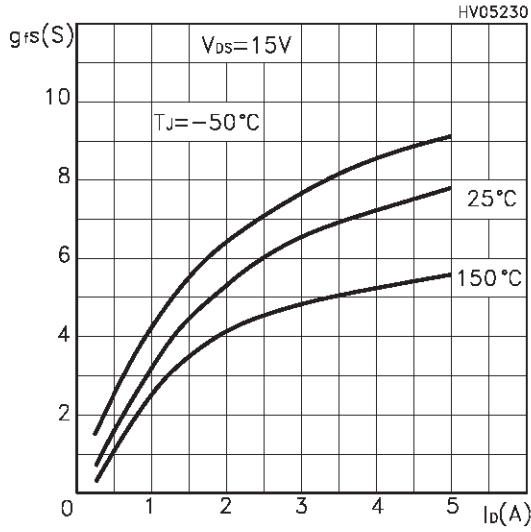
Output Characteristics



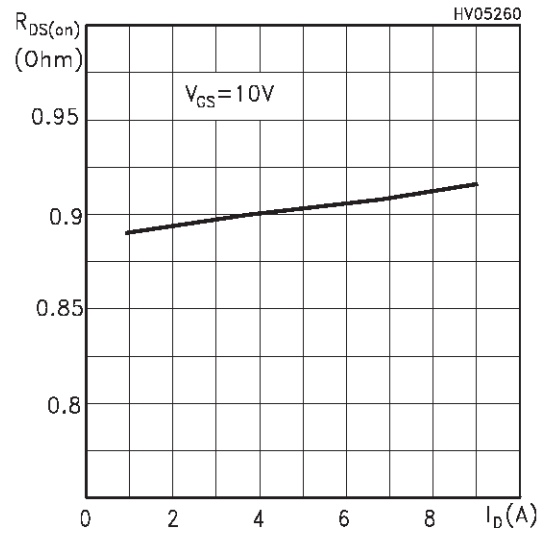
Transfer Characteristics



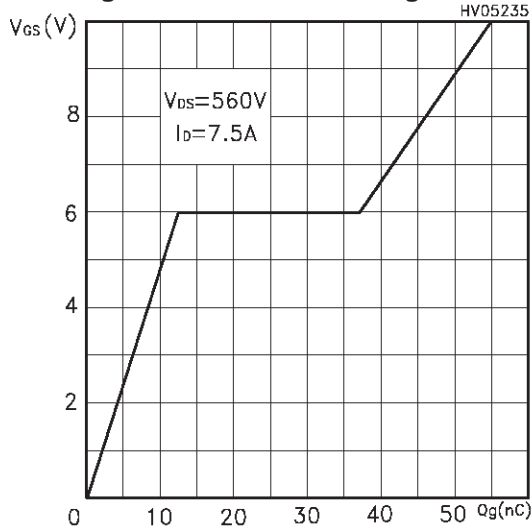
Transconductance



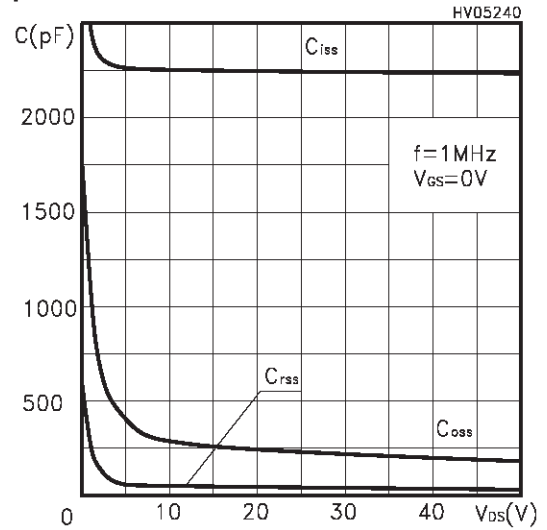
Static Drain-source On Resistance



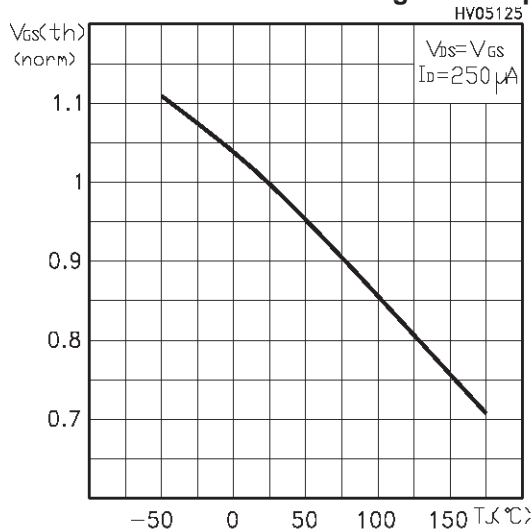
Gate Charge vs Gate-source Voltage



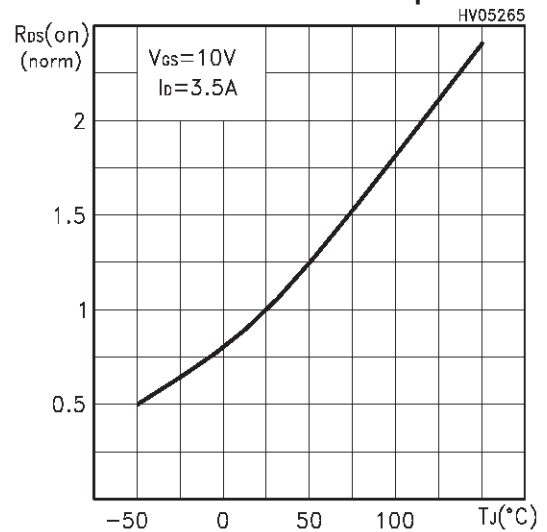
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

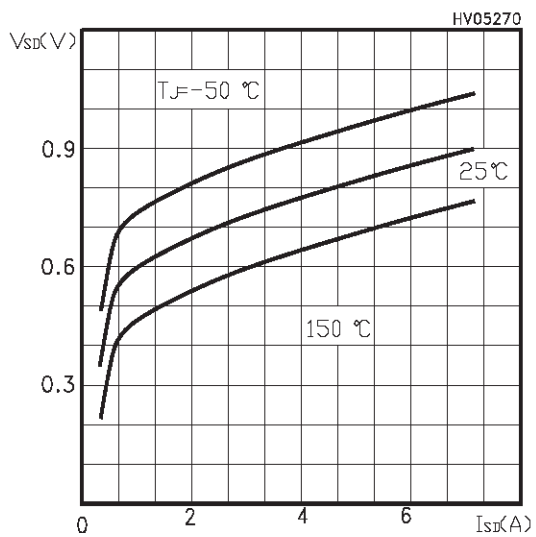


Fig. 1: Unclamped Inductive Load Test Circuit

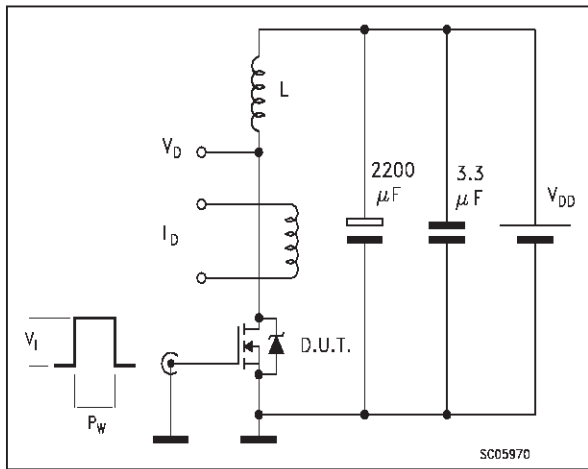


Fig. 2: Unclamped Inductive Waveform

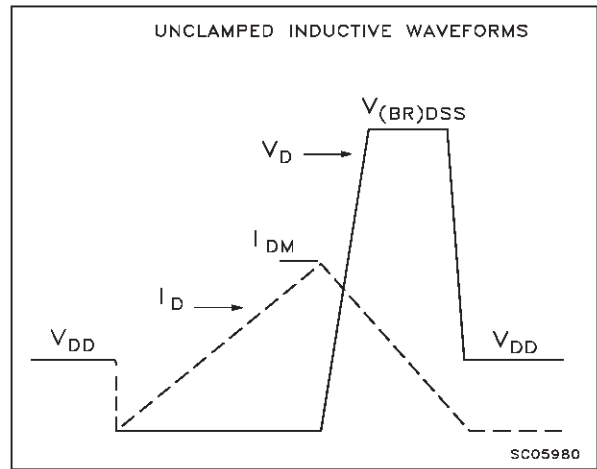


Fig. 3: Switching Times Test Circuits For Resistive Load

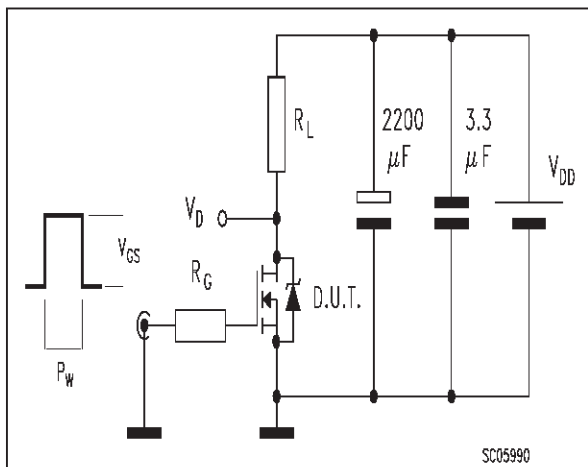


Fig. 4: Gate Charge test Circuit

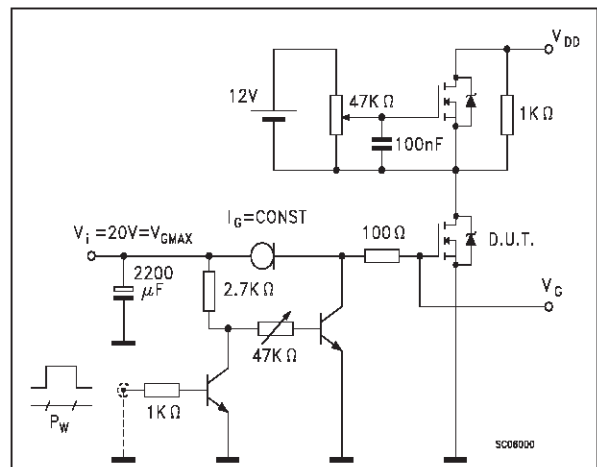
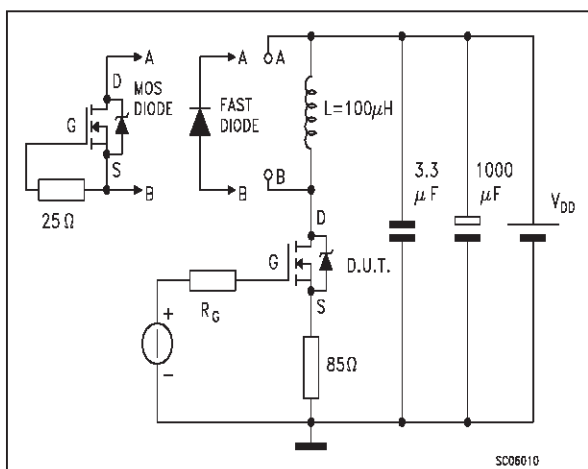
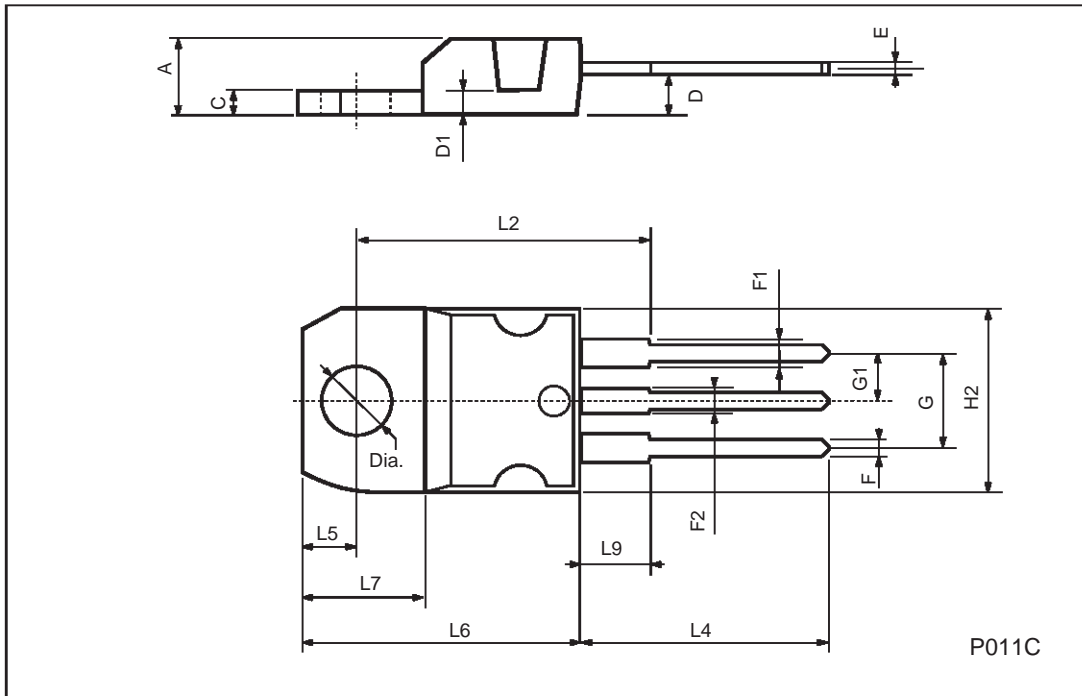


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



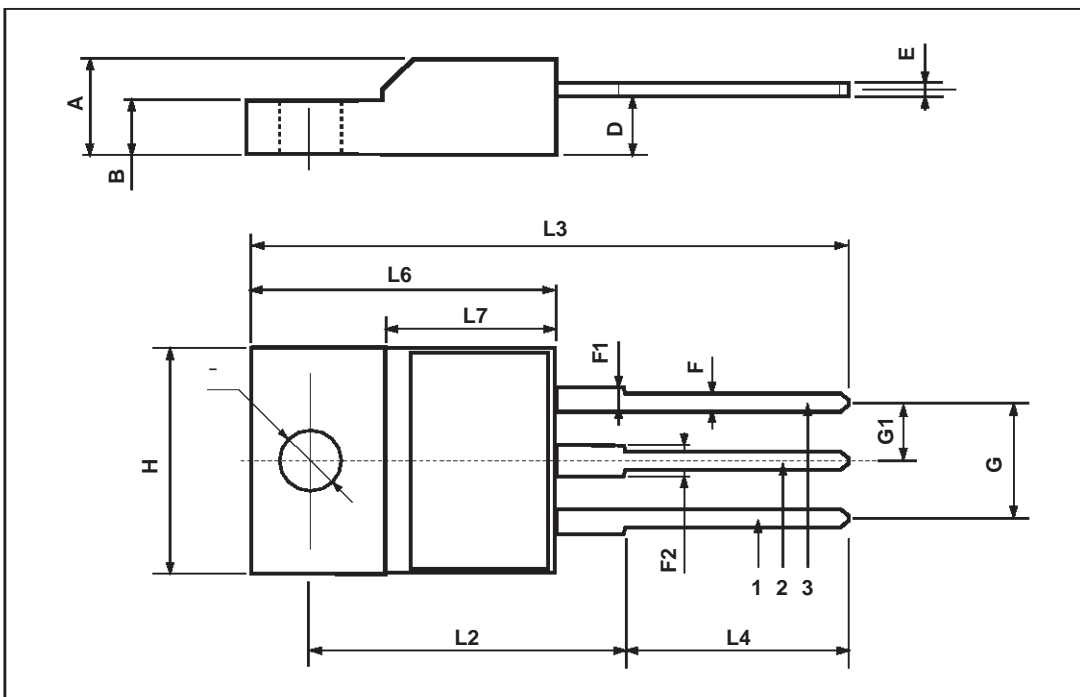
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



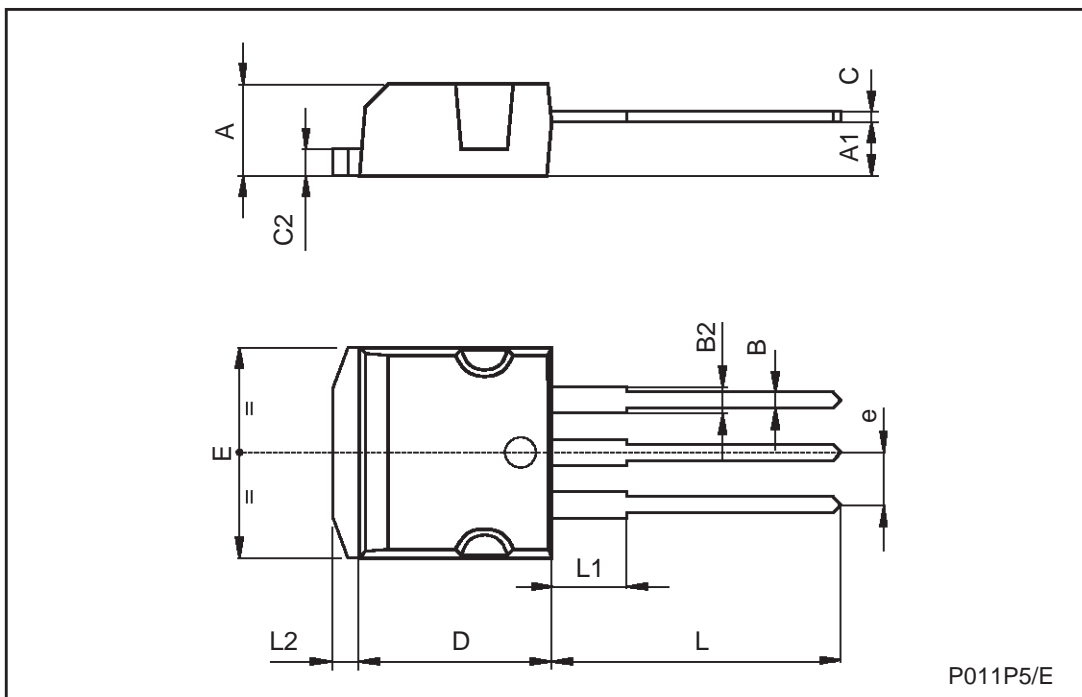
TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



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