



STD30NE06L

N - CHANNEL 60V - 0.025 Ω - 30A TO-252 STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD30NE06L	60 V	< 0.03 Ω	30 A

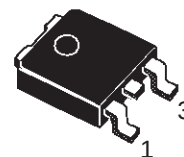
- TYPICAL R_{DS(on)} = 0.025 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW GATE CHARGE 100°C
- APPLICATION ORIENTED CHARACTERIZATION
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

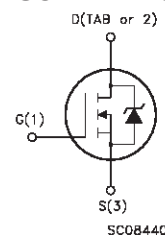
APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS



**DPAK
TO-252**
(Suffix "T4")

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	60	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 k Ω)	60	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	30	A
I _D	Drain Current (continuous) at T _c = 100 °C	21	A
I _{DM} (•)	Drain Current (pulsed)	120	A
P _{tot}	Total Dissipation at T _c = 25 °C	55	W
	Derating Factor	0.37	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} $\leq$ 30A, di/dt $\leq$ 300 A/ μ S, V_{DD} $\leq$ V_{(BR)DSS}, T_j $\leq$ T_{JMAX}

THERMAL DATA

$R_{thj-pcb}$	Thermal Resistance Junction-PC Board	Max	2.72	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	100	$^{\circ}\text{C/W}$
$R_{thj-sink}$	Thermal Resistance Case-sink	Typ	1.5	$^{\circ}\text{C/W}$
T_I	Maximum Lead Temperature For Soldering Purpose		275	$^{\circ}\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	30	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 25\text{ V}$)	100	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	60			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 15\text{ A}$ $V_{GS} = 5\text{ V}$ $I_D = 15\text{ A}$		0.022 0.025	0.028 0.030	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	30			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 15\text{ A}$	15	25		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0\text{ V}$		2370 350 90		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 30\text{ V}$ $I_D = 15\text{ A}$		27	50	ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Resistive Load, see fig. 3)		100	135	ns
Q_g	Total Gate Charge	$V_{DD} = 30\text{ V}$ $I_D = 30\text{ A}$ $V_{GS} = 5\text{ V}$		31	41	nC
Q_{gs}	Gate-Source Charge			13		nC
Q_{gd}	Gate-Drain Charge			13.5		nC

SWITCHING OFF

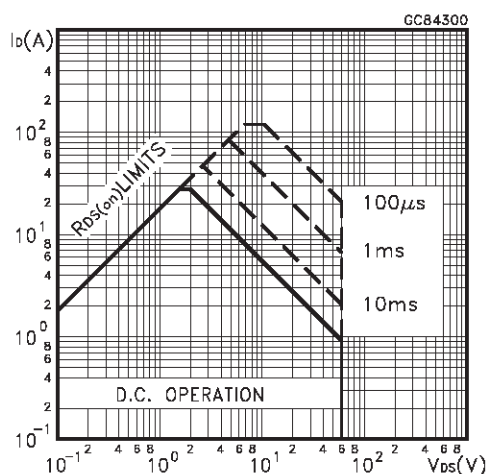
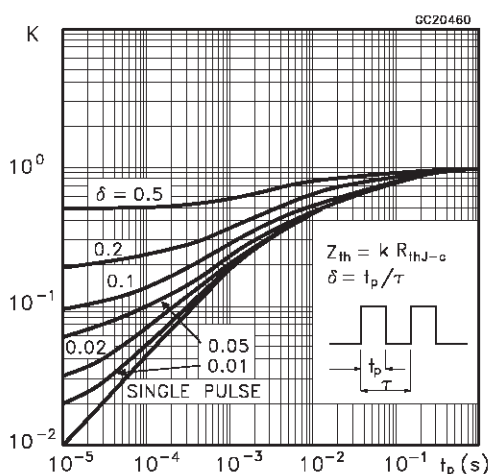
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_r(V_{off})$	Off-voltage Rise Time	$V_{DD} = 48\text{ V}$ $I_D = 30\text{ A}$		20	27	ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$		45	60	ns
t_c	Cross-over Time	(Inductive Load, see fig. 5)		72	100	ns

SOURCE DRAIN DIODE

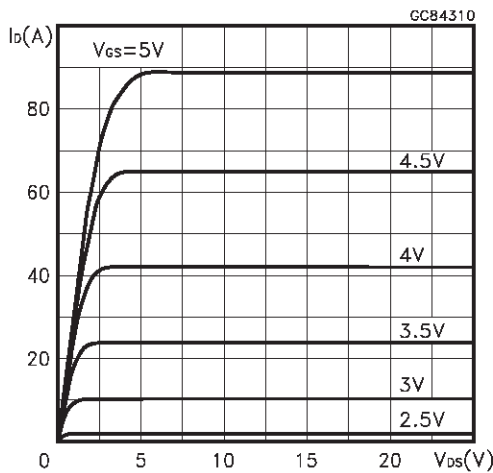
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				30	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				120	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 30\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 30\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		55		ns
Q_{rr}	Reverse Recovery Charge			0.1		μC
I_{RRM}	Reverse Recovery Current			3.5		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

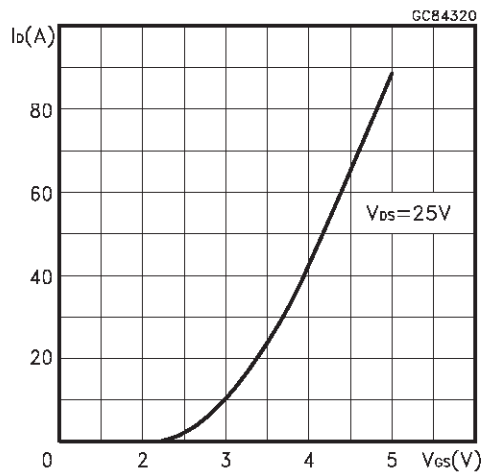
(•) Pulse width limited by safe operating area

Safe Operating Area**Thermal Impedance**

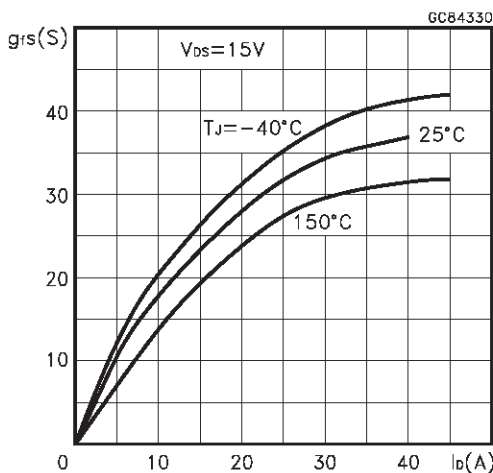
Output Characteristics



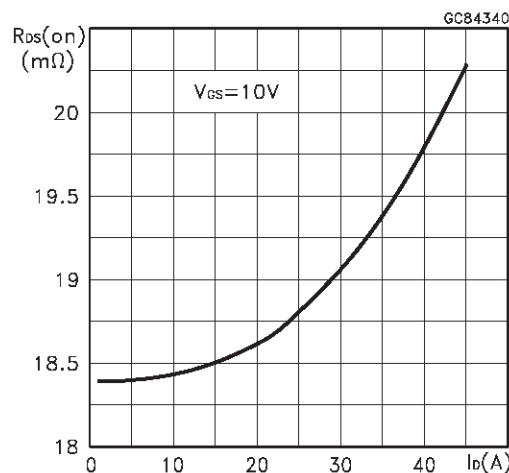
Transfer Characteristics



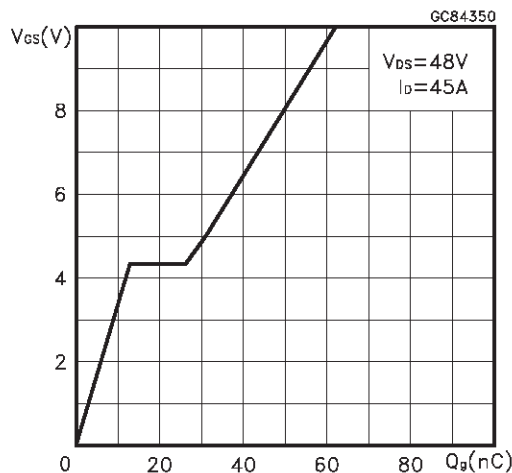
Transconductance



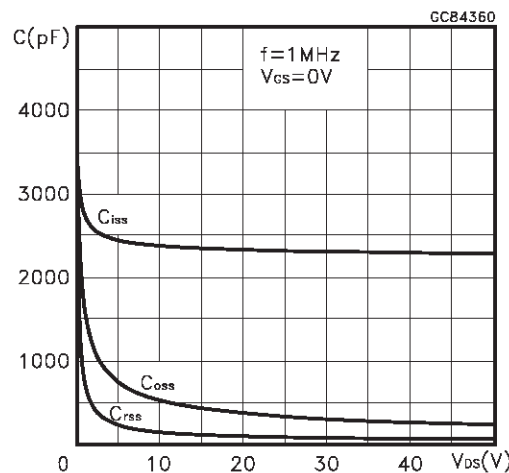
Static Drain-source On Resistance



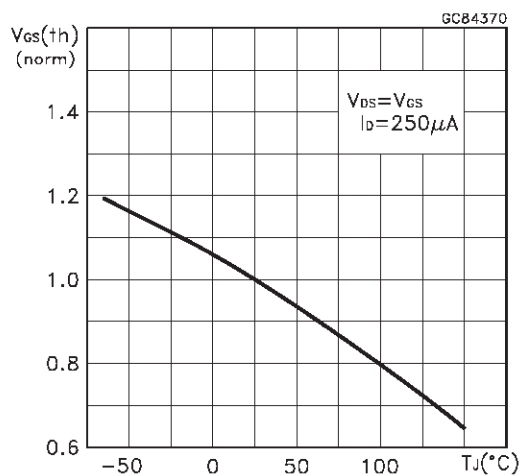
Gate Charge vs Gate-source Voltage



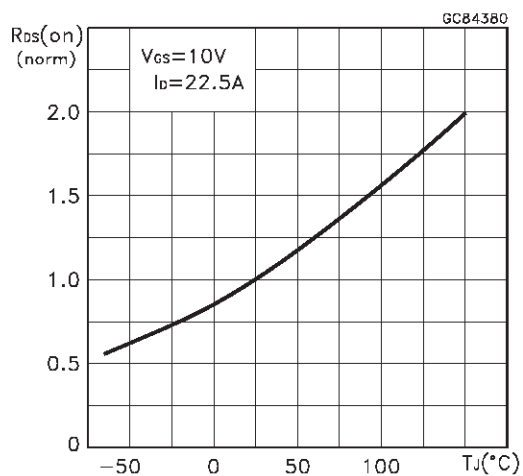
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

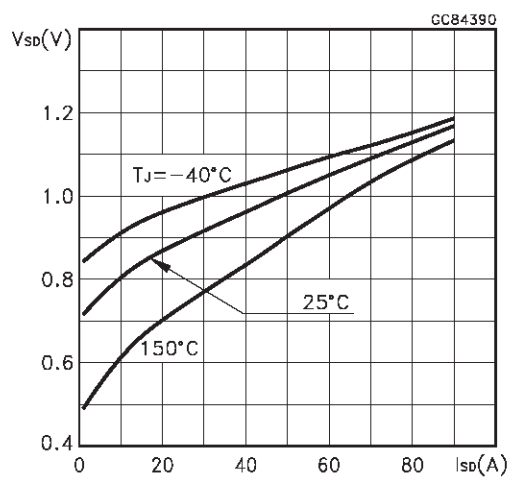


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Gate Charge test Circuit

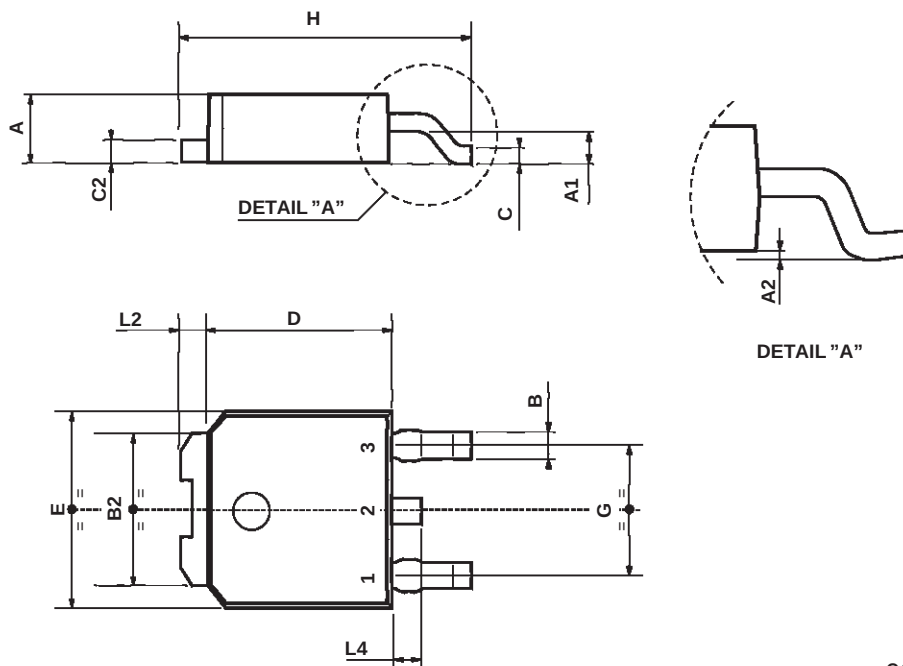


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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