



STGB10NB37LZ

N-CHANNEL CLAMPED 10A D²PAK INTERNALLY CLAMPED PowerMESH™ IGBT

TYPE	V _{CES}	V _{CE(sat)}	I _C
STGB10NB37LZ	CLAMPED	< 1.8 V	10 A

- POLYSILICON GATE VOLTAGE DRIVEN
- LOW THRESHOLD VOLTAGE
- LOW ON-VOLTAGE DROP
- HIGH CURRENT CAPABILITY
- HIGH VOLTAGE CLAMPING FEATURE
- SURFACE-MOUNTING D²PAK (TO-263)
POWER PACKAGE IN TUBE (NO SUFFIX)
OR IN TAPE & REEL (SUFFIX "T4")

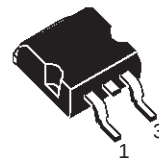
DESCRIPTION

Using the latest high voltage technology based on patented strip layout, SGS-Thomson has designed an advanced family of IGBTs with outstanding performances.

The built in collector-gate zener exhibits a very precise active clamping while the gate-emitter zener supplies an ESD protection.

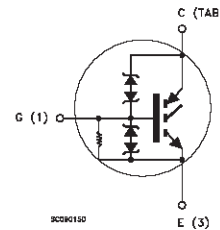
APPLICATIONS

- AUTOMOTIVE IGNITION



D²PAK
TO-263

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CES}	Collector-Emitter Voltage (V _{GS} = 0)	CLAMPED	V
V _{ECR}	Reverse Battery Protection	18	V
V _{GE}	Gate-Emitter Voltage	CLAMPED	V
I _C	Collector Current (continuous) at T _c = 25 °C	20	A
I _C	Collector Current (continuous) at T _c = 100 °C	20	A
I _{CM} (•)	Collector Current (pulsed)	60	A
P _{tot}	Total Dissipation at T _c = 25 °C	125	W
	Derating Factor	0.83	W/°C
E _{SD}	ESD (Human Body Model)	4	KV
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

STGB10NB37LZ

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	1.2	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	$^{\circ}C/W$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	0.2	$^{\circ}C/W$

ELECTRICAL CHARACTERISTICS ($T_j = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{(CES)}$	Clamped Voltage	$I_C = 2\text{ mA}$ $T_j = -40\text{ to }150^{\circ}C$ $V_{GE} = 0$	375	400	425	V
$BV_{(ECR)}$	Emitter Collector Break-down Voltage	$I_C = 75\text{ mA}$ $T_j = -40\text{ to }150^{\circ}C$ $V_{GE} = 0$	18			V
BV_{GE}	Gate Emitter Break-down Voltage	$I_C = \pm 2\text{ mA}$ $T_j = -40\text{ to }150^{\circ}C$	12		16	V
I_{CES}	Collector cut-off Current ($V_{GE} = 0$)	$V_{CE} = 15\text{ V}$ $V_{GE} = 0$ $T_j = 150^{\circ}C$ $V_{CE} = 200\text{ V}$ $V_{GE} = 0$ $T_j = 150^{\circ}C$			10 100	μA μA
I_{GES}	Gate-Emitter Leakage Current ($V_{CE} = 0$)	$V_{GE} = \pm 10\text{ V}$ $V_{CE} = 0$			± 0.7	mA
R_{GE}	Gate Emitter Resistance			20		$K\Omega$

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GE(th)}$	Gate Threshold Voltage	$V_{CE} = V_{GE}$ $I_C = 250\text{ }\mu A$ $T_j = -40\text{ to }150^{\circ}C$	0.6		2.4	V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	$V_{GE} = 4.5\text{ V}$ $I_C = 10\text{ A}$ $T_j = 25^{\circ}C$ $V_{GE} = 4.5\text{ V}$ $I_C = 10\text{ A}$ $T_j = -40^{\circ}C$		1.2 1.3	1.8	V V
I_C	Collector Current	$V_{GE} = 4.5\text{ V}$ $V_{CE} = 9\text{ V}$	20			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	$V_{CE} = 25\text{ V}$ $I_C = 10\text{ A}$	10	18		S
C_{ies} C_{oes} C_{res}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{CE} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GE} = 0$		1250 103 18	1700 140 25	pF pF pF
Q_G	Gate Charge	$V_{CE} = 320\text{ V}$ $I_C = 10\text{ A}$ $V_{GE} = 5\text{ V}$		28		nC

FUNCTIONAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_L	Latching Current	$V_{CLAMP} = 320\text{ V}$ $V_{GE} = 5\text{ V}$ $R_{G\text{OFF}} = 1\text{ K}\Omega$ $T_C = 125\text{ }^\circ\text{C}$	20			A
U.I.S.	Unclamped Inductive Switching Current Functional Test	$R_{G\text{OFF}} = 1\text{ K}\Omega$ $L = 200\text{ }\mu\text{H}$ $T_J = 125\text{ }^\circ\text{C}$ $R_{G\text{OFF}} = 1\text{ K}\Omega$ $L = 3\text{ mH}$ $T_{\text{start}} = 55\text{ }^\circ\text{C}$	15 12			A A
E_{AS}	Single Pulse Avalanche Energy	$T_{\text{start}} = 55\text{ }^\circ\text{C}$ $T_{\text{start}} = 150\text{ }^\circ\text{C}$			215 150	mJ mJ
E_{AR}	Reverse Avalanche Energy	$T_C = 125\text{ }^\circ\text{C}$ duty cycle < 1% pulse width limited by $t_{j\text{max}}$			10	mJ

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(\text{on})}$ t_r	Delay Time Rise Time	$V_{CC} = 320\text{ V}$ $I_C = 10\text{ A}$ $V_{GE} = 5\text{ V}$ $R_G = 1\text{ K}\Omega$		520 340		ns ns
$(di/dt)_{\text{on}}$ E_{on}	Turn-on Current Slope Turn-on Switching Losses	$V_{CC} = 320\text{ V}$ $I_C = 10\text{ A}$ $R_G = 1\text{ K}\Omega$ $V_{GE} = 5\text{ V}$		17 180		A/ μs μJ

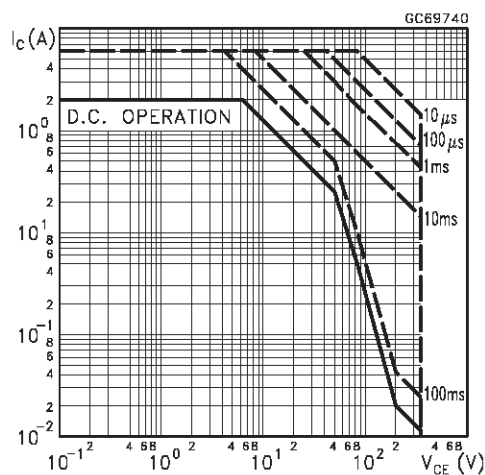
SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_c $t_r(v_{\text{off}})$ t_f $t_{d(\text{off})}$ $E_{\text{off}}(**)$	Cross-Over Time Off Voltage Rise Time Fall Time Off Voltage Delay Time Turn-off Switching Loss	$V_{CLAMP} = 320\text{ V}$ $I_C = 10\text{ A}$ $R_{GE} = 1\text{ K}\Omega$ $V_{GE} = 5\text{ V}$		4 2.2 1.5 14.8 4.0		μs μs μs μs mJ
t_c $t_r(v_{\text{off}})$ t_f $t_{d(\text{off})}$ $E_{\text{off}}(**)$	Cross-Over Time Off Voltage Rise Time Fall Time Off Voltage Delay Time Turn-off Switching Loss	$V_{CLAMP} = 320\text{ V}$ $I_C = 10\text{ A}$ $R_{GE} = 1\text{ K}\Omega$ $V_{GE} = 5\text{ V}$ $T_J = 125\text{ }^\circ\text{C}$		5.2 2.8 2 15.8 6.5		μs μs μs μs mJ

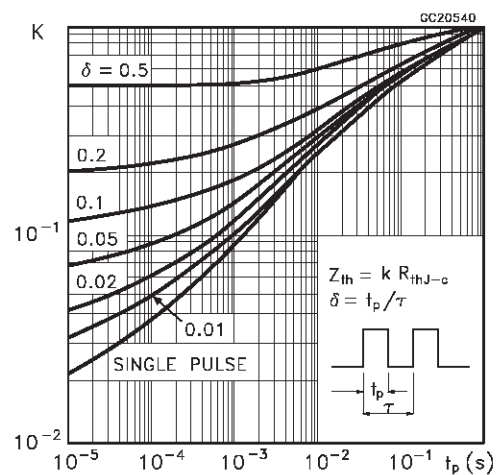
(*) Pulse width limited by safe operating area (**) Pulsed: Pulse duration = 300 ms, duty cycle 1.5 %

(**) Losses Include Also The Tail (jedec Standardization)

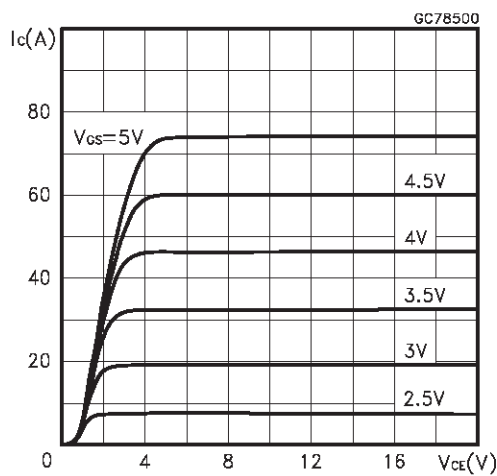
Safe Operating Area



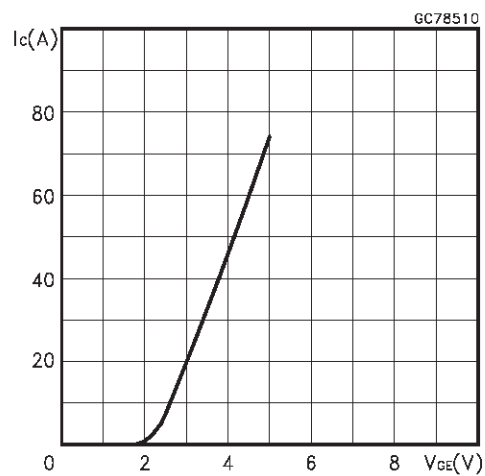
Thermal Impedance



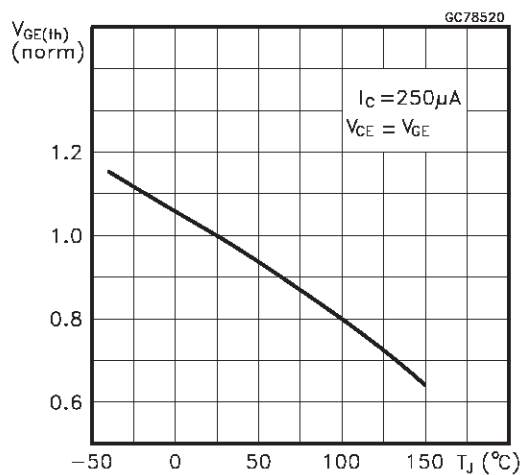
Output Characteristics



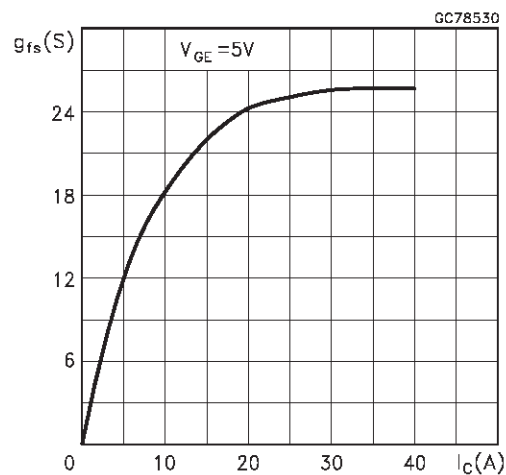
Transfer Characteristics



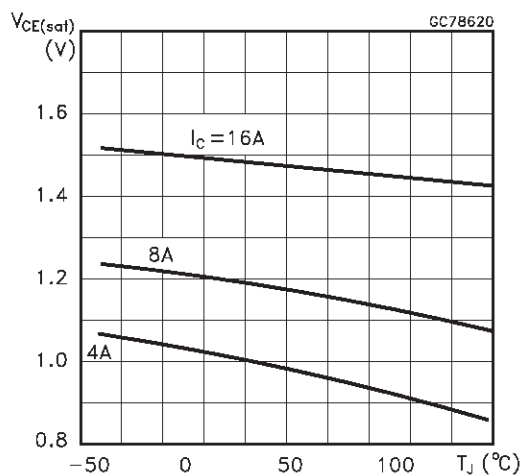
Normalized Gate Threshold Voltage vs Temperature



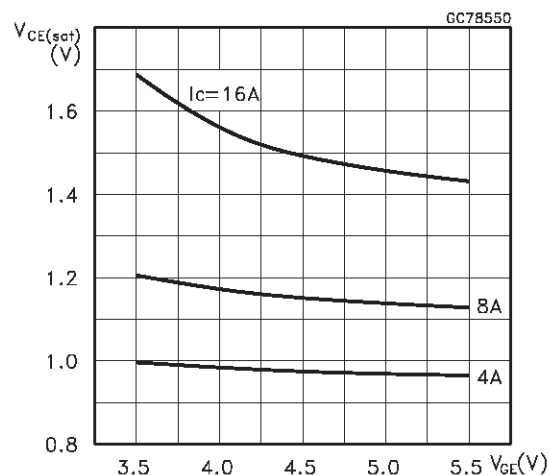
Transconductance



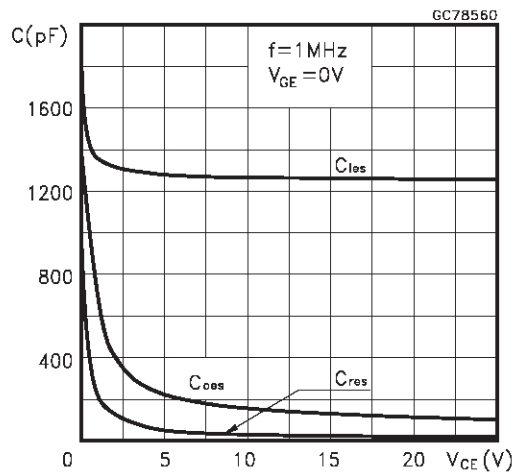
Collector-Emitter On Voltage vs Temperature



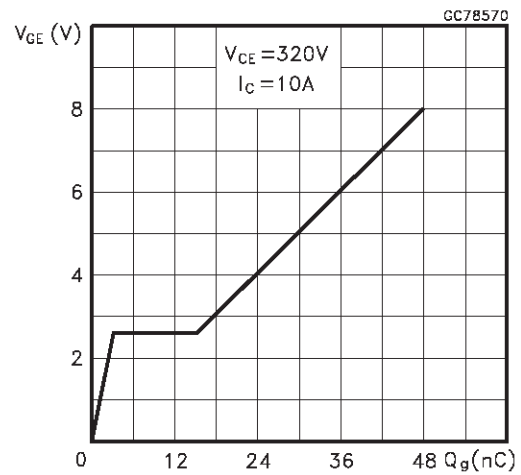
Collector-Emitter On Voltage vs Gate-Emitter Voltage



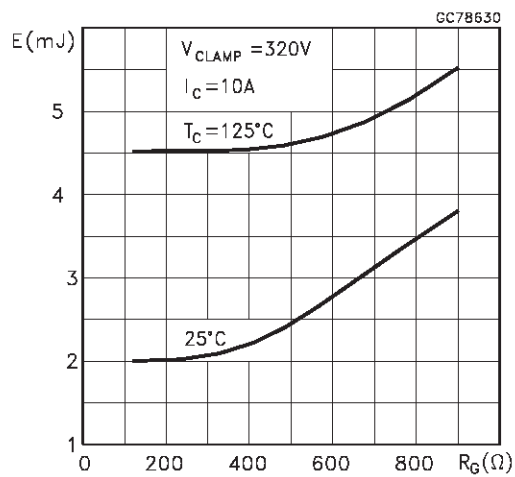
Capacitance Variations



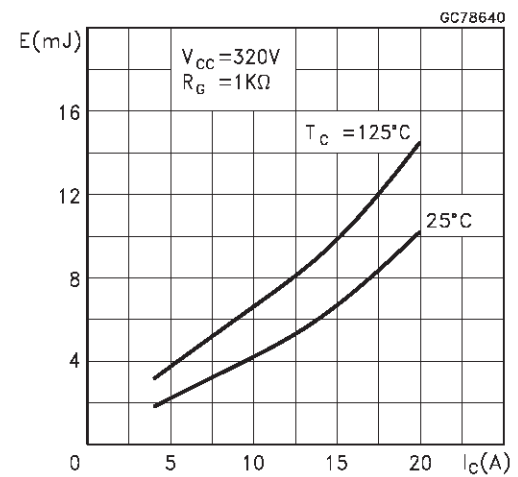
Gate Charge vs Gate-Emitter Voltage



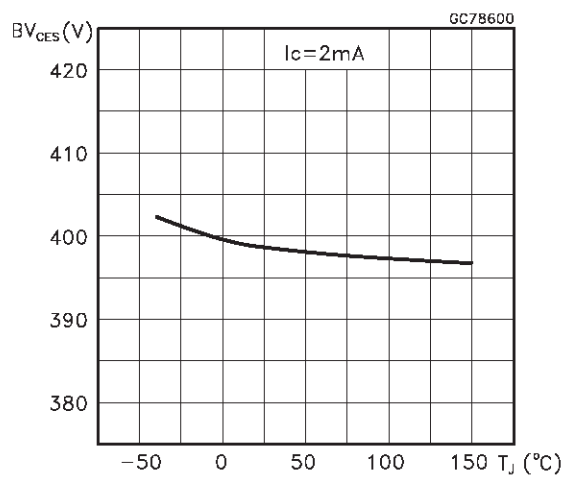
Off Losses vs Gate Resistance



Off Losses vs Collector Current



Break-down Voltage vs Temperature



Clamping Voltage vs Gate Resistance

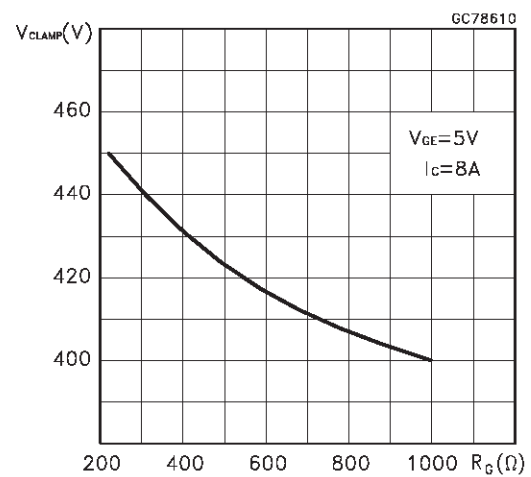


Fig. 1: Unclamped Inductive Load Test Circuit

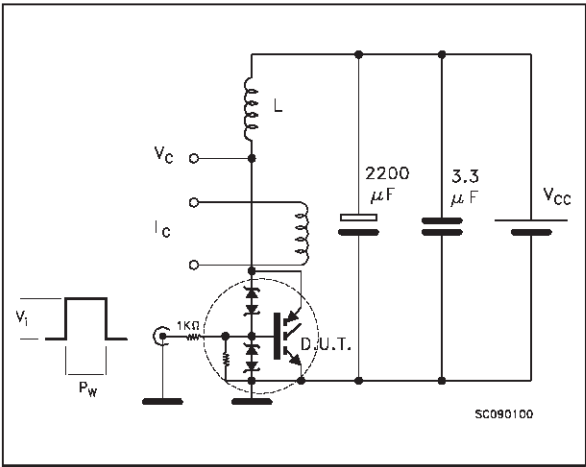


Fig. 2: Unclamped Inductive Waveform

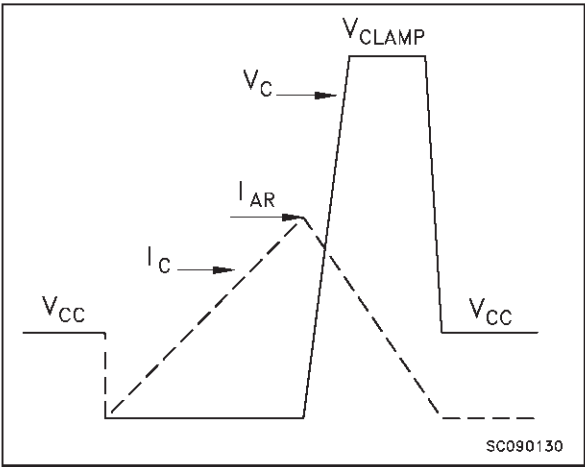


Fig. 3: Switching Times Test Circuits For Resistive Load

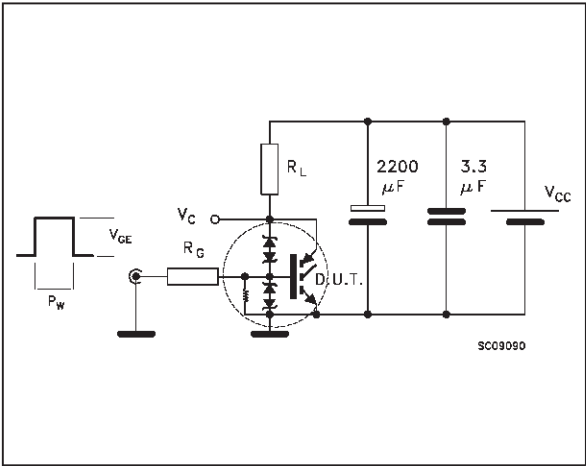


Fig. 4: Gate Charge test Circuit

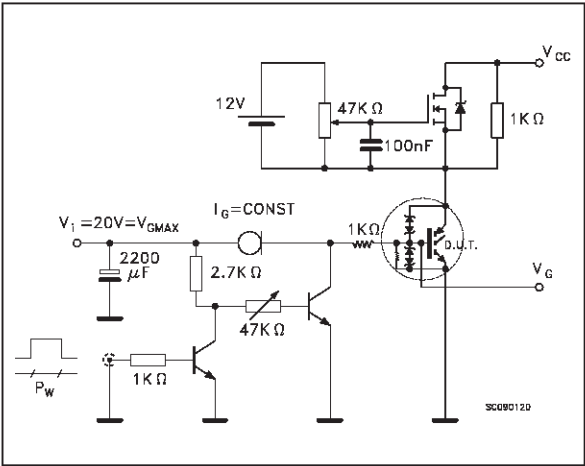
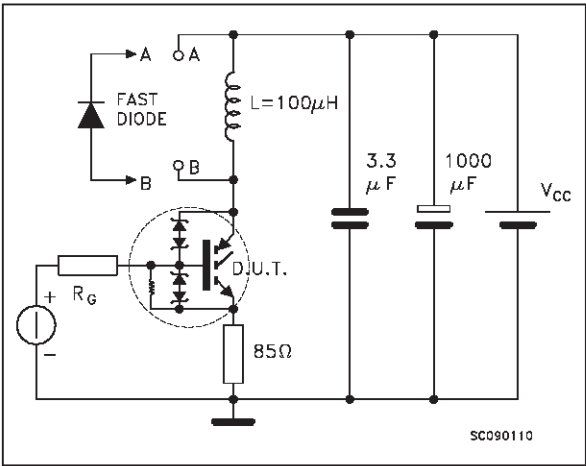
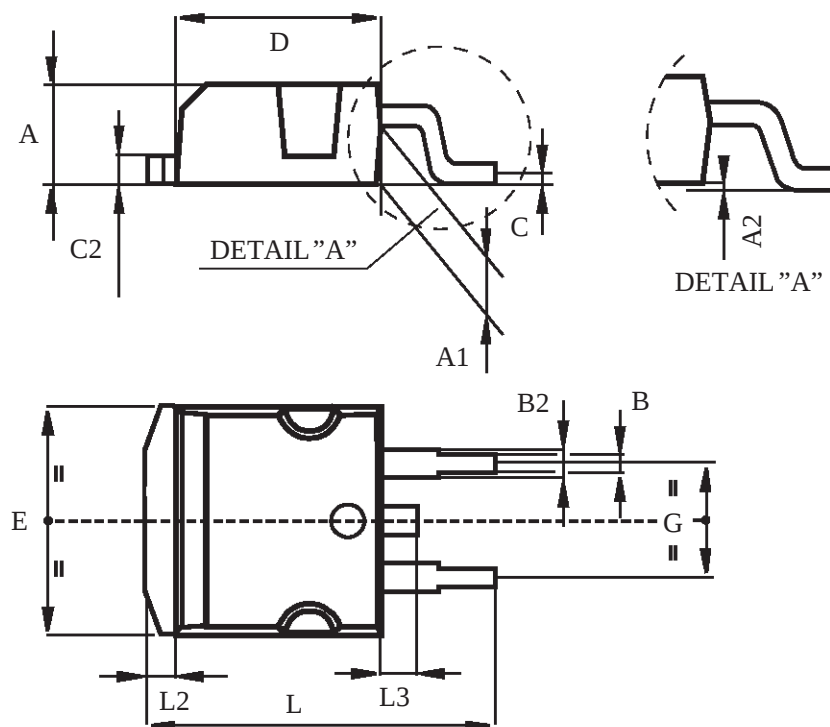


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-263 (D²PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.21		1.36	0.047		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



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