



STGD7NB60K

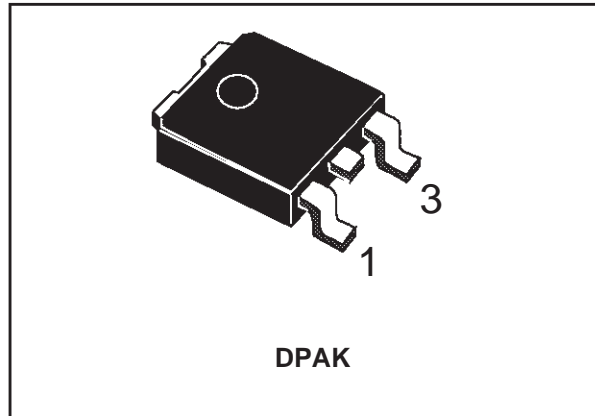
N-CHANNEL 7A - 600V - DPAK

SHORT CIRCUIT PROOF PowerMESH™ IGBT

PRELIMINARY DATA

TYPE	V _{CES}	V _{CE(sat)}	I _C
STD7NB60K	600 V	< 2.8 V	7 A

- HIGH INPUT IMPEDANCE (VOLTAGE DRIVEN)
- LOW ON-VOLTAGE DROP (V_{cesat})
- LOW ON-LOSSES
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- OFF LOSSES INCLUDE TAIL CURRENT
- VERY HIGH FREQUENCY OPERATION
- SHORT CIRCUIT RATED
- LATCH CURRENT FREE OPERATION

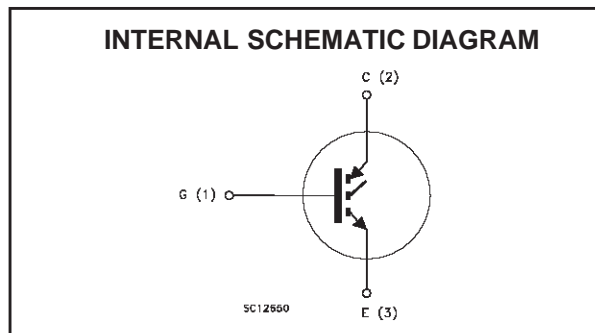


DESCRIPTION

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix "K" identifies a family optimized for high frequency motor control applications with short circuit withstand capability.

APPLICATIONS

- HIGH FREQUENCY MOTOR CONTROLS
- SMPS and PFC



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CES}	Collector-Emitter Voltage (V _{GS} = 0)	600	V
V _{ECR}	Emitter-Collector Voltage	20	V
V _{GE}	Gate-Emitter Voltage	±20	V
I _C	Collector Current (continuous) at T _C = 25°C	14	A
I _C	Collector Current (continuous) at T _C = 100°C	7	A
I _{CM} (■)	Collector Current (pulsed)	56	A
T _{sc}	Short Circuit Withstand	10	μs
P _{TOT}	Total Dissipation at T _C = 25°C	55	W
	Derating Factor	0.44	W/°C
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	2.27	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	100	°C/W
Rthc-h	Thermal Resistance Case-heatsink Typ	0.5	°C/W

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collectro-Emitter Breakdown Voltage	$I_C = 250 \mu A, V_{GE} = 0$	600			V
I_{CES}	Collector cut-off ($V_{GE} = 0$)	$V_{CE} = \text{Max Rating}, T_C = 25 \text{ }^\circ\text{C}$ $V_{CE} = \text{Max Rating}, T_C = 125 \text{ }^\circ\text{C}$			10 100	μA μA
I_{GES}	Gate-Emitter Leakage Current ($V_{CE} = 0$)	$V_{GE} = \pm 20V, V_{CE} = 0$			± 100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GE(th)}$	Gate Threshold Voltage	$V_{CE} = V_{GE}, I_C = 250\mu A$	5		7	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$V_{GE} = 15V, I_C = 7 A$ $V_{GE} = 15V, I_C = 7 A, T_J = 125^\circ\text{C}$		2.3 1.9	2.8	V V

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	$V_{CE} = 25 V, I_C = 7 A$	3.5	5		S
C_{ies}	Input Capacitance	$V_{CE} = 25V, f = 1 \text{ MHz}, V_{GE} = 0$		560		pF
C_{oes}	Output Capacitance		68		pF	
C_{res}	Reverse Transfer Capacitance		15		pF	
Q_g	Total Gate Charge	$V_{CE} = 480V, I_C = 7 A,$ $V_{GE} = 15V$		42	55	nC
Q_{ge}	Gate-Emitter Charge		T.B.D.		nC	
Q_{gc}	Gate-Collector Charge		T.B.D.		nC	
tscw	Short Circuit Withstand Time	$V_{ce} = 0.5 BV_{ces}, V_{GE} = 15 V,$ $T_J = 125^\circ\text{C}, R_G = 10 \Omega$	10			μs

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{CC} = 480 V, I_C = 7 A$ $R_G = 10 \Omega, V_{GE} = 15 V$		15		ns
t_r	Rise Time		48		ns	
$(di/dt)_{on}$	Turn-on Current Slope	$V_{CC} = 480 V, I_C = 7 A, R_G = 10 \Omega$ $V_{GE} = 15 V, T_J = 125^\circ\text{C}$		160		A/ μs
Eon	Turn-on Switching Losses			70		μJ

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_c	Cross-over Time	$V_{CC} = 480 \text{ V}$, $I_C = 7 \text{ A}$, $R_{GE} = 10 \Omega$, $V_{GE} = 15 \text{ V}$		85		ns
$t_r(V_{off})$	Off Voltage Rise Time			20		ns
$t_{d(off)}$	Delay Time			75		ns
t_f	Fall Time			70		ns
$E_{off(**)}$	Turn-off Switching Loss			85		μJ
E_{ts}	Total Switching Loss			130		μJ
t_c	Cross-over Time	$V_{CC} = 480 \text{ V}$, $I_C = 7 \text{ A}$, $R_{GE} = 10 \Omega$, $V_{GE} = 15 \text{ V}$ $T_j = 125 \text{ }^\circ\text{C}$		150		ns
$t_r(V_{off})$	Off Voltage Rise Time			50		ns
$t_{d(off)}$	Delay Time			110		ns
t_f	Fall Time			110		ns
$E_{off(**)}$	Turn-off Switching Loss			220		μJ
E_{ts}	Total Switching Loss			290		μJ

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by max. junction temperature.
 (**). Losses include Also the Tail (Jedec Standardization)

Fig. 1: Gate Charge test Circuit

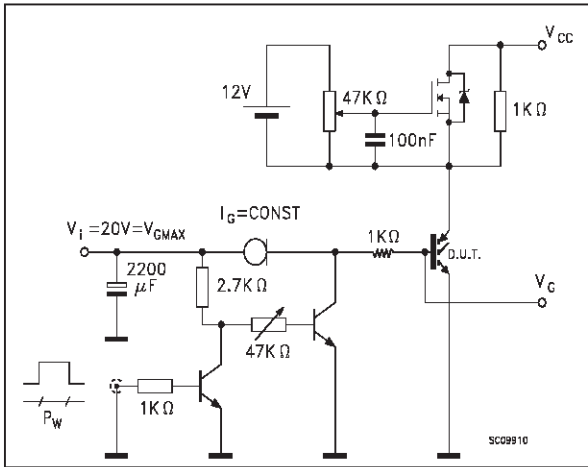
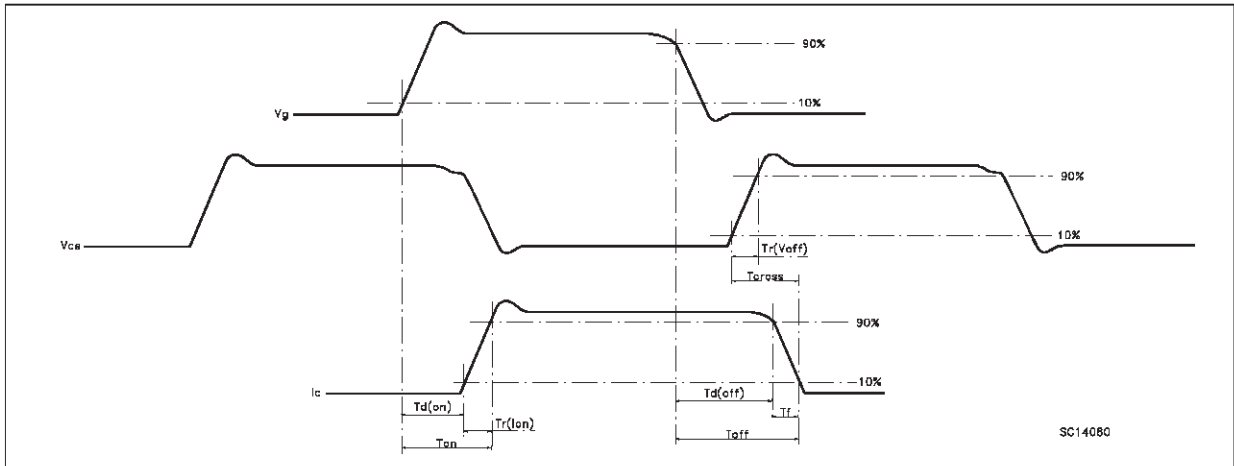
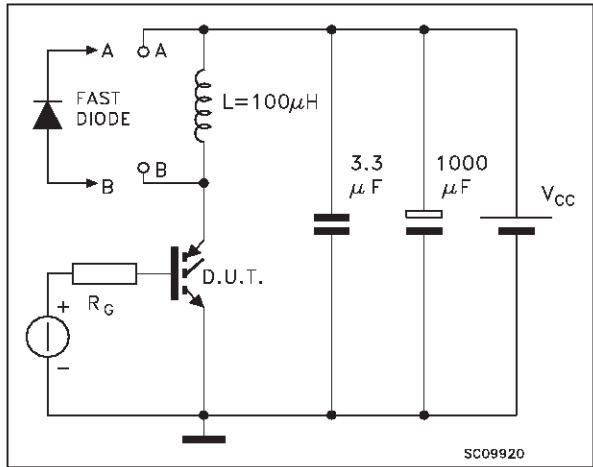
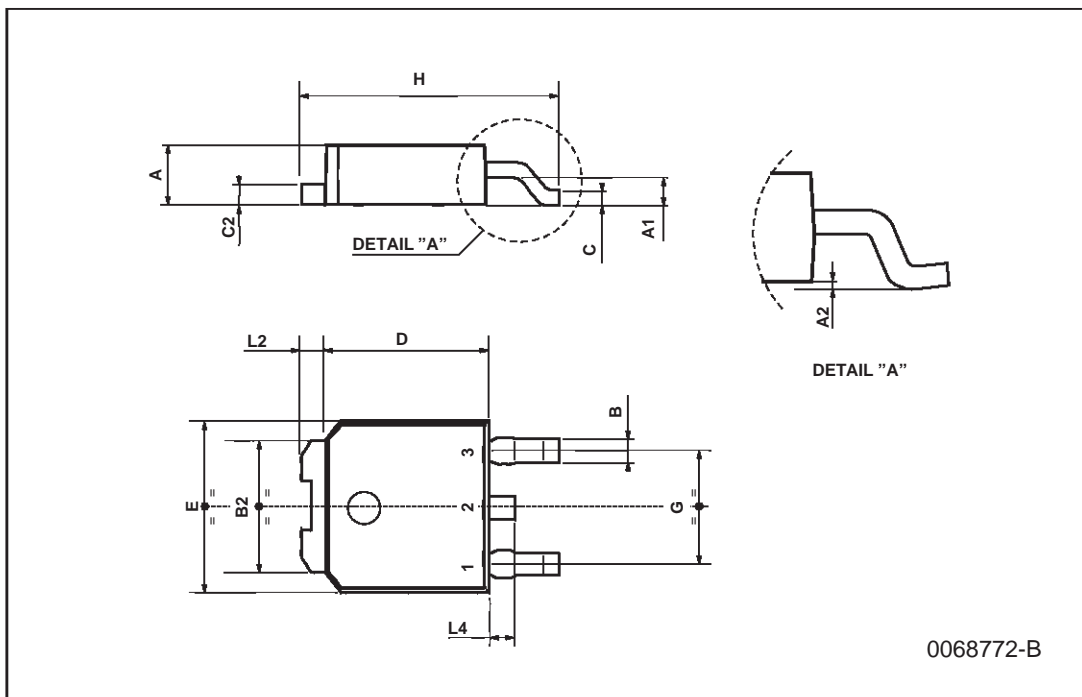


Fig. 2: Test Circuit For Inductive Load Switching



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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