



# STP20NE06 STP20NE06FP

N - CHANNEL 60V - 0.06  $\Omega$  - 20A TO-220/TO-220FP  
STripFET™ POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP20NE06	60 V	< 0.080 $\Omega$	20 A
STP20NE06FP	60 V	< 0.080 $\Omega$	13 A

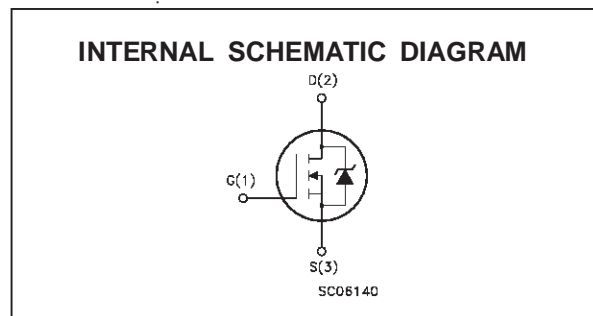
- TYPICAL R<sub>DS(on)</sub> = 0.06  $\Omega$
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW GATE CHARGE 100 °C
- APPLICATION ORIENTED CHARACTERIZATION

### DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique " Single Feature Size™ " strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC & DC-AC CONVERTERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP20NE06	STP20NE06FP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	60		V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	60		V
V <sub>GS</sub>	Gate-source Voltage	$\pm 20$		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 25 °C	20	13	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>c</sub> = 100 °C	14	9	A
I <sub>DM</sub> (*)	Drain Current (pulsed)	80	80	A
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	70	30	W
	Derating Factor	0.47	0.2	W/°C
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	—	2000	V
dv/dt	Peak Diode Recovery voltage slope	7		V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 175		°C
T <sub>j</sub>	Max. Operating Junction Temperature	175		°C

(\*) Pulse width limited by safe operating area

(1) I<sub>SD</sub>  $\leq$  20 A, di/dt  $\leq$  300 A/ $\mu$ S, V<sub>DD</sub>  $\leq$  V<sub>(BR)DSS</sub>, T<sub>j</sub>  $\leq$  T<sub>JMAX</sub>

## STP20NE06/FP

### THERMAL DATA

			TO-220	TO-220FP	
R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	2.14	5	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max	62.5		°C/W
R <sub>thc-sink</sub>	Thermal Resistance Case-sink	Typ	0.5		°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose		300		°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	20	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 25V)	100	mJ

### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>c</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			± 100	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 10 A		0.060	0.080	Ω
I <sub>D(on)</sub>	On State Drain Current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> V <sub>GS</sub> = 10 V	20			A

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> I <sub>D</sub> = 10 A	5	9		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V f = 1 MHz V <sub>GS</sub> = 0		900		pF
C <sub>oss</sub>	Output Capacitance			125		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			35		pF

**ELECTRICAL CHARACTERISTICS** (continued)

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 30\text{ V}$ $I_D = 10\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		20		ns
$t_r$	Rise Time			45		ns
$Q_g$	Total Gate Charge	$V_{DD} = 48\text{ V}$ $I_D = 20\text{ A}$ $V_{GS} = 10\text{ V}$		25	35	nC
$Q_{gs}$	Gate-Source Charge			10		nC
$Q_{gd}$	Gate-Drain Charge			6		nC

**SWITCHING OFF**

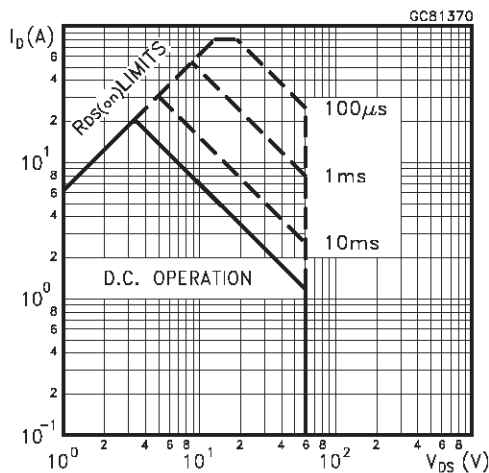
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 48\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		8		ns
$t_f$	Fall Time			25		ns
$t_c$	Cross-over Time			37		ns

**SOURCE DRAIN DIODE**

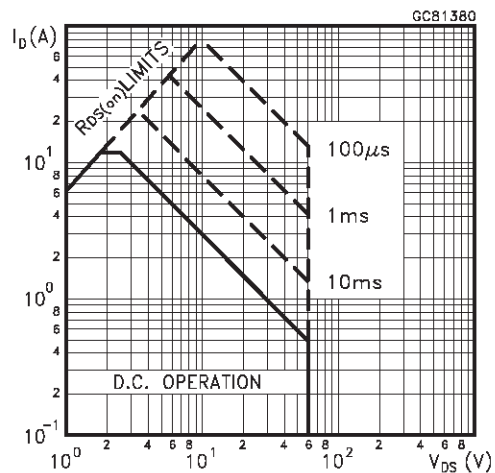
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				20	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				80	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 20\text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 20\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		50		ns
$Q_{rr}$	Reverse Recovery Charge			115		nC
$I_{RRM}$	Reverse Recovery Current			4.5		A

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %  
 (•) Pulse width limited by safe operating area

Safe Operating Area for TO-220

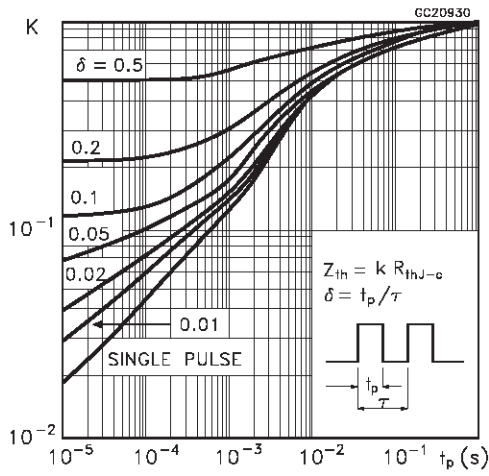


Safe Operating Area for TO-220FP

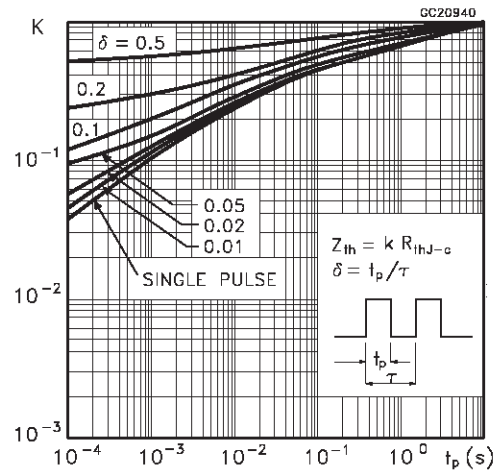


# STP20NE06/FP

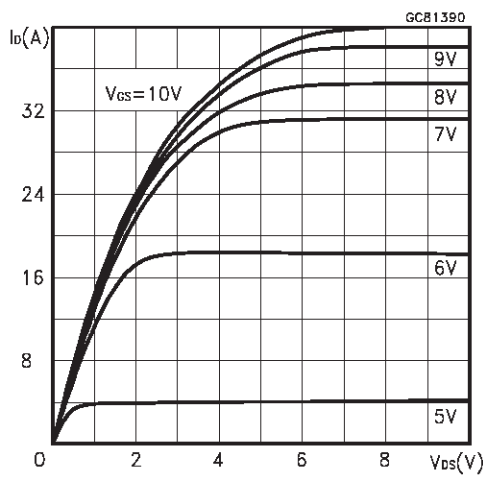
Thermal Impedance for TO-220



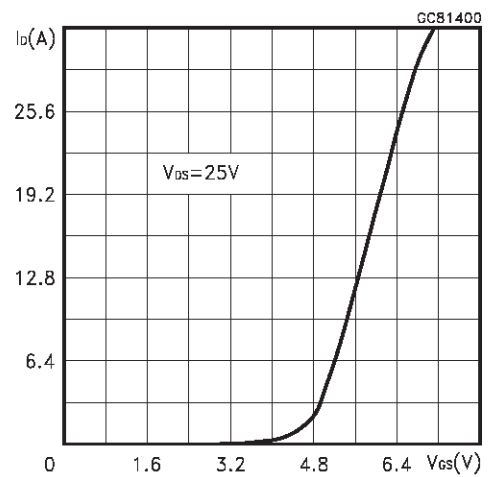
Thermal Impedance for TO-220FP



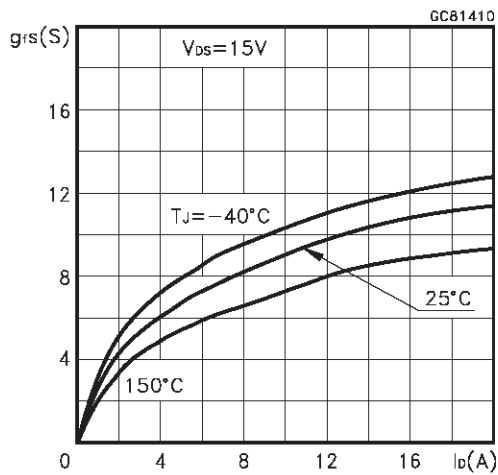
Output Characteristics



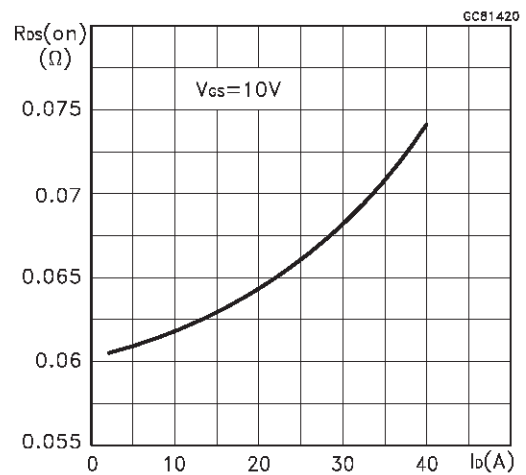
Transfer Characteristics



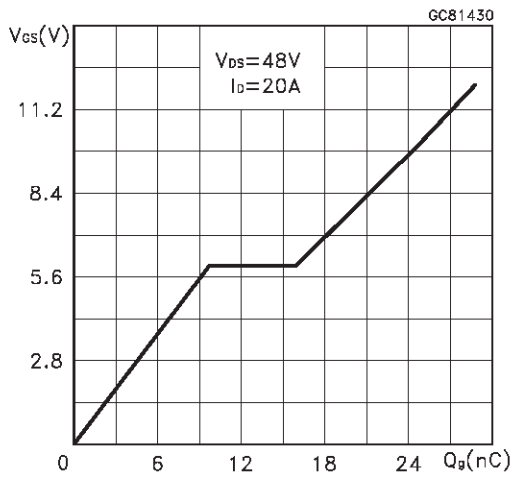
Transconductance



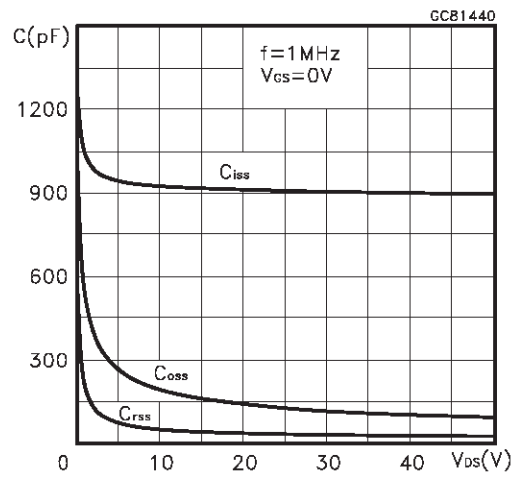
Static Drain-source On Resistance



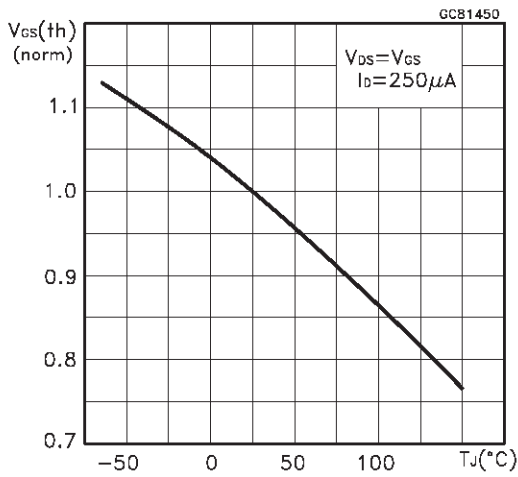
Gate Charge vs Gate-source Voltage



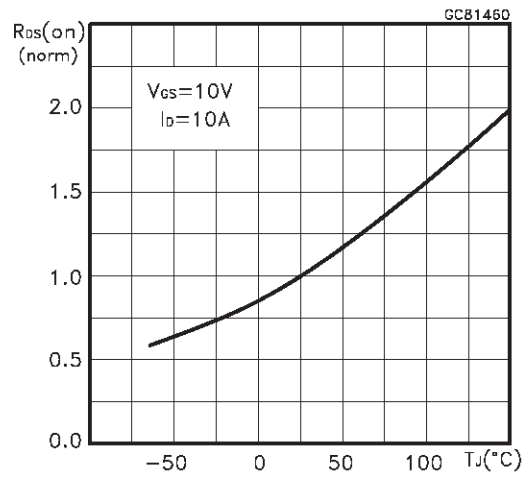
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

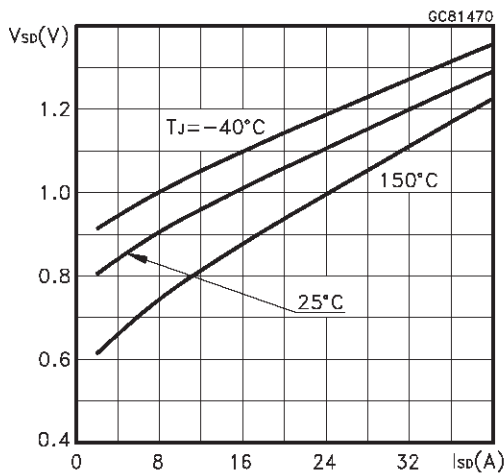


Fig. 1: Unclamped Inductive Load Test Circuit

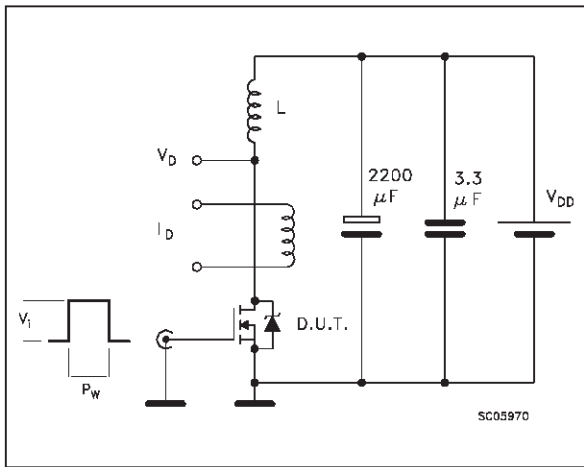


Fig. 2: Unclamped Inductive Waveform

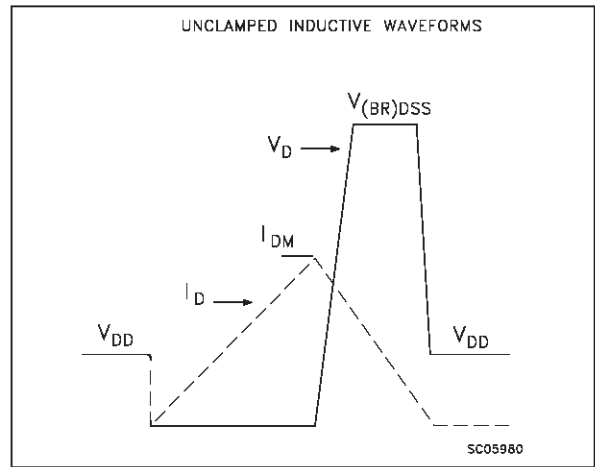


Fig. 3: Switching Times Test Circuits For Resistive Load

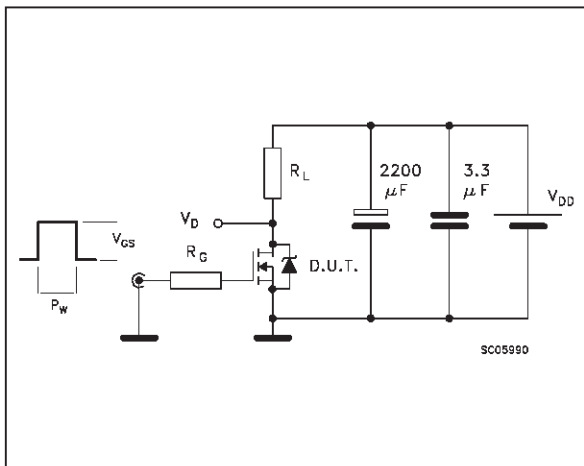


Fig. 4: Gate Charge test Circuit

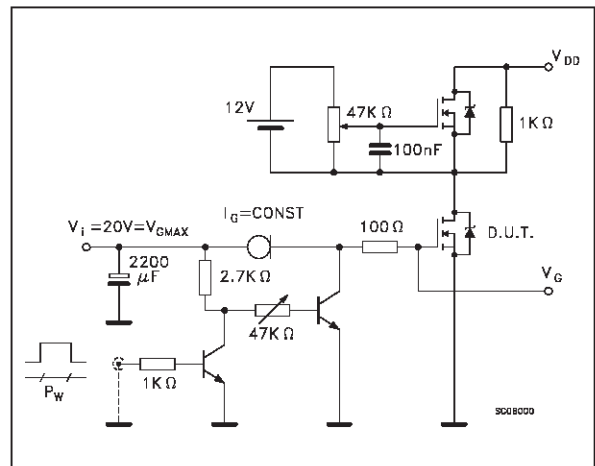
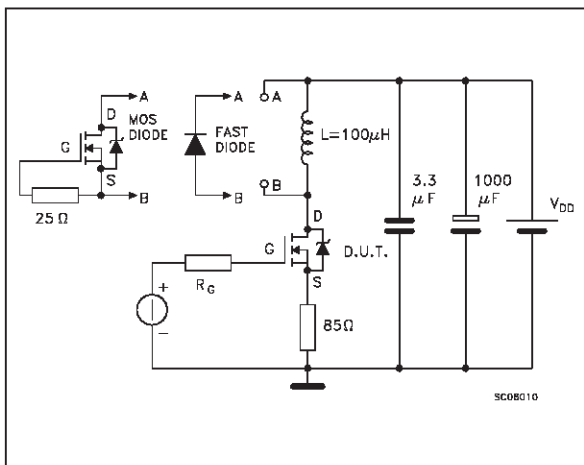
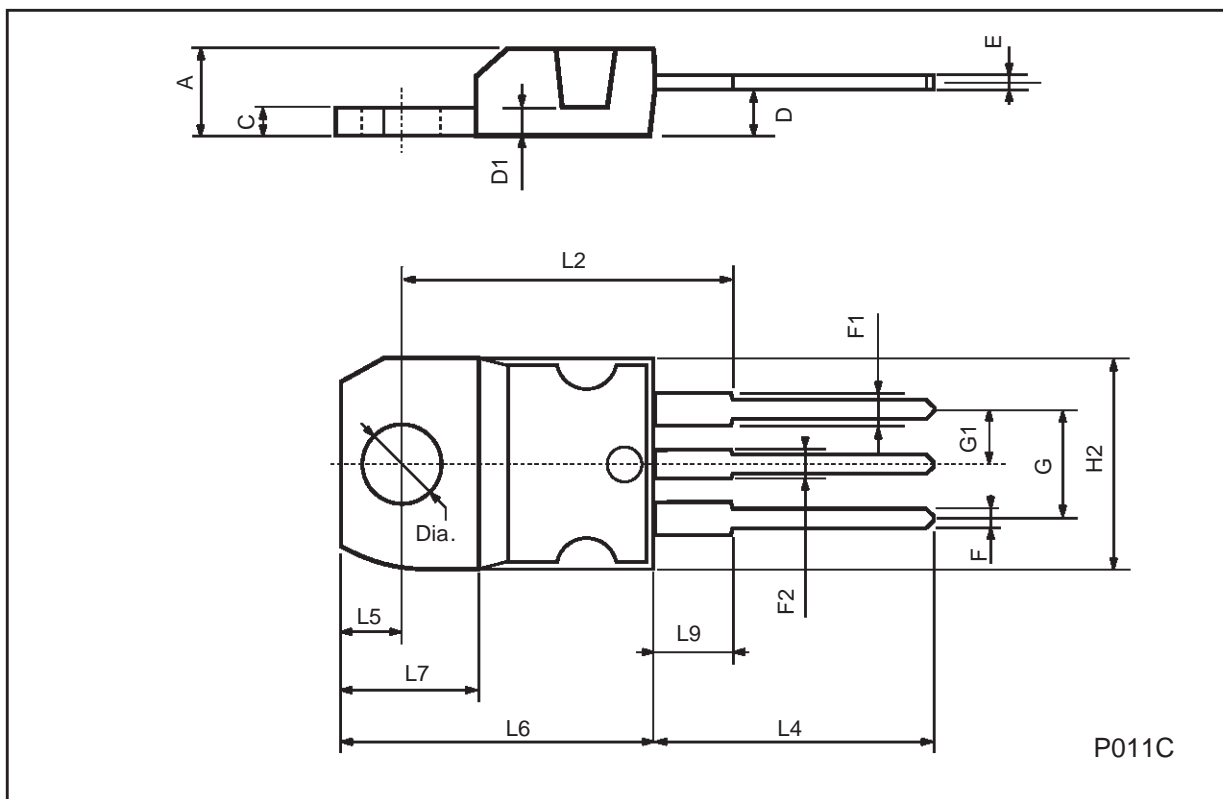


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



## TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126





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