



STP4NB50 STP4NB50FP

N - CHANNEL ENHANCEMENT MODE PowerMESH™ MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP4NB50	500 V	< 2.8 Ω	3.8 A
STP4NB50FP	500 V	< 2.8 Ω	2.5 A

- TYPICAL R_{DS(on)} = 2.5 Ω
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED
- EXTREMELY HIGH dv/dt CAPABILITY

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, SGS-Thomson has designed an advanced family of Power MOSFETs with outstanding performance. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R_{DS(on)} per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

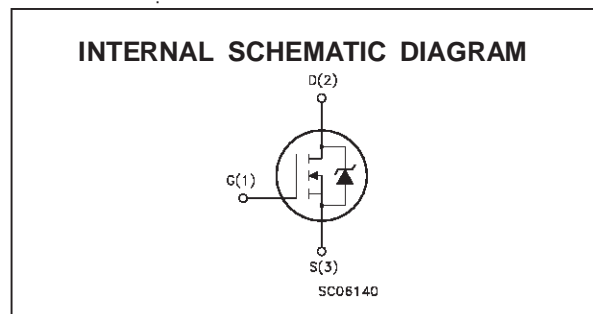
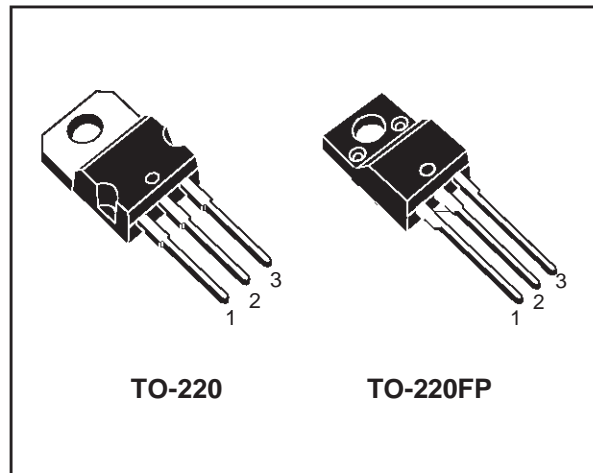
- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP4NB50	STP4NB50FP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500		V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	500		V
V _{GS}	Gate-source Voltage	± 30		V
I _D	Drain Current (continuous) at T _c = 25 °C	3.8	2.5	A
I _D	Drain Current (continuous) at T _c = 100 °C	2.4	1.6	A
I _{DM} (•)	Drain Current (pulsed)	15.2	15.2	A
P _{tot}	Total Dissipation at T _c = 25 °C	80	35	W
	Derating Factor	0.64	0.28	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4.5	4.5	V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	—	2500	V
T _{stg}	Storage Temperature	-65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 4A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}



STP4NB50/FP

THERMAL DATA

			TO-220	TO220-FP	
R _{thj-case}	Thermal Resistance Junction-case	Max	1.56	3.57	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	62.5		°C/W
R _{thc-sink}	Thermal Resistance Case-sink	Typ	0.5		°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max, δ < 1%)	3.8	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	220	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA V _{GS} = 0	500			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _c = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 30 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V I _D = 1.9 A		2.5	2.8	Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{DS(on)max} V _{GS} = 10 V	3.8			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} I _D = 1.9 A	1.2	2.3		S
C _{iss}	Input Capacitance	V _{DS} = 25 V f = 1 MHz V _{GS} = 0		400	520	pF
C _{oss}	Output Capacitance			62	84	pF
C _{rss}	Reverse Transfer Capacitance			7.5	10	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 250\text{ V}$ $I_D = 1.9\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		11	17	ns
t_r	Rise Time			8	12	ns
Q_g	Total Gate Charge	$V_{DD} = 400\text{ V}$ $I_D = 3.8\text{ A}$ $V_{GS} = 10\text{ V}$		15	21	nC
Q_{gs}	Gate-Source Charge			6.5		nC
Q_{gd}	Gate-Drain Charge			5		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400\text{ V}$ $I_D = 3.8\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		8	12	ns
t_f	Fall Time			5	9	ns
t_c	Cross-over Time			14	20	ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				3.8	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				15.2	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 3.8\text{ A}$ $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 3.8\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		245		ns
Q_{rr}	Reverse Recovery Charge			980		μC
I_{RRM}	Reverse Recovery Current			8		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

Fig. 1: Unclamped Inductive Load Test Circuit

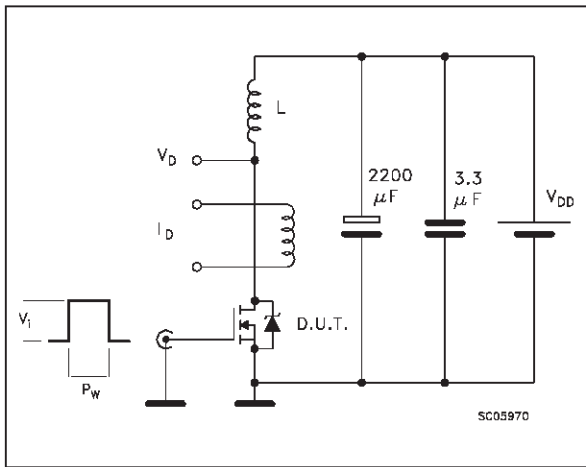


Fig. 2: Unclamped Inductive Waveform

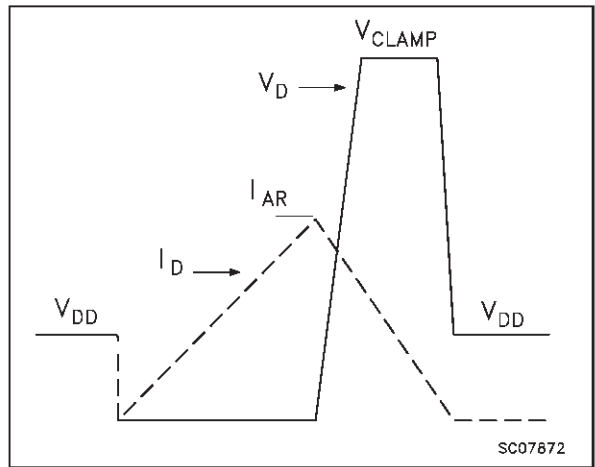


Fig. 3: Switching Times Test Circuits For Resistive Load

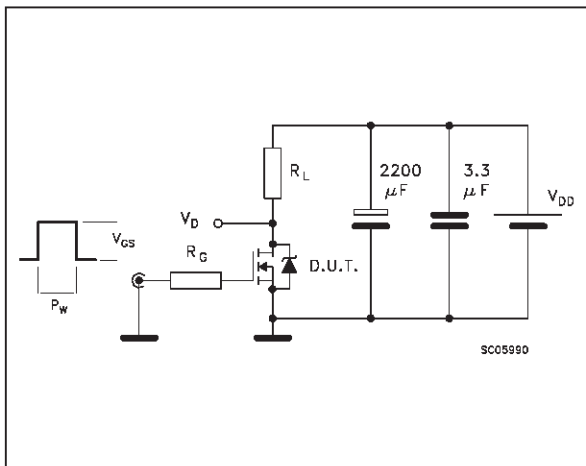


Fig. 4: Gate Charge test Circuit

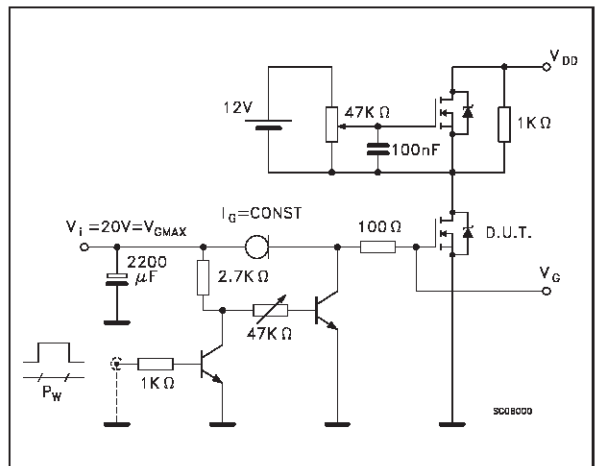
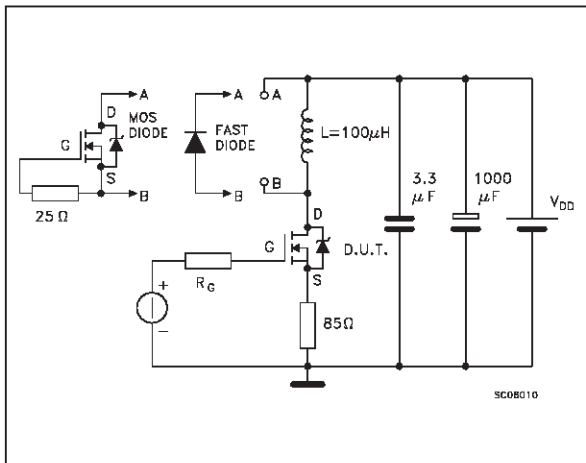
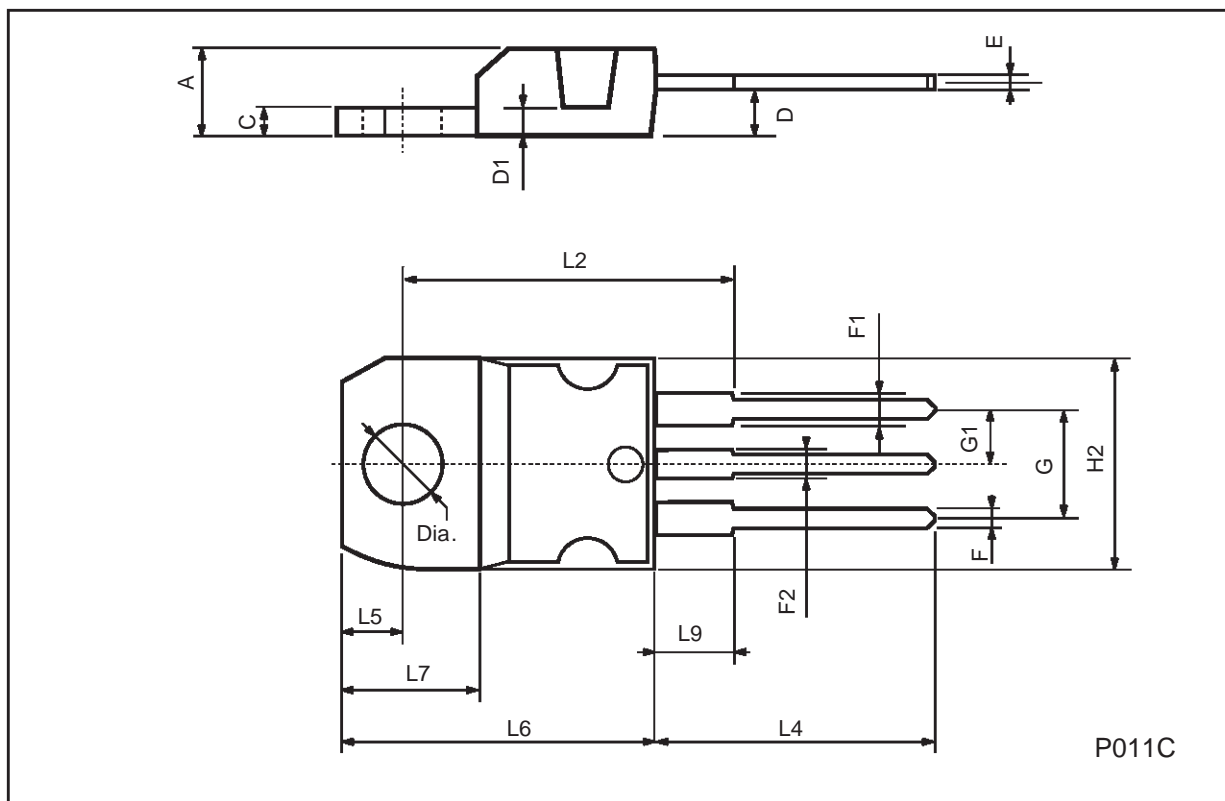


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



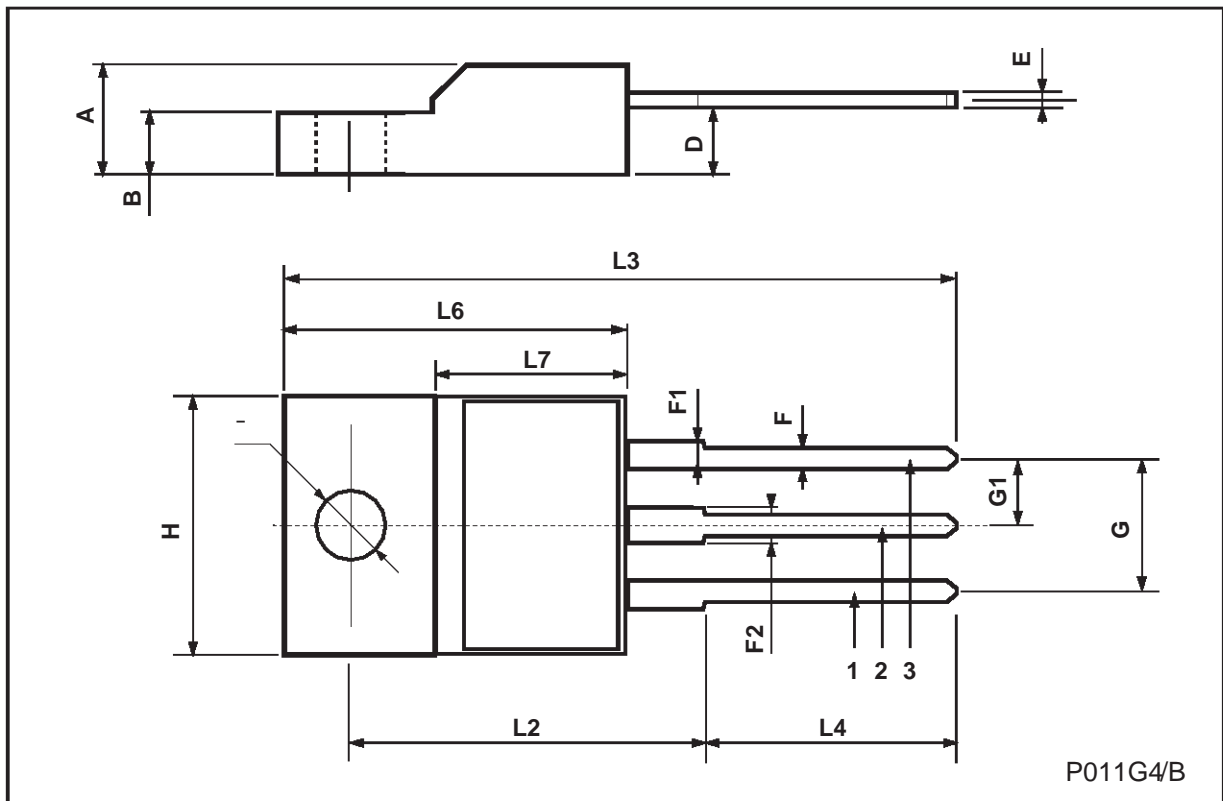
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



TO-220FP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



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