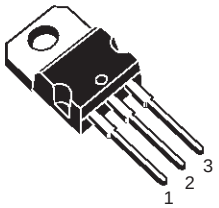
STP80PF55

P-CHANNEL 55V - 0.016 Ω - 80A TO-220
STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STB80PF55	55 V	< 0.018 Ω	80 A

- TYPICAL $R_{DS}(on)$ = 0.016 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION



TO-220

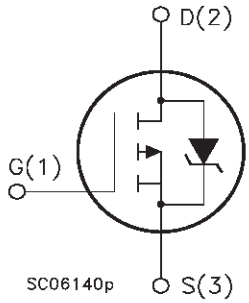
DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- MOTOR CONTROL
- DC-DC & DC-AC CONVERTERS

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	55	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	55	V
V_{GS}	Gate- source Voltage	± 16	V
$I_{D(*)}$	Drain Current (continuos) at T_C = 25°C	80	A
I_D	Drain Current (continuos) at T_C = 100°C	57	A
I_{DM}(•)	Drain Current (pulsed)	320	A
P_{tot}	Total Dissipation at T_C = 25°C	300	W
	Derating Factor	2	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	1.4	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Max. Operating Junction Temperature		

(•) Pulse width limited by safe operating area
(*) Current Limited by Package

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed
(1) $I_{SD} \leq 40A$, $di/dt \leq 300A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX.}$
(2) Starting T_j = 25 °C, I_D = 80A, V_{DD} = 40V

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	Typ	300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	55			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 16 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 40 A		0.016	0.018	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 40 A		32		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		5500 1130 600		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 25 V I_D = 40 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 3)		35 190		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 25 V I_D = 80 A V_{GS}= 10V		190 27 65	258	nC nC nC

SWITCHING OFF (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 25 V I_D = 40 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 3)		165 80		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{clamp} = 40 V I_D = 80 A R_G = 4.7 Ω V_{GS} = 10 V (Inductive Load, Figure 5)		60 40 85		ns ns ns

SOURCE DRAIN DIODE (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				80 320	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 80 A V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 80 A di/dt = 100A/µs V_{DD} = 25 V T_j = 150°C (see test circuit, Figure 5)		110 495 9		ns nC A

(*) Pulse width [300 µs, duty cycle 1.5 %.
(•) Pulse width limited by T_{JMAX}

Fig. 1: Unclamped Inductive Load Test Circuit

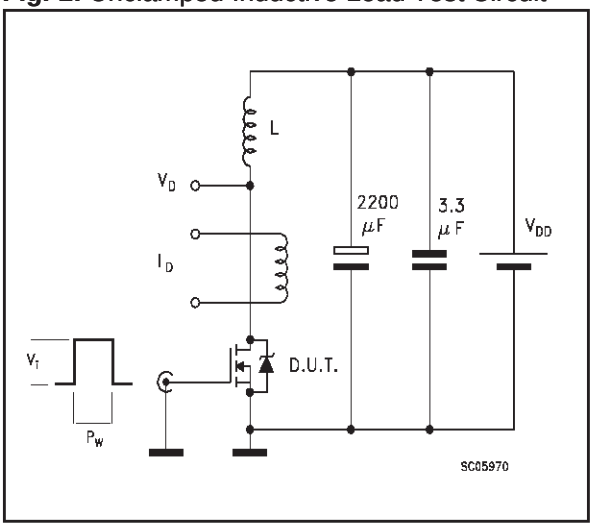


Fig. 2: Unclamped Inductive Waveform

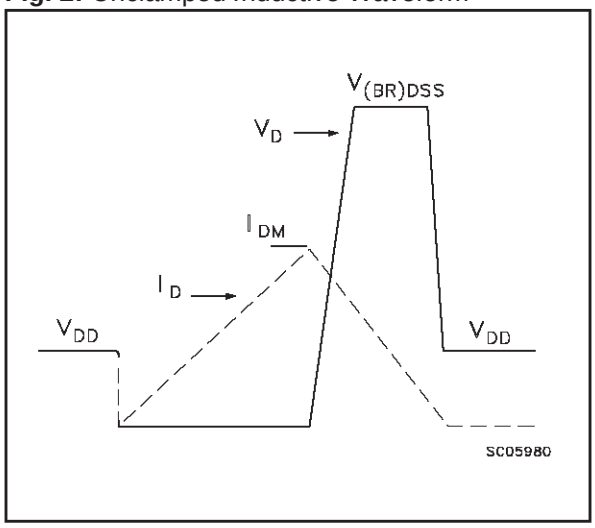


Fig. 3: Switching Times Test Circuits For Resistive Load

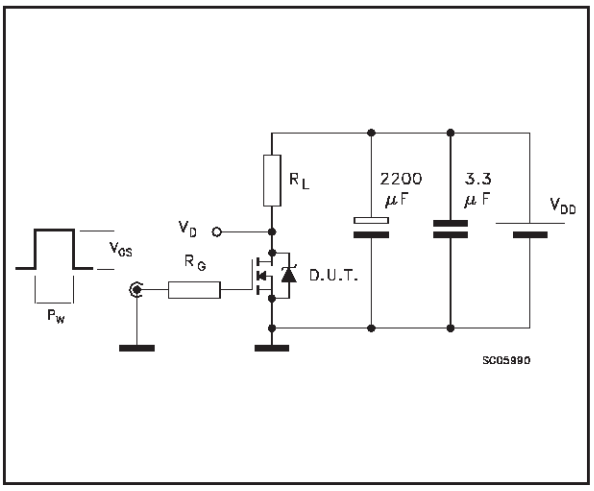


Fig. 4: Gate Charge test Circuit

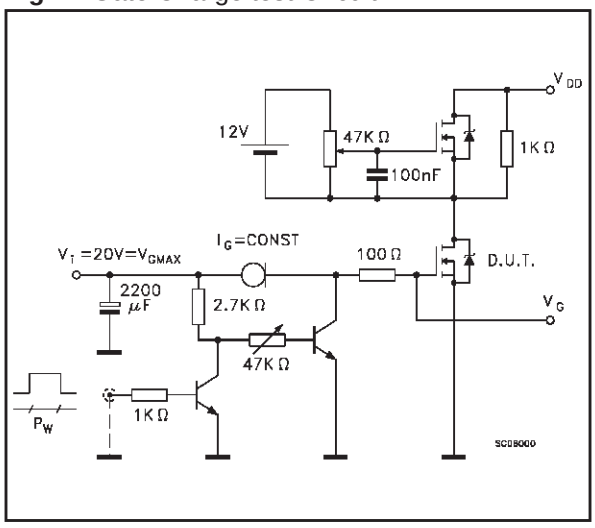
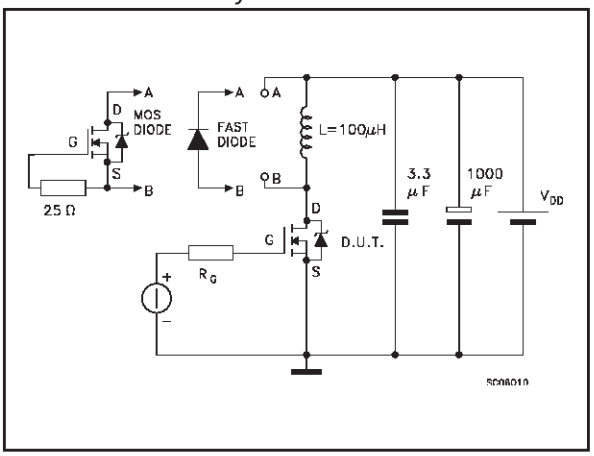


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151