

STS17NF3LL N-CHANNEL 30V - 0.0045Ω - 17A SO-8 STripFET™ MOSFET FOR DC-DC CONVERSION

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	ID		
STS17NF3LL	30 V	< 0.0055Ω	17 A		
$TVDICAL B_{-1}(ap) = 0.004EO$					

- TYPICAL $R_{DS}(on) = 0.0045\Omega$
- OPTIMAL R_{DS(ON)} x Q_g TRADE-OFF @4.5V
 CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- SWITCHING LOSSES REDUCED

DESCRIPTION

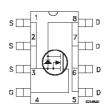
This application specific Power MOSFET is the third generation of STMicroelectronics unique "Single Feature SizeTM" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. Such features make it the best choice in high efficiency DC-DC converters for Telecom and Computer industries.

APPLICATIONS

- DC-DC CONVERTERS FOR TELECOM AND NOTEBOOK CPU CORE
- SYNCHRONOUS RECTIFIER

SO-8

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage ($V_{GS} = 0$)	30	V
V _{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	30	V
V _{GS}	Gate- source Voltage	± 18	V
۱ _D	Drain Current (continuous) at T _A = 25°C Drain Current (continuous) at T _A = 100°C	17 12	A A
I _{DM} (1)	Drain Current (pulsed)	68	А
Ртот	Total Dissipation at $T_A = 25^{\circ}C$	3.2	W

(•) Pulse width limited by safe operating area

STS17NF3LL

THERMAL DATA

Rthj-amb	(*) Thermal Resistance Junction-ambient Max	47	°C/W
Rthj-lead	Thermal Resistance Junction-leads Max	16	°C/W
Tj	Max. Operating Junction Temperature	– 55 to 175	°C
T _{stg}	Storage Temperature	- 55 10 175	

(*) When mounted on 1 inch $\,$ FR4 Board, 2oz of Cu, t \leq 10 sec.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$	30			V
IDSS	Zero Gate Voltage	V _{DS} = Max Rating			1	μΑ
	Drain Current ($V_{GS} = 0$)	V_{DS} = Max Rating, T_{C} = 125 °C			10	μΑ
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	$V_{GS} = \pm 18V$			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
R _{DS(on)}	Static Drain-source On	$V_{GS} = 10 \text{ V}, I_D = 8.5 \text{ A}$		0.0045	0.0055	Ω
	Resistance	V_{GS} = 4.5 V, I _D = 8.5 A		0.0055	0.007	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 15V , I _D = 8.5 A		TBD		S
Ciss	Input Capacitance	$V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0$		2160		рF
Coss	Output Capacitance			614		pF
C _{rss}	Reverse Transfer Capacitance			98		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
td(on)	Turn-on Delay Time	$V_{DD} = 15 \text{ V}, \text{I}_{D} = 6\text{A}$		23.5		ns
tr	Rise Time	$\label{eq:G} \begin{array}{l} R_{G} = 4.7 \Omega \; V_{GS} = 4.5 V \\ (\text{see test circuit, Figure 1}) \end{array}$		39		ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$\label{eq:VDD} \begin{array}{l} V_{DD} = 24 \ V, I_{D} = 17 \ A, \\ V_{GS} = 4.5 \ V \\ (\text{see test circuit, Figure 2}) \end{array}$		26 7 12	35	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
td(off) t _f	Turn-off-Delay Time Fall Time			47.5 37		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain Current				17	A
I _{SDM} (1)	Source-drain Current (pulsed)				68	А
V _{SD} (2)	Forward On Voltage	I _{SD} = 17 A, V _{GS} = 0			1.2	V
t _{rr} Q _{rr} IRRM	Reverse Recovery Time Reverse Recovery ChargeReverse Recovery Current	$\begin{split} I_{SD} &= 12.5 \text{ A, di/dt} = 100 \text{A}/\mu\text{s,} \\ V_{DD} &= 15 \text{ V, } \text{T}_{j} = 150^{\circ}\text{C} \\ (\text{see test circuit, Figure 3}) \end{split}$		39 45 2.3		ns nC A

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

57.

Fig. 1: Switching Times Test Circuit For Resistive Load

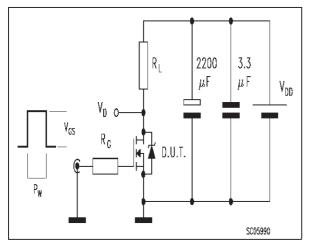


Fig. 3: Test Circuit For Diode Recovery Behaviour

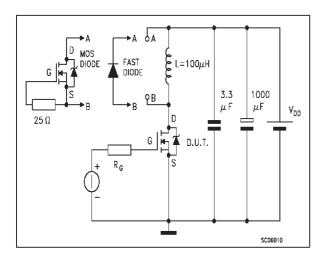
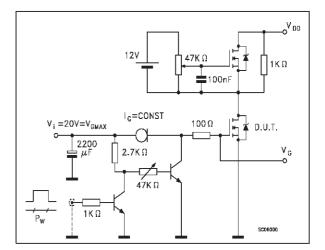


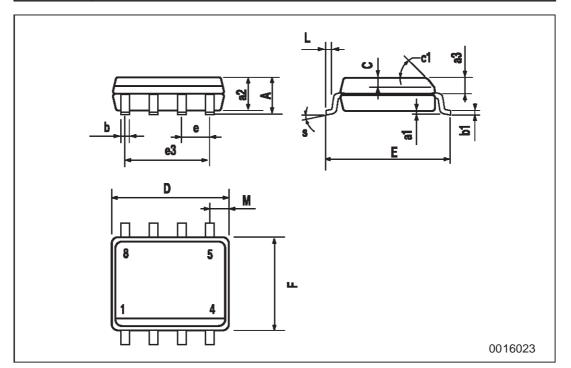
Fig. 2: Gate Charge test Circuit



57.

DIM.		mm		inch							
Dilai.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.					
А			1.75			0.068					
a1	0.1		0.25	0.003		0.009					
a2			1.65			0.064					
a3	0.65		0.85	0.025		0.033					
b	0.35		0.48	0.013		0.018					
b1	0.19		0.25	0.007		0.010					
С	0.25		0.5	0.010		0.019					
c1		-	45	(typ.)							
D	4.8		5.0	0.188		0.196					
E	5.8		6.2	0.228		0.244					
е		1.27			0.050						
e3		3.81			0.150						
F	3.8		4.0	0.14		0.157					
L	0.4		1.27	0.015		0.050					
М			0.6			0.023					
S		-		max.)	8 (max.)						

SO-8 MECHANICAL DATA



<u>57.</u>

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics. © The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved STMicroelectronics GROUP OF COMPANIES Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco Singapore - Spain - Sweden - Switzerland - United Kingdom - United States. © http://www.st.com

57.