

N-CHANNEL 30V - 0.016 Ω - 9A SO-8 LOW GATE CHARGE STripFET™ II POWER MOSFET

ТҮРЕ	VDSS	RDS(on)	ID
STS9NF3LL	30 V	<0.019 Ω	9 A

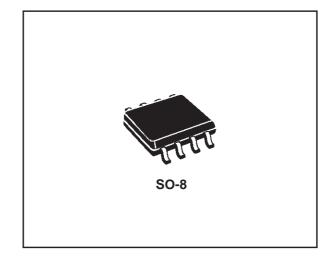
- TYPICAL $R_{DS}(on) = 0.016 \Omega$
- OPTIMAL R_{DS}(on) x Qg TRADE-OFF @ 4.5V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

DESCRIPTION

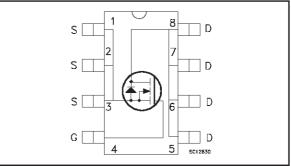
This application specific Power MOSFET is the second generation of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

APPLICATIONS

 SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PCs



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	30	V
V _{GS}	Gate- source Voltage	± 16	V
Ι _D	Drain Current (continuos) at $T_C = 25^{\circ}C$	9	A
ID	Drain Current (continuos) at T _C = 100°C	5.6	A
I _{DM} (●)	Drain Current (pulsed)	36	A
Ptot	Total Dissipation at $T_C = 25^{\circ}C$	2.5	W

(•) Pulse width limited by safe operating area.

November 2001

THERMAL DATA

Rthj-amb (*)Thermal Resistance Junction-ambient Tj Maximum Operating Junction Temperature Tstg Storage Temperature	Max	50 150 -55 to 150	°C/W °C °C	
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 $^{(\ast)}$ When mounted on FR-4 board with 0.5 in^2 pad of Cu.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25 \ ^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _(BR) DSS	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$	30			V
IDSS	Zero Gate Voltage Drain Current (V _{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_{C} = 125°C			1 10	μΑ μΑ
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	$V_{GS} = \pm 16 V$			±100	nA

ON (*)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$	I _D = 250 μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V V _{GS} = 4.5 V	I _D = 4.5 A I _D = 4.5 A		0.016 0.019	0.019 0.022	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V_{DS} =15 V I_D = 4 A		12.5		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		800 250 60		pF pF pF



ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
td(on) t _r	Turn-on Delay Time Rise Time	$ \begin{array}{ll} V_{DD} = 15 \ V & I_D = 4.5 \ A \\ R_G = 4.7 \ \Omega & V_{GS} = 4.5 \ V \\ (\text{Resistive Load, Figure 1}) \end{array} $		18 32		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 15 V I _D = 9 A V _{GS} = 5 V (see test circuit, Figure 2)		12.5 3.2 4.5	17	nC nC nC

SWITCHING OFF

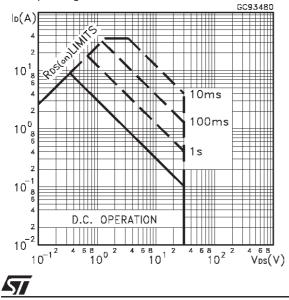
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	$ \begin{array}{ll} V_{DD} = 15 \ V & I_D = 4.5 \ A \\ R_G = 4.7 \Omega, & V_{GS} = 4.5 \ V \\ (\text{Resistive Load, Figure 3}) \end{array} $		21 11		ns ns

SOURCE DRAIN DIODE

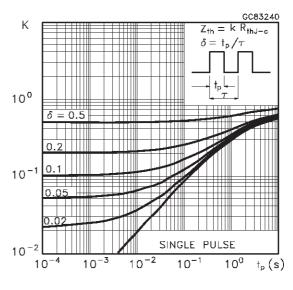
Symbol	Parameter Test Conditions		conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (●)	Source-drain Current Source-drain Current (pulsed)					9 36	A A
V _{SD} (*)	Forward On Voltage	I _{SD} = 9 A	$V_{GS} = 0$			1.2	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 9 A V _{DD} = 15 V (see test circu	di/dt = 100A/µs T _j = 150°C uit, Figure 3)		23 17 1.5		ns nC A

(*)Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

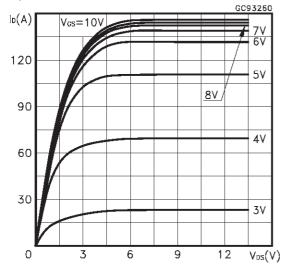
Safe Operating Area



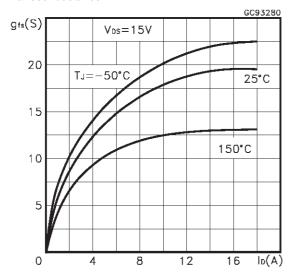
Thermal Impedance



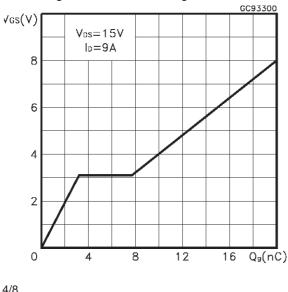
Output Characteristics

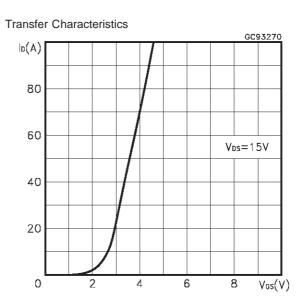


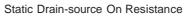
Transconductance

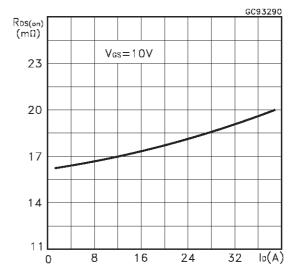


Gate Charge vs Gate-source Voltage

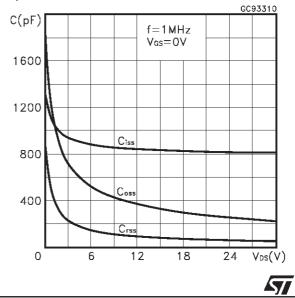


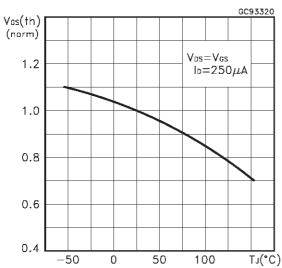






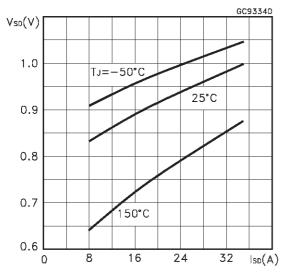
Capacitance Variations



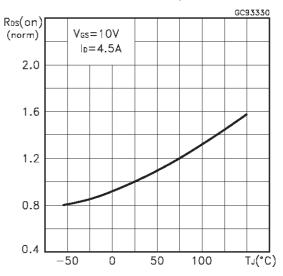


Normalized Gate Threshold Voltage vs Temperature

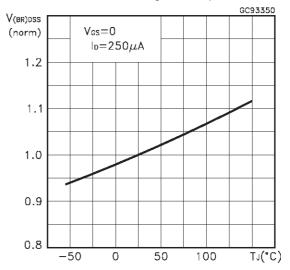
Source-drain Diode Forward Characteristics



Normalized on Resistance vs Temperature



Normalized Breakdown Voltage vs Temperature.



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Fig. 1: Switching Times Test Circuits For Resistive Load

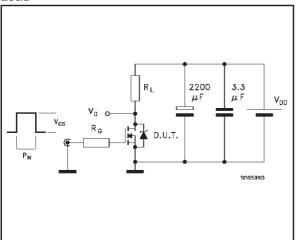


Fig. 3: Test Circuit For Diode Recovery Behaviour

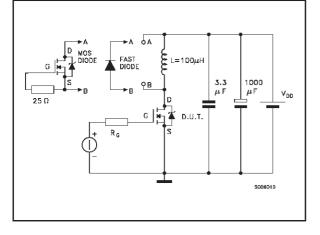
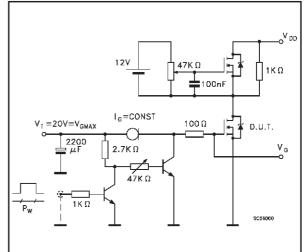


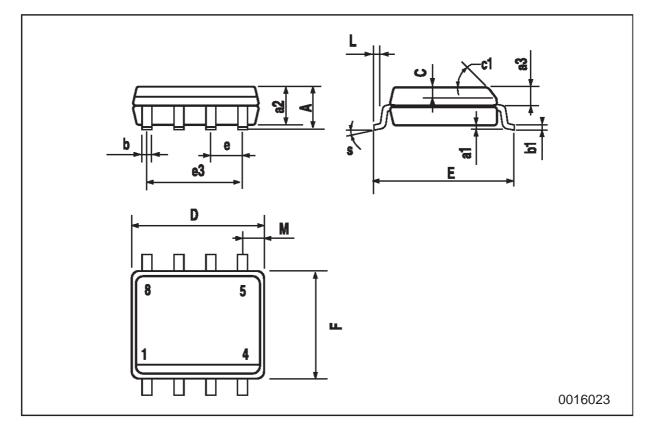
Fig. 2: Gate Charge test Circuit



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DIM.		mm			inch	
DIM.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1			45	(typ.)		
D	4.8		5.0	0.188		0.196
Е	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023
S			8 (r	nax.)		

SO-8 MECHANICAL DATA



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