

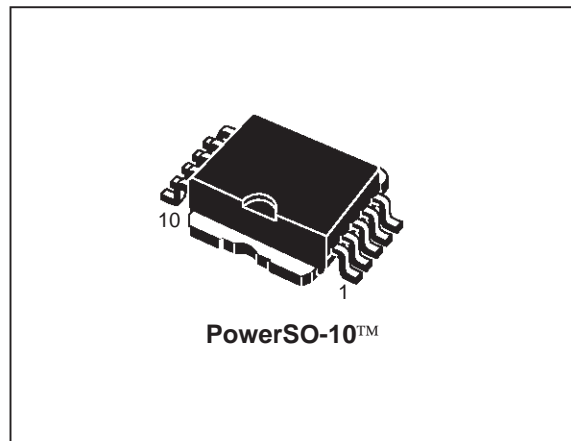
SINGLE CHANNEL HIGH SIDE SOLID STATE RELAY

TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN610SP	10m Ω	45A	36 V

- OUTPUT CURRENT: 45 A
- CMOS COMPATIBLE INPUT
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST:
 - LOSS OF GROUND AND LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (*)

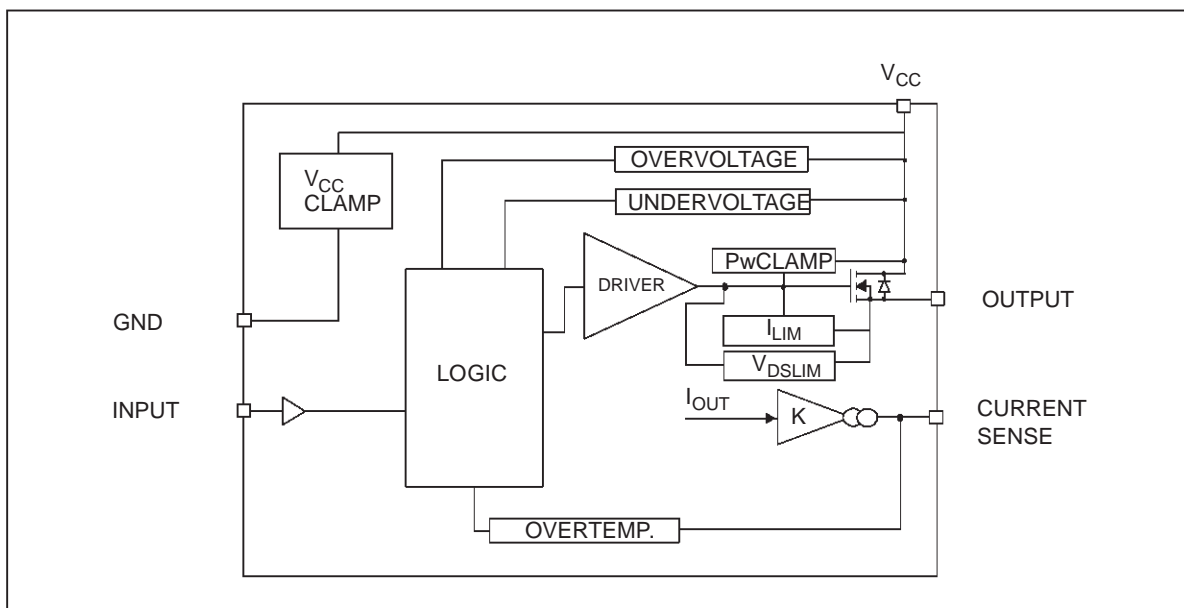
DESCRIPTION

The VN610SP is a monolithic device made using STMicroelectronics VIPower M0-3 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin



voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio). Active current limitation combined with thermal shut-down and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

BLOCK DIAGRAM

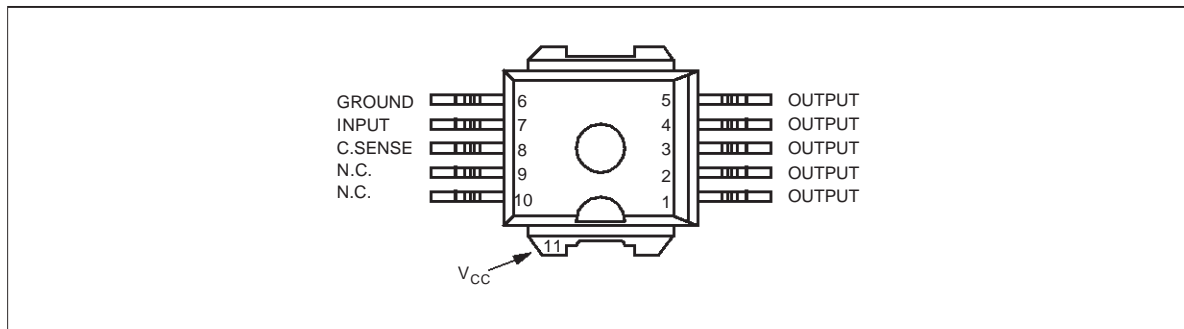


(*) See application schematic at page 9

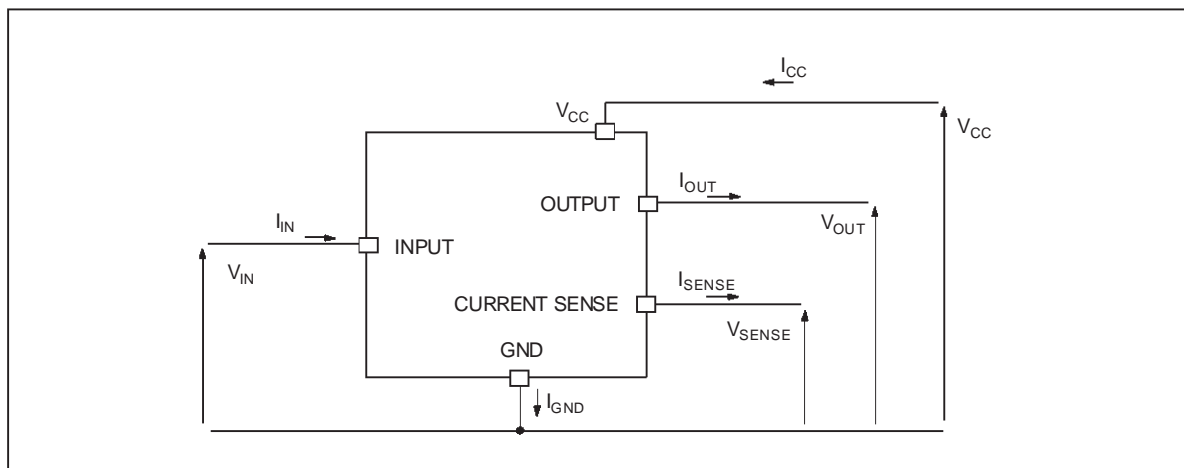
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-50	A
I_{IN}	DC input current	+/- 10	mA
$V_{CSSENSE}$	Current sense maximum voltage	-3 +15	V V
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5Ω; C=100pF)		
	- INPUT	4000	V
	- CURRENT SENSE	2000	V
	- OUTPUT	5000	V
	- V_{CC}	5000	V
E_{MAX}	Maximum Switching Energy (L=0.13mH; R _L =0Ω; V _{bat} =13.5V; T _{jstart} =150°C; I _L =75A)	510	mJ
P_{TOT}	Power dissipation at T _C ≤25°C	125	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

CONNECTION DIAGRAM (TOP VIEW)



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX)	1	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (MAX)	51 (*)	°C/W

(*) When mounted on a standard single-sided FR-4 board with 50mm² of Cu (at least 35µm thick).

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C; unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CC}	Operating supply voltage		5.5	13	36	V
V _{USD}	Undervoltage shutdown		3	4	5.5	V
V _{OV}	Overvoltage shutdown	(See Note 1)	36			V
R _{ON}	On state resistance	I _{OUT} =15A; T _j =25°C I _{OUT} =15A; T _j =150°C I _{OUT} =9A; V _{CC} =6V			10 20 35	mΩ mΩ mΩ
V _{clamp}	Clamp Voltage	I _{CC} =20 mA (see note 1)	41	48	55	V
I _S	Supply current	Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V Off State; V _{CC} =13V; V _{IN} =V _{OUT} =0V; T _j =25°C On State; V _{CC} =13V; V _{IN} =5V; I _{OUT} =0A R _{SENSE} =3.9K		10 10	25 20 5	µA µA mA
I _{L(off1)}	Off State Output Current	V _{IN} =V _{OUT} =0V	0		50	µA
I _{L(off2)}	Off State Output Current	V _{IN} =0V; V _{OUT} =3.5V	-75		0	µA
I _{L(off3)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =125°C			5	µA
I _{L(off4)}	Off State Output Current	V _{IN} =V _{OUT} =0V; V _{CC} =13V; T _j =25°C			3	µA

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on delay time	R _L =0.87Ω		50		µs
t _{d(off)}	Turn-off delay time	R _L =0.87Ω		50		µs
(dV _{OUT} /dt) _{on}	Turn-on voltage slope	R _L =0.87Ω		See relative diagram		V/µs
(dV _{OUT} /dt) _{off}	Turn-off voltage slope	R _L =0.87Ω		See relative diagram		V/µs

PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I _{lim}	DC Short circuit current	V _{CC} =13V 5.5V<V _{CC} <36V	45	75	120 120	A A
T _{TSD}	Thermal shutdown temperature		150	175	200	°C
T _R	Thermal reset temperature		135			°C
T _{HYST}	Thermal hysteresis		7	15		°C
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} =2A; V _{IN} =0; L=6mH	V _{CC} -41	V _{CC} -48	V _{CC} -55	V
V _{ON}	Output voltage drop limitation	I _{OUT} =1.5A; T _j = -40°C...+150°C		50		mV

ELECTRICAL CHARACTERISTICS (continued)
CURRENT SENSE ($9V \leq V_{CC} \leq 16V$) (See Figure 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	$I_{OUT}=1.5A$; $V_{SENSE}=0.5V$; $T_j = -40^{\circ}C \dots 150^{\circ}C$	3300	4400	6000	
dK_1/K_1	Current Sense Ratio Drift	$I_{OUT}=1.5A$; $V_{SENSE}=0.5V$; $T_j = -40^{\circ}C \dots 150^{\circ}C$	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	$I_{OUT}=15A$; $V_{SENSE}=4V$; $T_j = -40^{\circ}C$ $T_j = 25^{\circ}C \dots 150^{\circ}C$	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current Sense Ratio Drift	$I_{OUT}=15A$; $V_{SENSE}=4V$; $T_j = -40^{\circ}C$ $T_j = 25^{\circ}C \dots 150^{\circ}C$	-6		+6	%
K_3	I_{OUT}/I_{SENSE}	$I_{OUT}=45A$; $V_{SENSE}=4V$; $T_j = -40^{\circ}C$ $T_j = 25^{\circ}C \dots 150^{\circ}C$	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current Sense Ratio Drift	$I_{OUT}=45A$; $V_{SENSE}=4V$; $T_j = -40^{\circ}C$ $T_j = 25^{\circ}C \dots 150^{\circ}C$	-6		+6	%
I_{SENSE0}	Analog sense current	$V_{CC}=6 \dots 16V$; $I_{OUT}=0A$; $V_{SENSE}=0V$; $T_j = -40^{\circ}C \dots 150^{\circ}C$ Off State; $V_{IN}=0V$ On State; $V_{IN}=5V$	0 0		5 10	μA μA
V_{SENSE}	Max analog sense output voltage	$V_{CC}=5.5V$; $I_{OUT}=7.5A$; $R_{SENSE}=10K\Omega$ $V_{CC} > 8V$; $I_{OUT}=15A$; $R_{SENSE}=10K\Omega$	3.5 5			V V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	$V_{CC}=13V$; $R_{SENSE}=3.9K\Omega$		5.5		V
R_{SENSEH}	Analog sense output impedance in overtemperature condition	$V_{CC}=13V$		400		Ω
t_{DSENSE}	Current sense delay reponse	to 90% I_{SENSE} (see note 2)			500	μs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	$V_{IN}=1.25V$	1			μA
V_{IH}	Input high level voltage		3.25			V
I_{IH}	High level input current	$V_{IN}=3.25V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	6	6.8 -0.7	8	V V

Note 1: V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Note 2: current sense signal delay after positive input slope.

Note: Sense pin doesn't have to be left floating.

TRUTH TABLE

VN610SP

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V_{SENSEH}
Undervoltage	L	L	0
	H	L	0
Overvoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	$(T_j < T_{TSD})$ 0
	H	L	$(T_j > T_{TSD})$ V_{SENSEH}
Short circuit to V_{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 1: Switching Characteristics (Resistive load $R_L=0.87\Omega$)

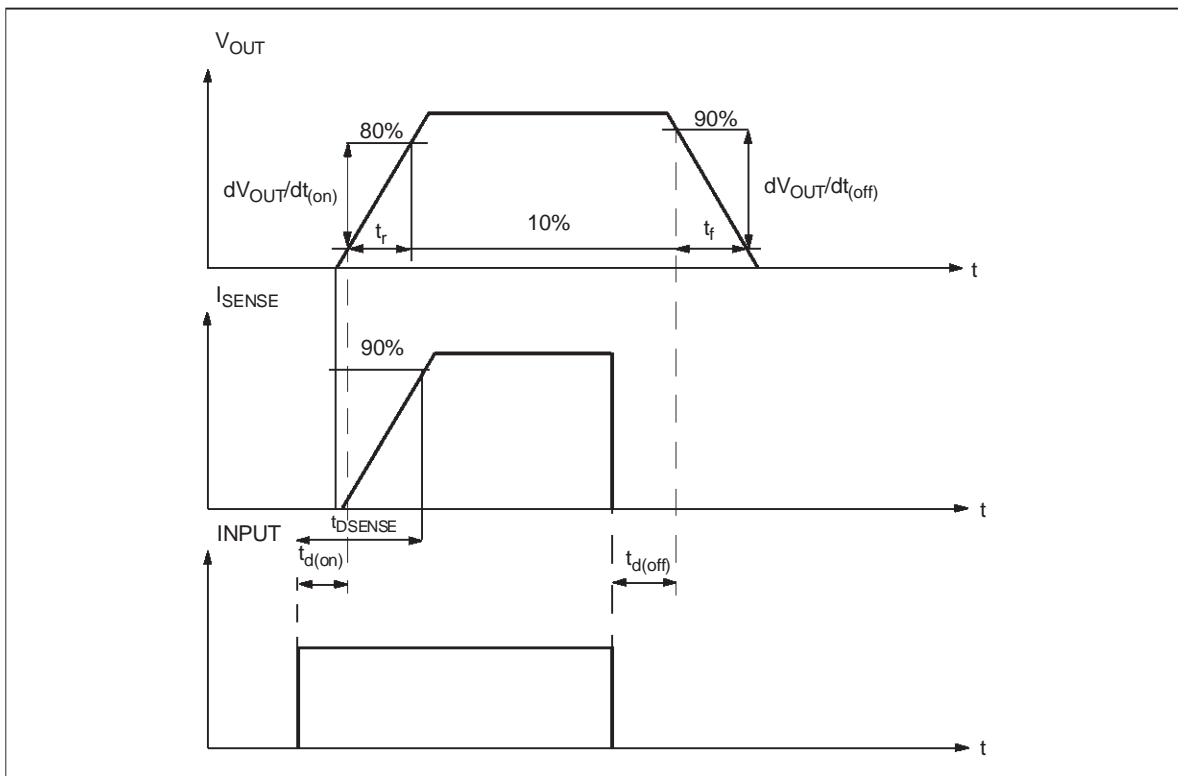


Figure 2: I_{OUT}/I_{SENSE} versus I_{OUT}

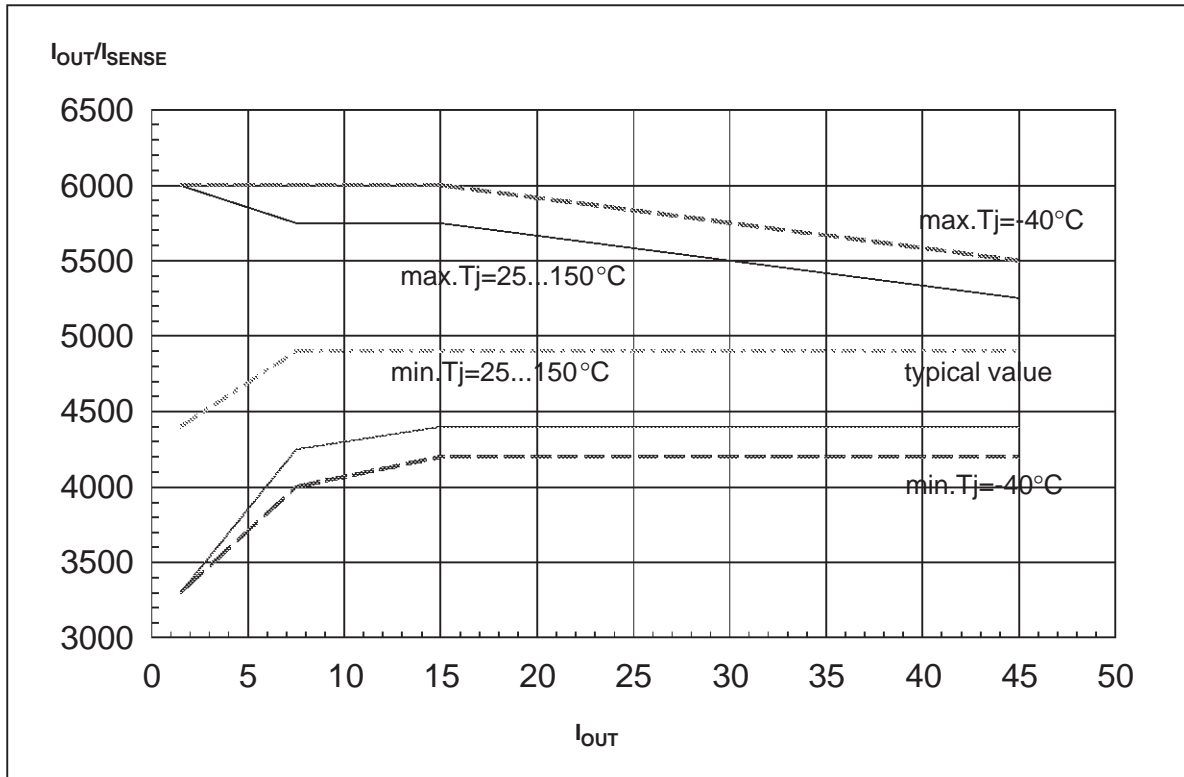
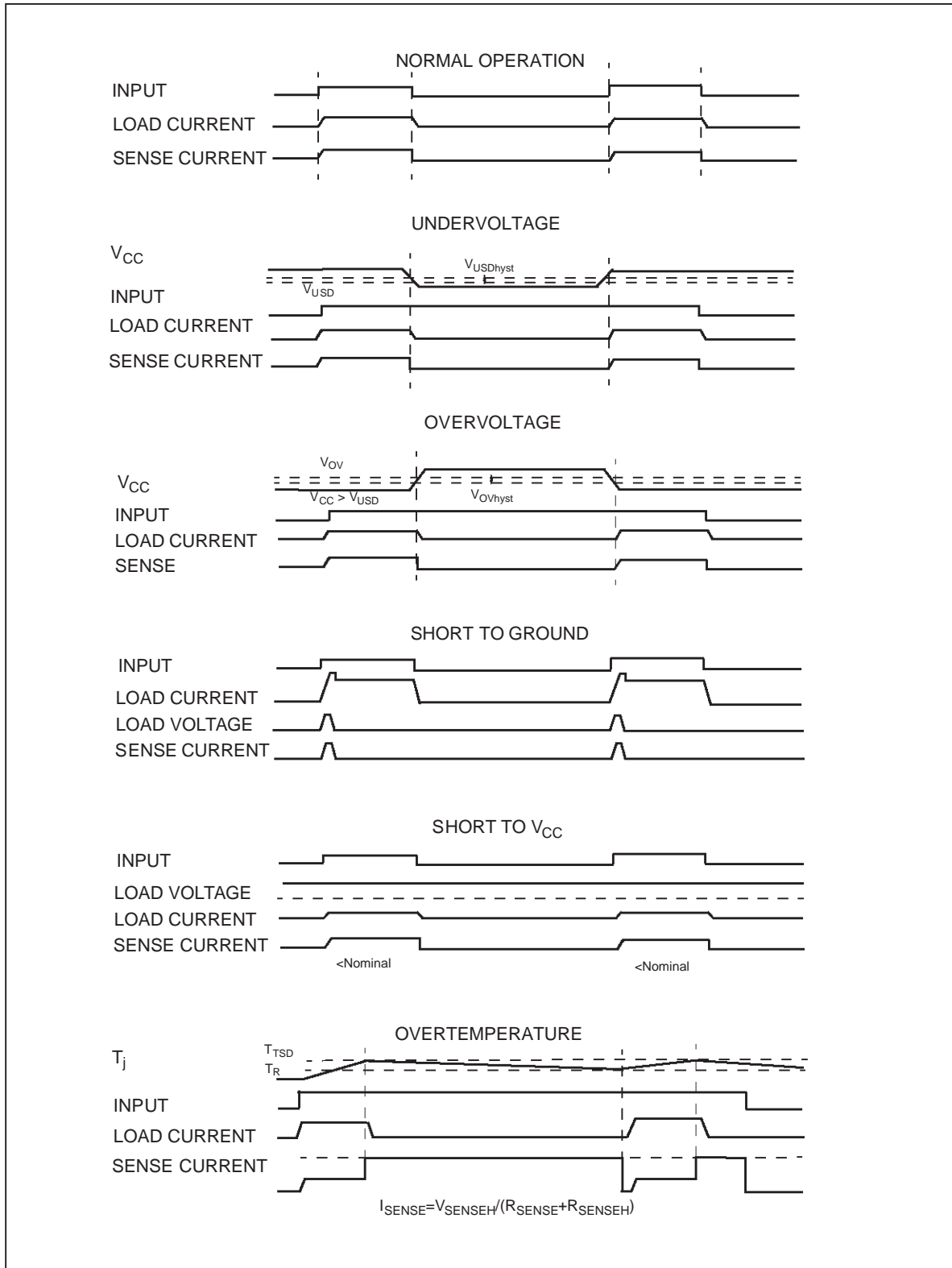
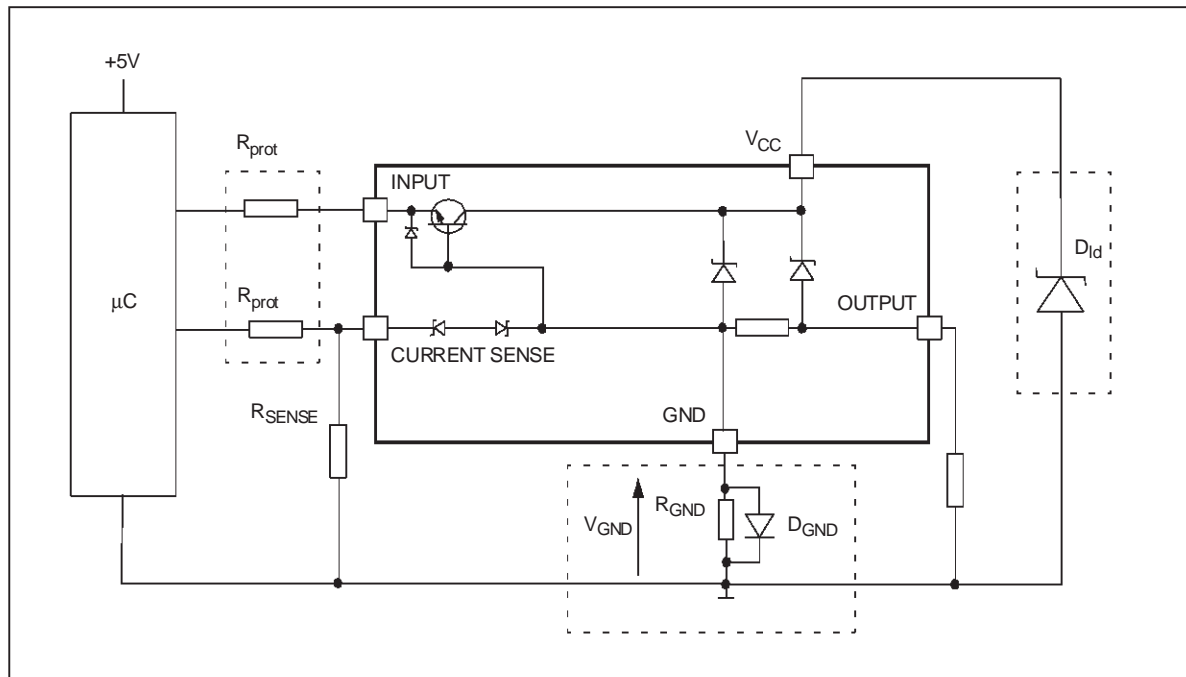


Figure 3: Waveforms



APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND} = 1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j 600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{id} is necessary (Transil or MOV) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

 μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

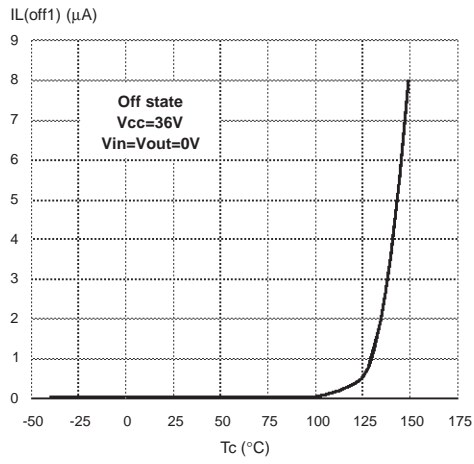
$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

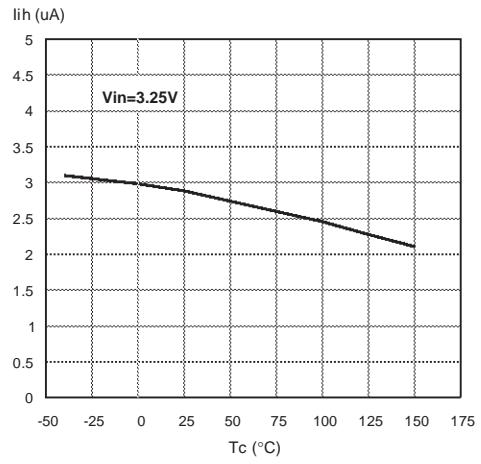
For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$
 $5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$.

Recommended R_{prot} value is 10k Ω .

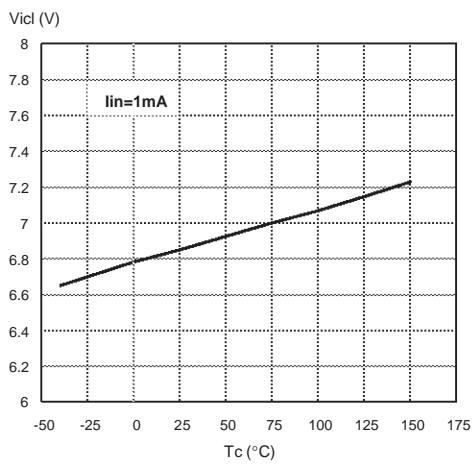
Off State Output Current



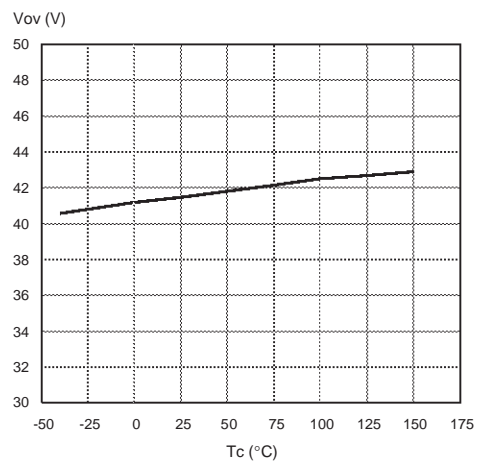
High Level Input Current



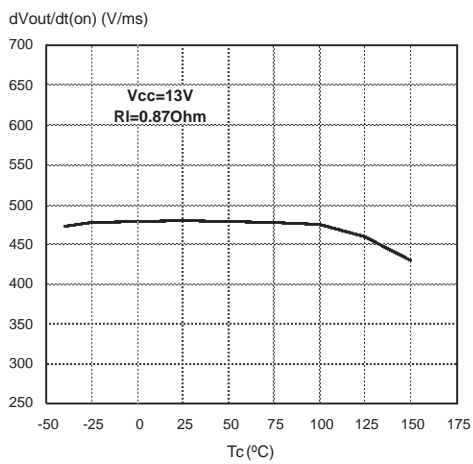
Input Clamp Voltage



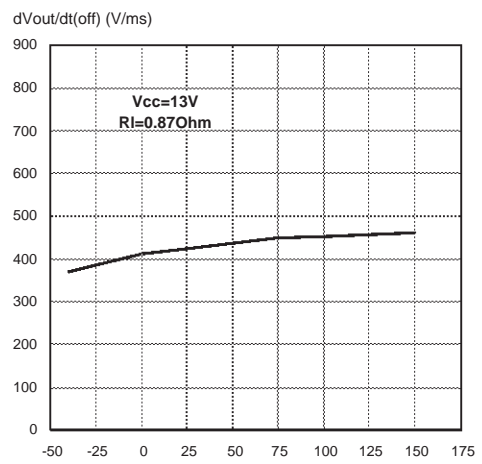
Overvoltage Shutdown



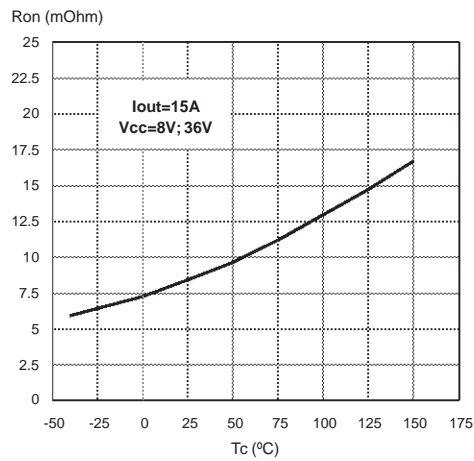
Turn-on Voltage Slope



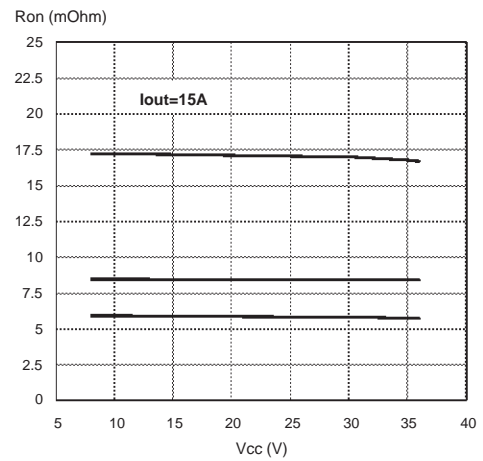
Turn-off Voltage Slope



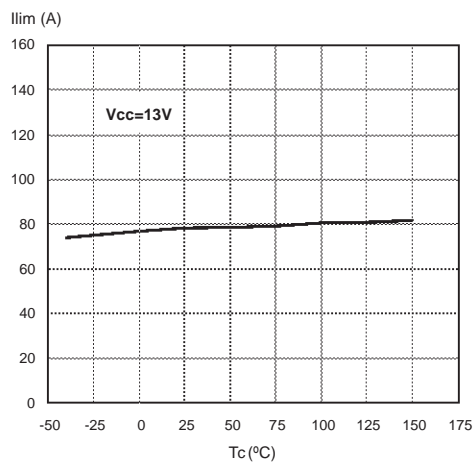
On State Resistance Vs T_{case}



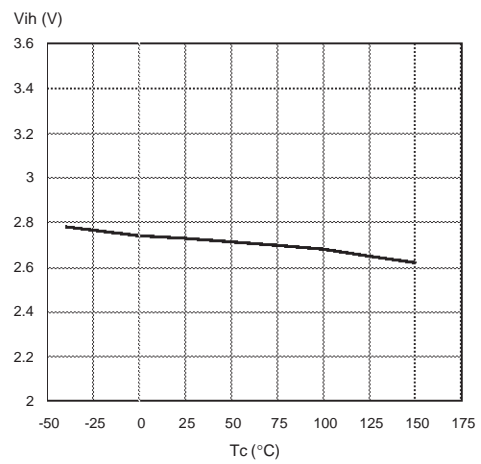
On State Resistance Vs V_{CC}



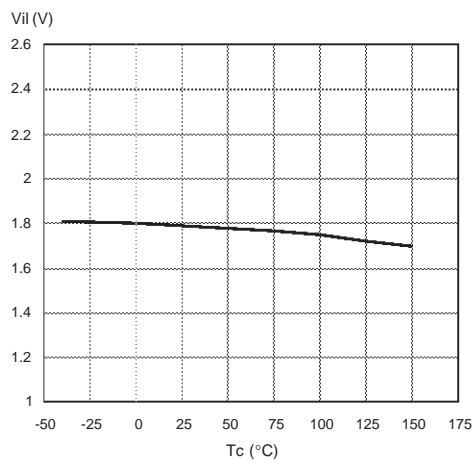
I_{LIM} Vs T_{case}



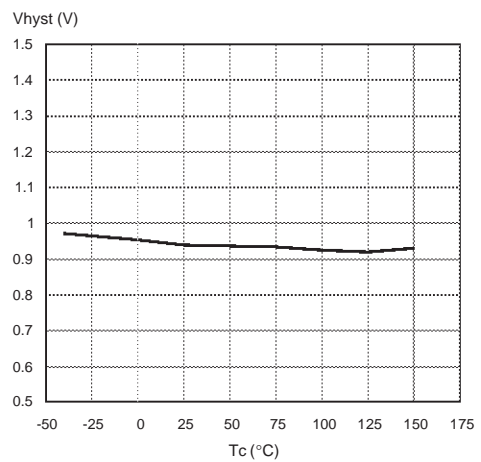
Input High Level



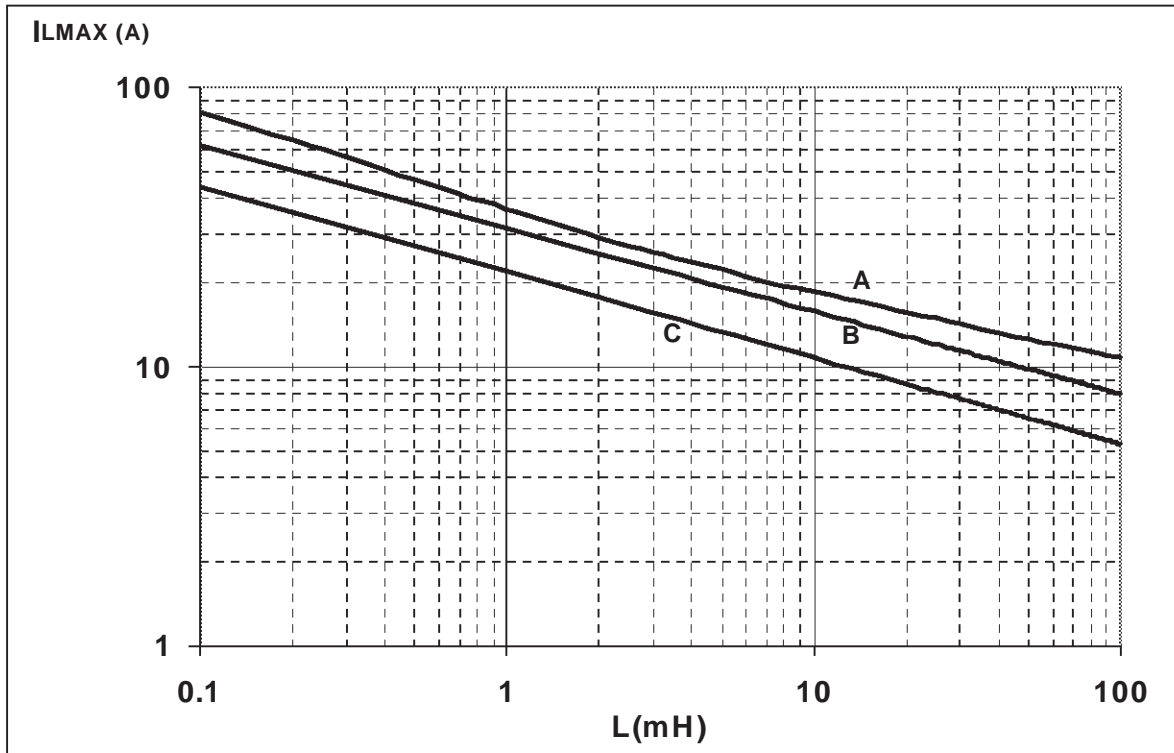
Input Low Level



Input Hysteresis Voltage



Maximum turn off current versus load inductance



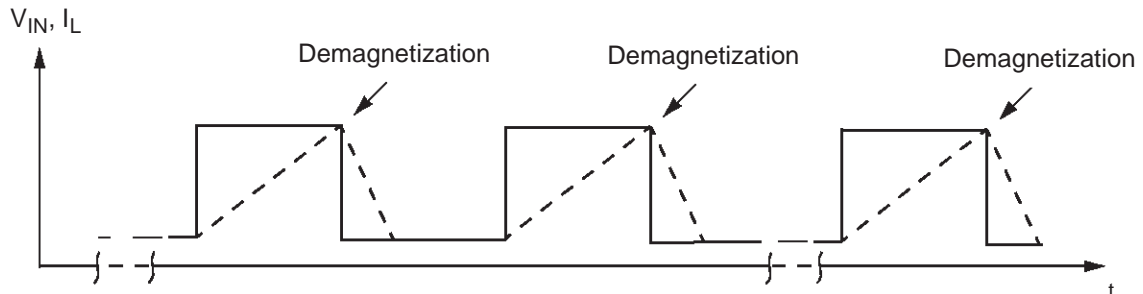
- A = Single Pulse at $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Conditions:

$V_{CC}=13.5V$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

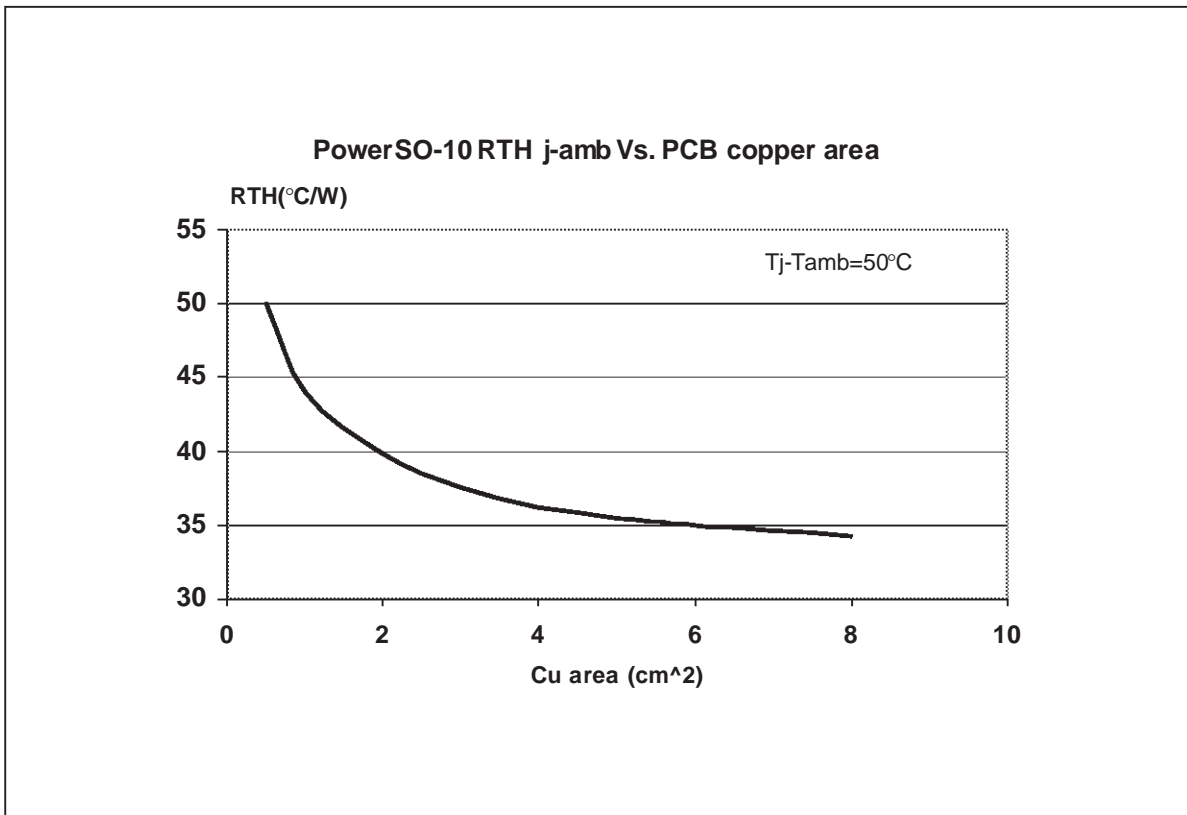


PowerSO-10™ THERMAL DATA

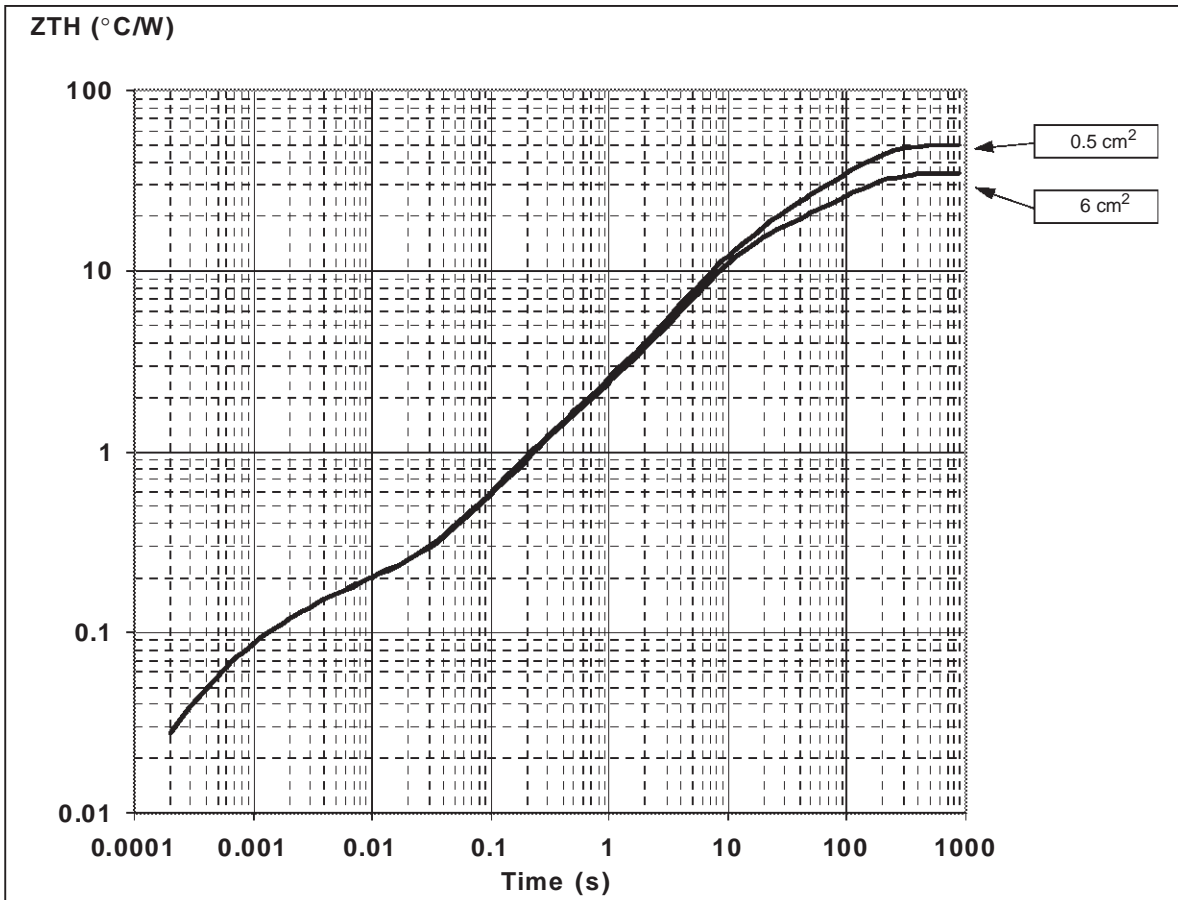
PowerSO-10™ PC Board

Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35 μ m, Copper areas: from minimum pad lay-out to 8cm²).

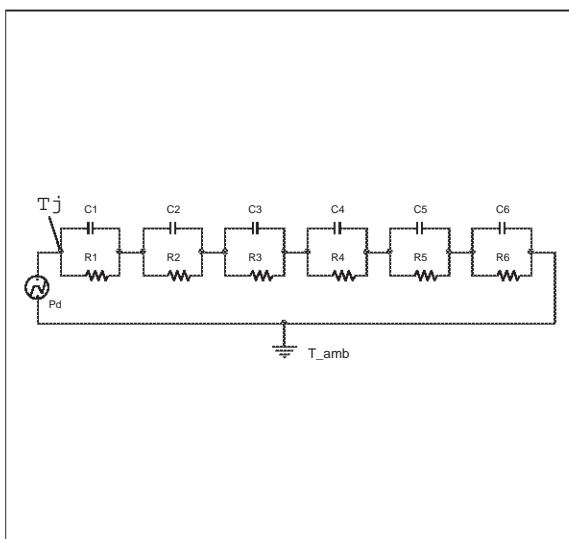
$R_{thj-amb}$ Vs PCB copper area in open box free air condition



Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in PowerSO-10



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

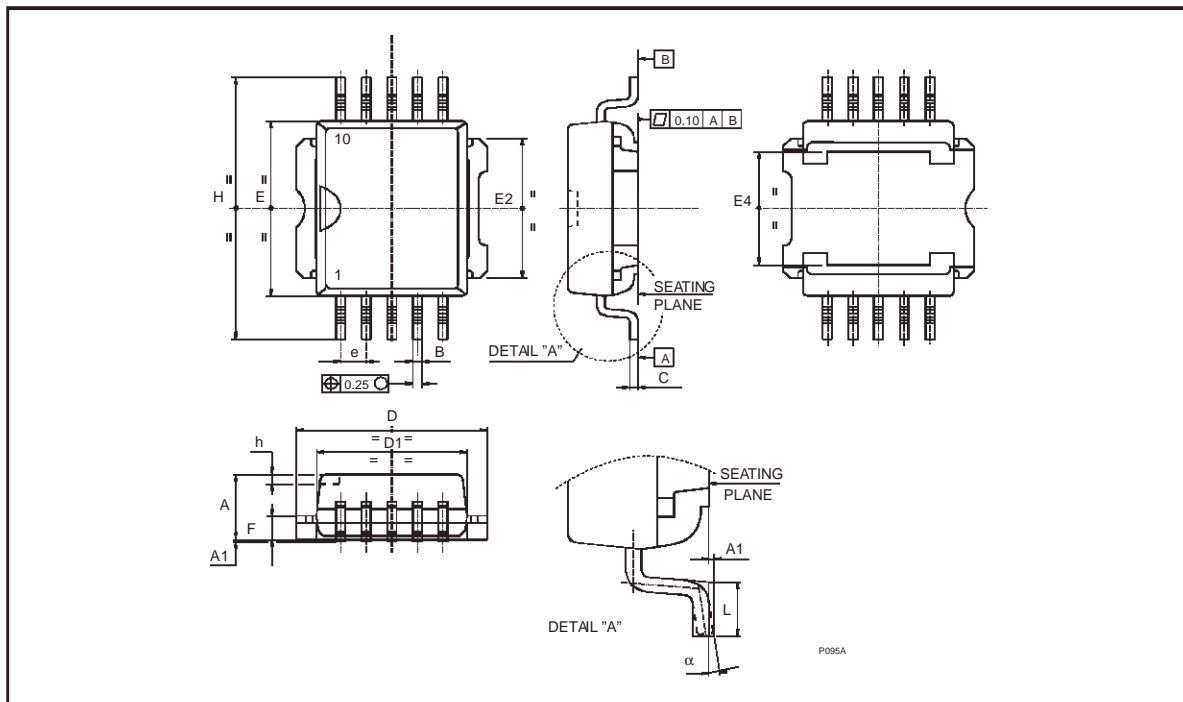
Thermal Parameter

Area/island (cm^2)	0.5	6
R1 ($^{\circ}C/W$)	0.016	
R2 ($^{\circ}C/W$)	0.06	
R3 ($^{\circ}C/W$)	0.08	
R4 ($^{\circ}C/W$)	0.8	
R5 ($^{\circ}C/W$)	12	
R6 ($^{\circ}C/W$)	37	22
C1 ($W.s/^{\circ}C$)	0.002	
C2 ($W.s/^{\circ}C$)	1.00E-02	
C3 ($W.s/^{\circ}C$)	0.04	
C4 ($W.s/^{\circ}C$)	0.3	
C5 ($W.s/^{\circ}C$)	0.75	
C6 ($W.s/^{\circ}C$)	3	5

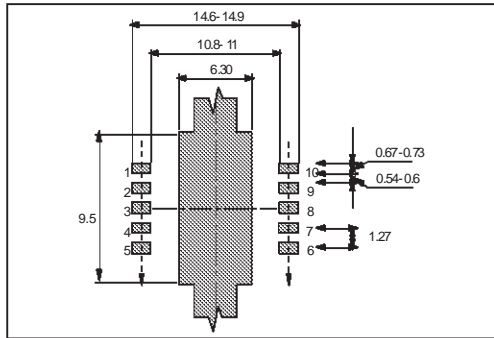
PowerSO-10™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0°		8°	0°		8°
α (*)	2°		8°	2°		8°

(*) Muar only POA P013P



PowerSO-10™ SUGGESTED PAD LAYOUT



TUBE SHIPMENT (no suffix)

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

TAPE AND REEL SHIPMENT (suffix "13TR")

40mm min. Access hole at slant inclination

Full radius

Tape slit in .0125" for tape star: 2.5mm min width

C measured at nub

REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / - 0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

TAPE DIMENSIONS
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

TOP COVER TAPE

User Direction of Feed

End

Start

No components

Components

No components

500mm min

Empty components pockets sealed with cover tape.

User direction of feed

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