



VNP20N07FI VNB20N07/VNV20N07

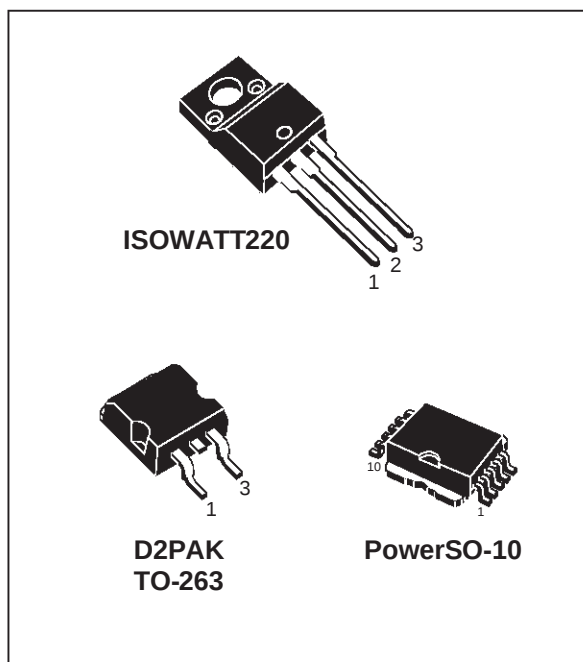
"OMNIFET":
FULLY AUTOPROTECTED POWER MOSFET

TYPE	V _{clamp}	R _{DS(on)}	I _{lim}
VNP20N07FI	70 V	0.05 Ω	20 A
VNB20N07	70 V	0.05 Ω	20 A
VNV20N07	70 V	0.05 Ω	20 A

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

DESCRIPTION

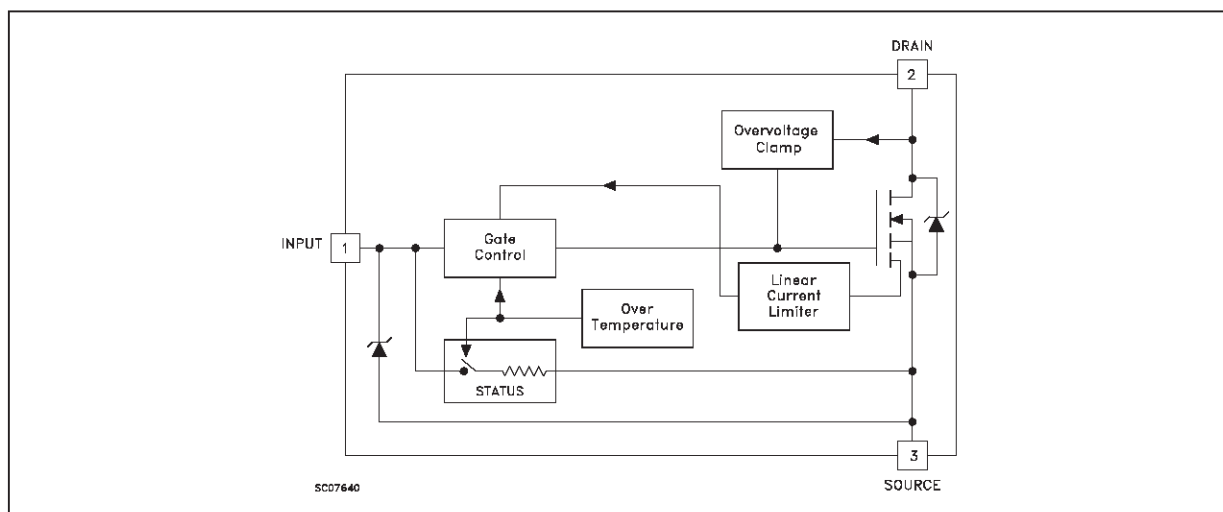
The VNP20N07FI, VNB20N07 and VNV20N07 are monolithic devices made using STMicroelectronics VIPower M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shut-down, linear current limitation and overvoltage clamp protect the chip in harsh



environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

BLOCK DIAGRAM (*)



(*) PowerSO-10 Pin Configuration : INPUT = 6,7,8,9,10; SOURCE = 1,2,4,5; DRAIN = TAB

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value		Unit
		PowerSO-10 D2PAK	ISOWATT220	
V_{DS}	Drain-source Voltage ($V_{in} = 0$)	Internally Clamped		V
V_{in}	Input Voltage	18		V
I_D	Drain Current	Internally Limited		A
I_R	Reverse DC Output Current	-28		A
V_{esd}	Electrostatic Discharge (C= 100 pF, R=1.5 K Ω)	2000		V
P_{tot}	Total Dissipation at $T_c = 25^\circ\text{C}$	83	34	W
T_j	Operating Junction Temperature	Internally Limited		$^\circ\text{C}$
T_c	Case Operating Temperature	Internally Limited		$^\circ\text{C}$
T_{stg}	Storage Temperature	-55 to 150		$^\circ\text{C}$

THERMAL DATA

		ISOWATT220	PowerSO-10	D2PAK	
$R_{thj-case}$	Thermal Resistance Junction-case Max	3.75	1.5	1.5	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	62.5	50	62.5	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CLAMP}	Drain-source Clamp Voltage	$I_D = 200\text{ mA}$ $V_{in} = 0$	60	70	80	V
V_{CLTH}	Drain-source Clamp Threshold Voltage	$I_D = 2\text{ mA}$ $V_{in} = 0$	55			V
V_{INCL}	Input-Source Reverse Clamp Voltage	$I_{in} = -1\text{ mA}$	-1		-0.3	V
I_{DSS}	Zero Input Voltage Drain Current ($V_{in} = 0$)	$V_{DS} = 13\text{ V}$ $V_{in} = 0$ $V_{DS} = 25\text{ V}$ $V_{in} = 0$			50 200	μA μA
I_{ISS}	Supply Current from Input Pin	$V_{DS} = 0\text{ V}$ $V_{in} = 10\text{ V}$		250	500	μA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{IN(th)}$	Input Threshold Voltage	$V_{DS} = V_{in}$ $I_D + I_{in} = 1\text{ mA}$	0.8		3	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{in} = 10\text{ V}$ $I_D = 10\text{ A}$ $V_{in} = 5\text{ V}$ $I_D = 10\text{ A}$			0.05 0.07	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} = 13\text{ V}$ $I_D = 10\text{ A}$	13	17		S
C_{OSS}	Output Capacitance	$V_{DS} = 13\text{ V}$ $f = 1\text{ MHz}$ $V_{in} = 0$		500	800	pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING (**)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_d = 10\text{ A}$		90	180	ns
t_r	Rise Time	$V_{gen} = 10\text{ V}$ $R_{gen} = 10\text{ }\Omega$		240	400	ns
$t_{d(off)}$	Turn-off Delay Time	(see figure 3)		430	800	ns
t_f	Fall Time			150	300	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_d = 10\text{ A}$		800	1200	ns
t_r	Rise Time	$V_{gen} = 10\text{ V}$ $R_{gen} = 1000\text{ }\Omega$		1.5	2.2	μs
$t_{d(off)}$	Turn-off Delay Time	(see figure 3)		6	10	μs
t_f	Fall Time			3.5	5.5	μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 15\text{ V}$ $I_D = 10\text{ A}$ $V_{in} = 10\text{ V}$ $R_{gen} = 10\text{ }\Omega$		60		A/ μs
Q_i	Total Input Charge	$V_{DD} = 12\text{ V}$ $I_D = 10\text{ A}$ $V_{in} = 10\text{ V}$		60		nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 10\text{ A}$ $V_{in} = 0$			1.6	V
$t_{rr}(**)$	Reverse Recovery Time	$I_{SD} = 10\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$		165		ns
$Q_{rr}(**)$	Reverse Recovery Charge	(see test circuit, figure 5)		0.55		μC
$I_{RRM}(**)$	Reverse Recovery Current			6.5		A

PROTECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain Current Limit	$V_{in} = 10\text{ V}$ $V_{DS} = 13\text{ V}$ $V_{in} = 5\text{ V}$ $V_{DS} = 13\text{ V}$	14 14	20 20	28 28	A A
$t_{dlim}(**)$	Step Response Current Limit	$V_{in} = 10\text{ V}$ $V_{in} = 5\text{ V}$		29 70	60 140	μs μs
$T_{jsh}(**)$	Overtemperature Shutdown		150			$^\circ\text{C}$
$T_{jrs}(**)$	Overtemperature Reset		135			$^\circ\text{C}$
$I_{gf}(**)$	Fault Sink Current	$V_{in} = 10\text{ V}$ $V_{in} = 5\text{ V}$		50 20		mA mA
$E_{as}(**)$	Single Pulse Avalanche Energy	starting $T_j = 25\text{ }^\circ\text{C}$ $V_{DD} = 20\text{ V}$ $V_{in} = 10\text{ V}$ $R_{gen} = 1\text{ K}\Omega$ $L = 10\text{ mH}$	0.95			J

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(**) Parameters guaranteed by design/characterization

PROTECTION FEATURES

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user's standpoint is that a small DC current (I_{ISS}) flows into the Input pin in order to supply the internal circuitry.

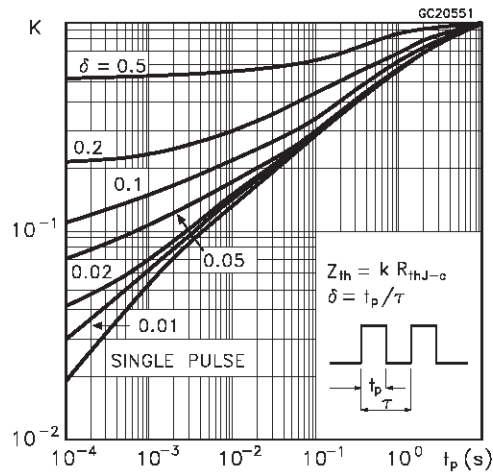
The device integrates:

- **OVERVOLTAGE CLAMP PROTECTION:** internally set at 70V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- **LINEAR CURRENT LIMITER CIRCUIT:** limits the drain current I_d to I_{lim} whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

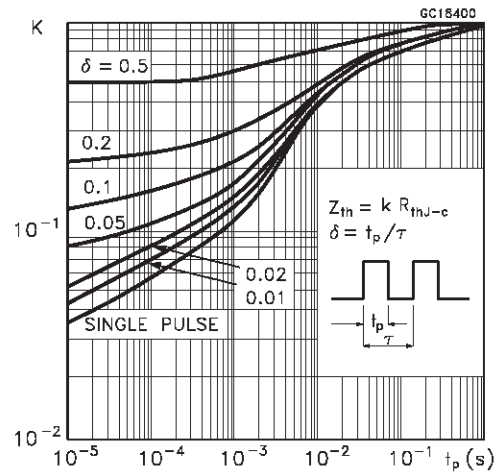
- **OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:** these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150°C. The device is automatically restarted when the chip temperature falls below 135°C.
- **STATUS FEEDBACK:** In the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω . The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

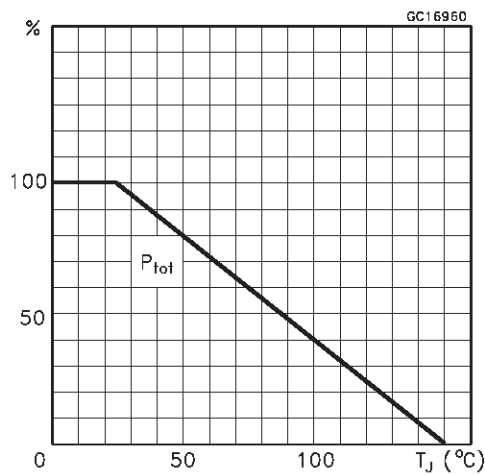
Thermal Impedance For ISOWATT220



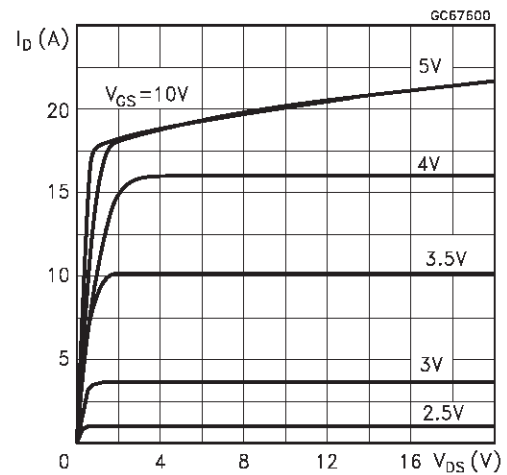
Thermal Impedance For D2PAK / PowerSO-10



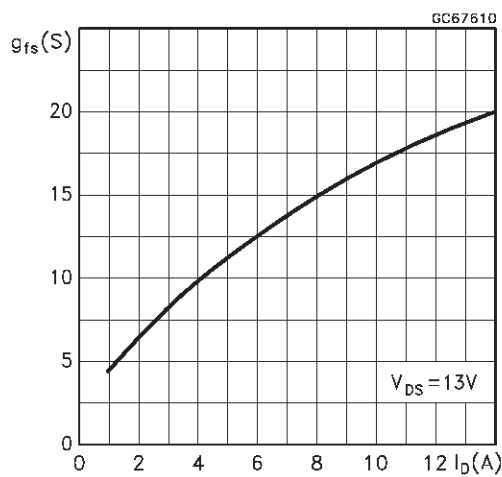
Derating Curve



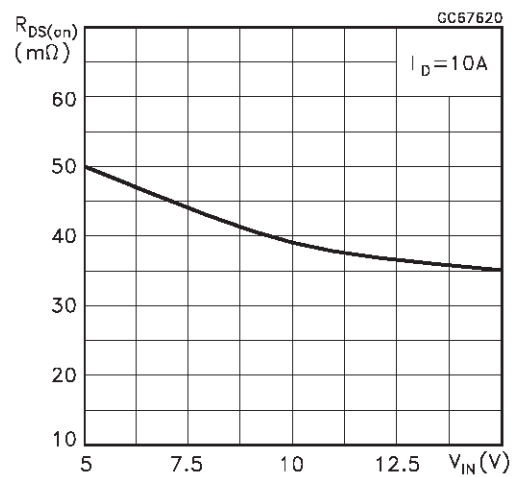
Output Characteristics



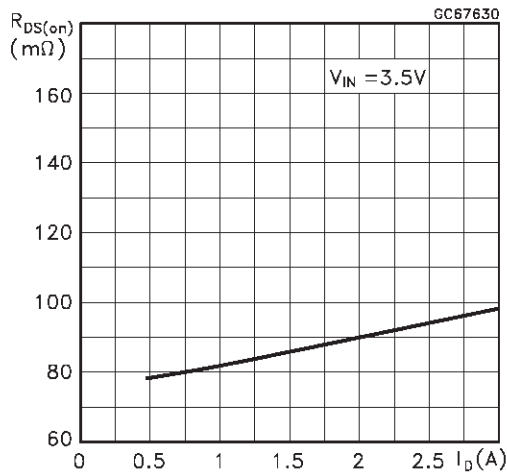
Transconductance



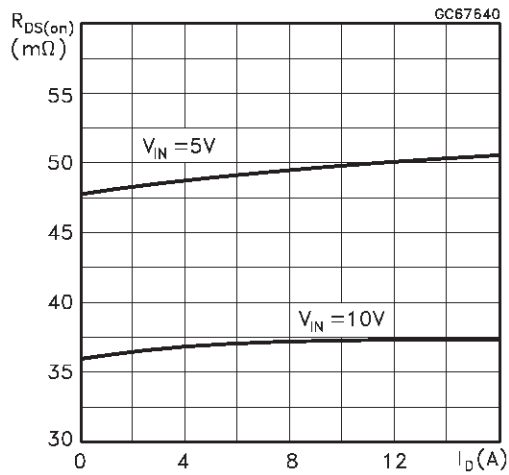
Static Drain-Source On Resistance vs Input Voltage



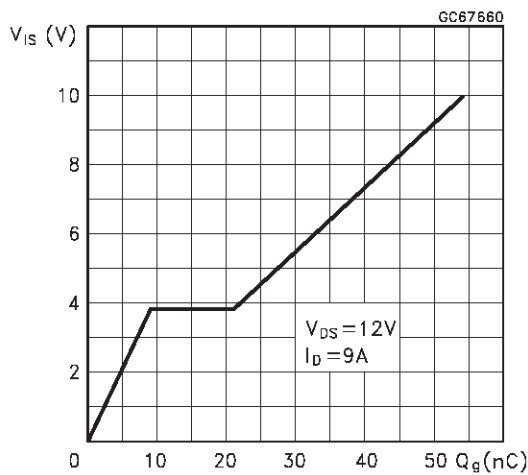
Static Drain-Source On Resistance



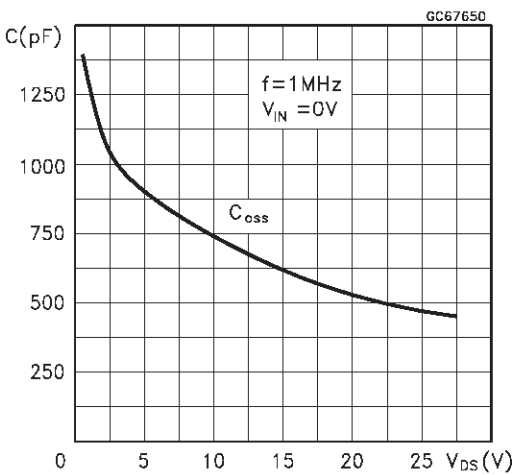
Static Drain-Source On Resistance



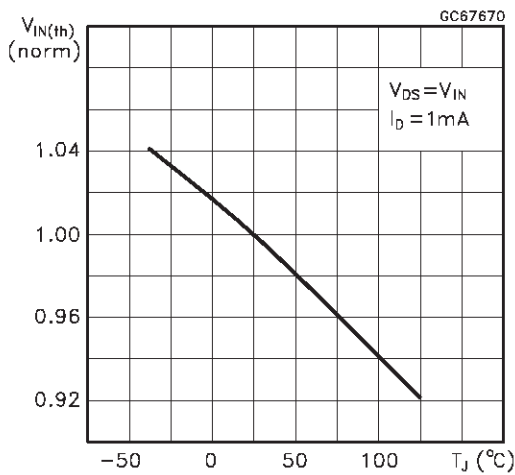
Input Charge vs Input Voltage



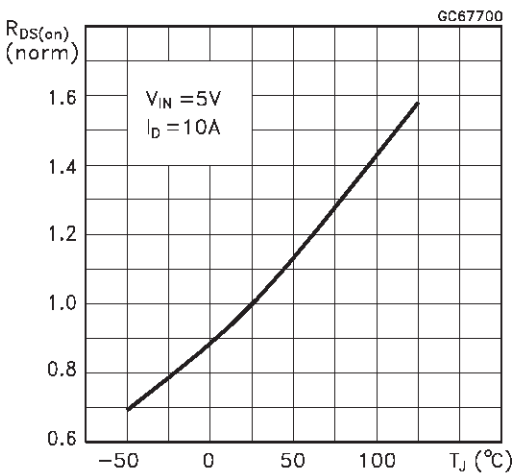
Capacitance Variations



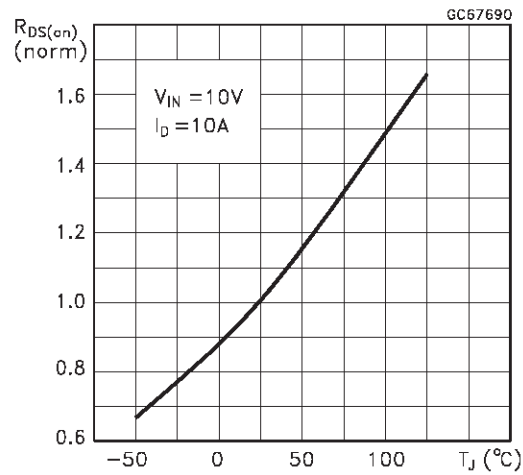
Normalized Input Threshold Voltage vs Temperature



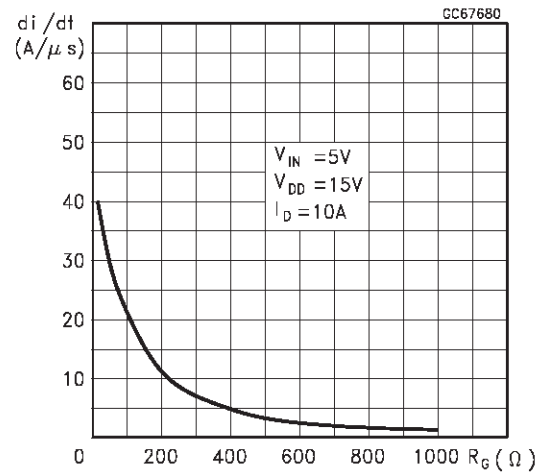
Normalized On Resistance vs Temperature



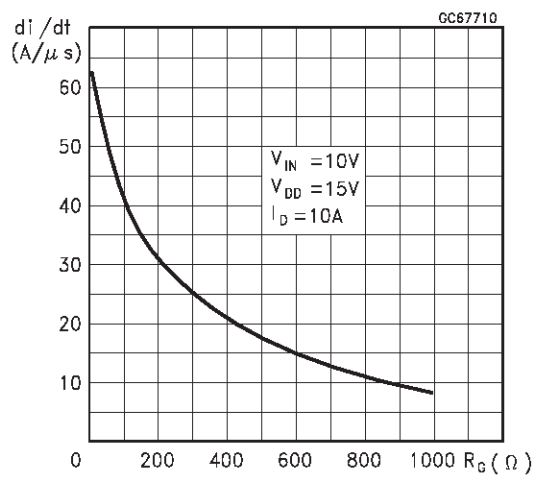
Normalized On Resistance vs Temperature



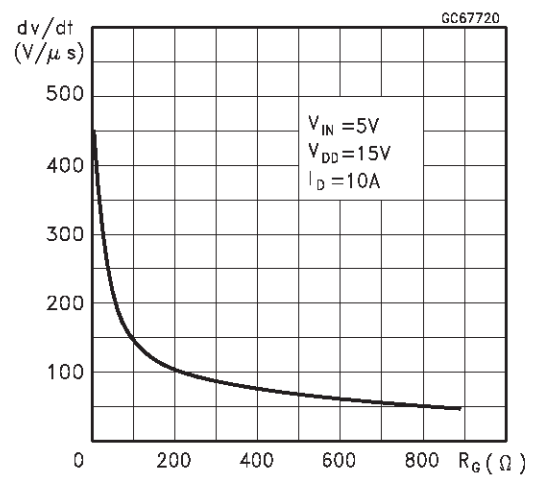
Turn-on Current Slope



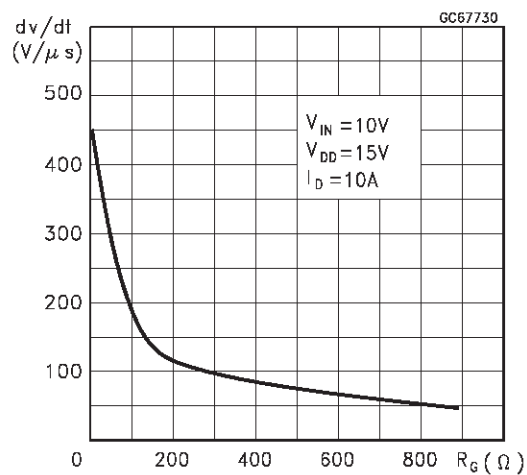
Turn-on Current Slope



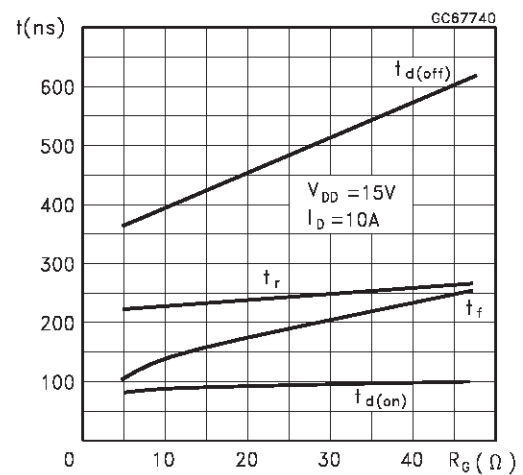
Turn-off Drain-Source Voltage Slope



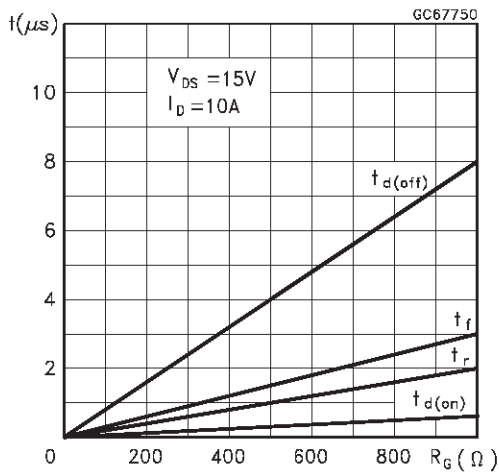
Turn-off Drain-Source Voltage Slope



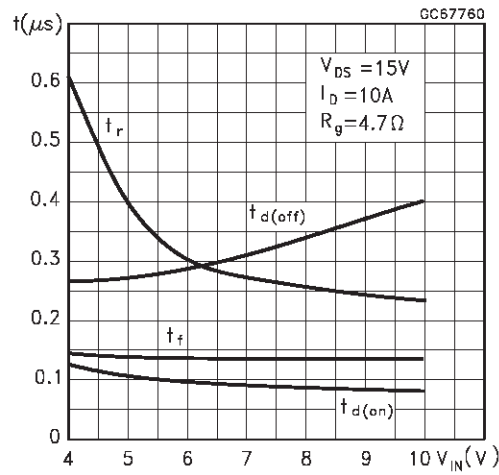
Switching Time Resistive Load



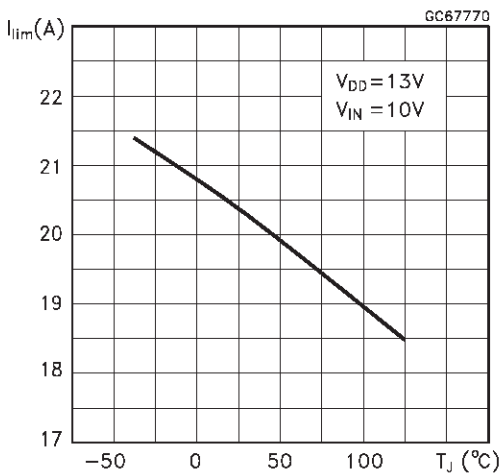
Switching Time Resistive Load



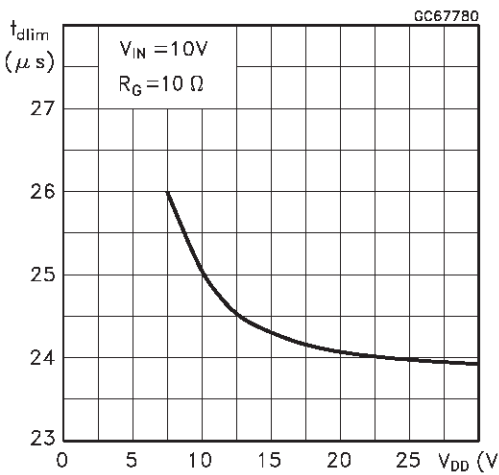
Switching Time Resistive Load



Current Limit vs Junction Temperature



Step Response Current Limit



Source Drain Diode Forward Characteristics

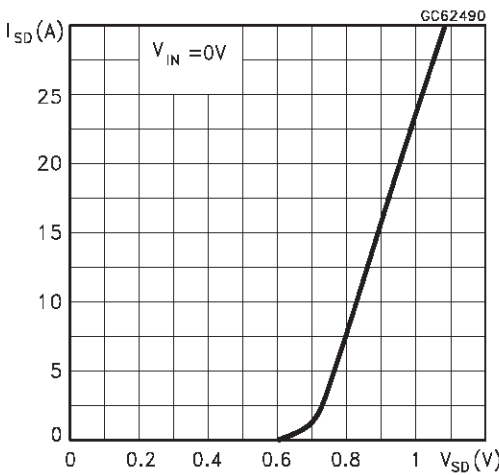
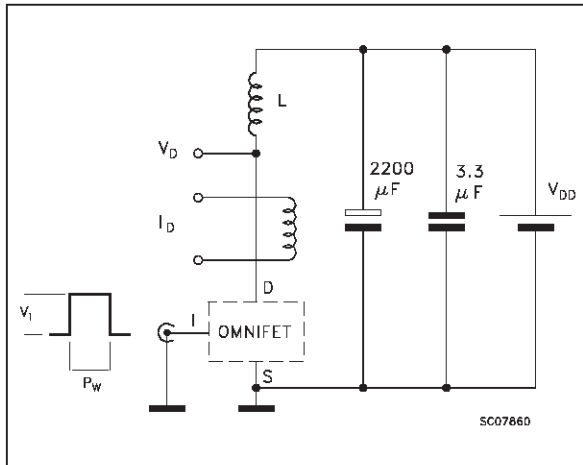
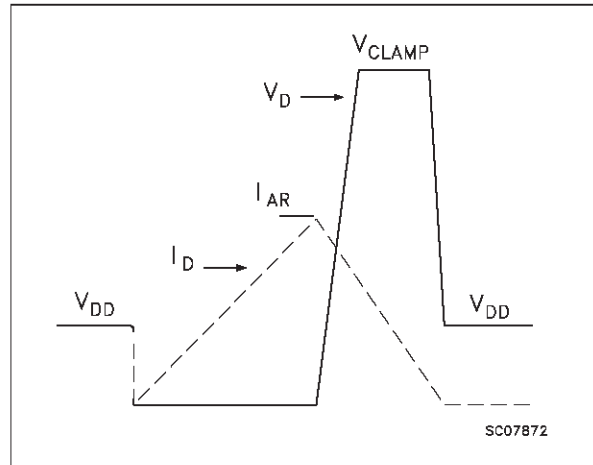
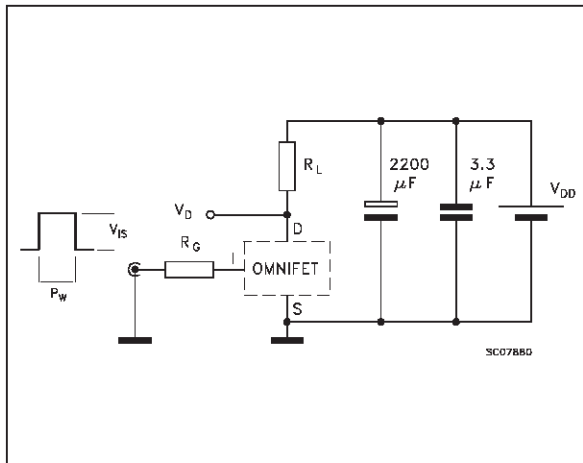
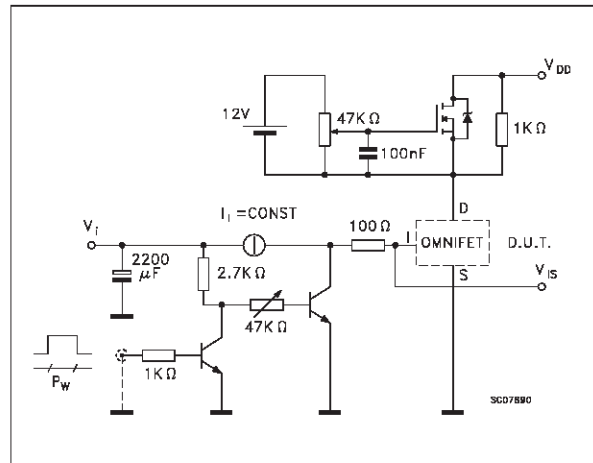
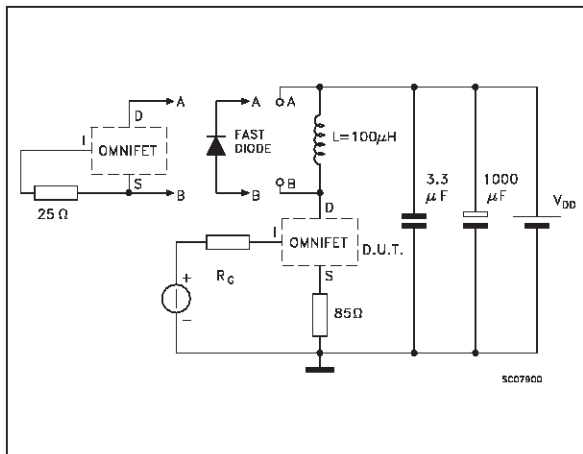
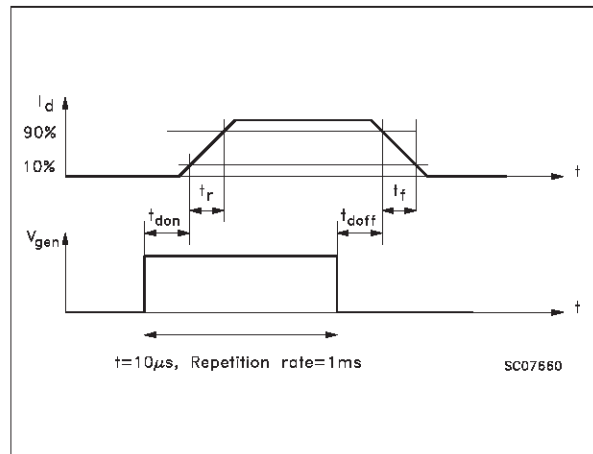
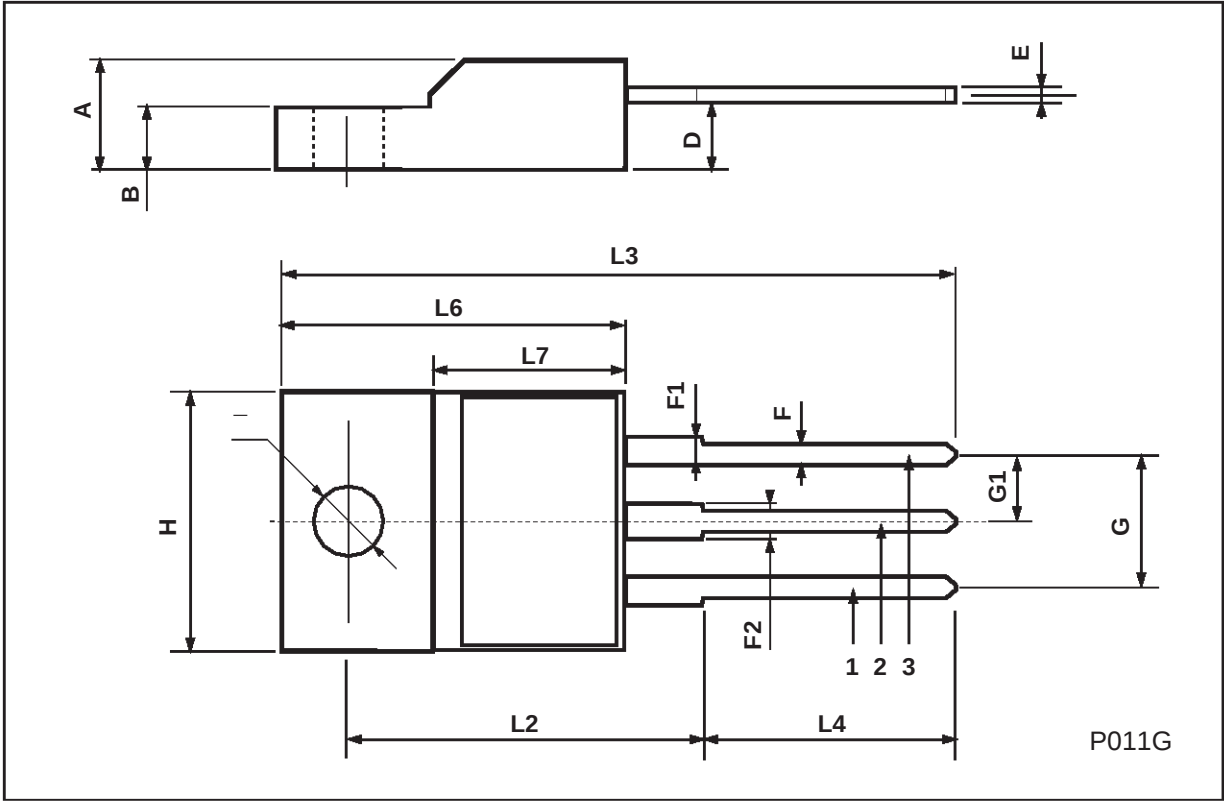


Fig. 1: Unclamped Inductive Load Test Circuits

Fig. 2: Unclamped Inductive Waveforms

Fig. 3: Switching Times Test Circuits For Resistive Load

Fig. 4: Input Charge Test Circuit

Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

Fig. 6: Waveforms


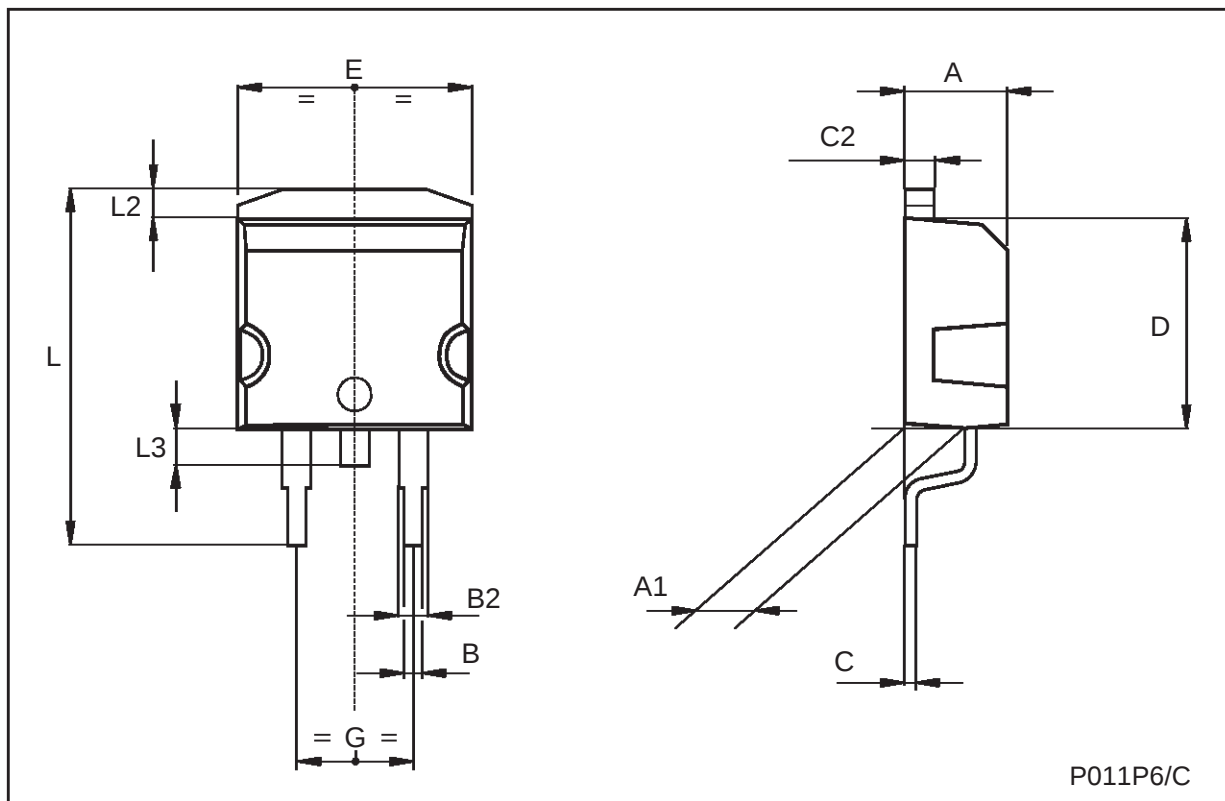
ISOWATT220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



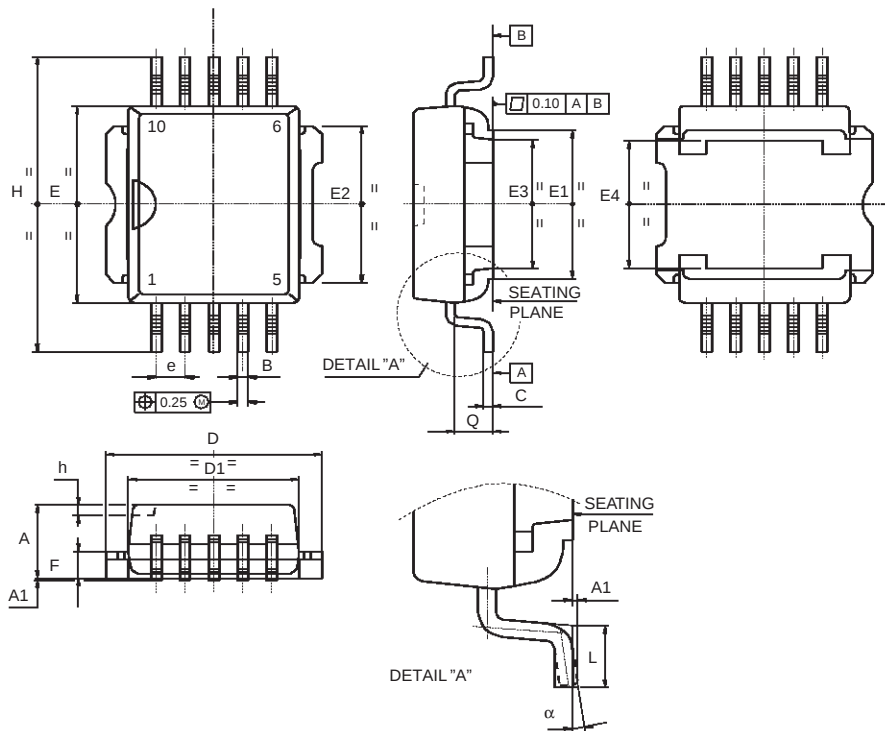
TO-263 (D2PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.3		4.6	0.169		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.25		1.4	0.049		0.055
C	0.45		0.6	0.017		0.023
C2	1.21		1.36	0.047		0.053
D	8.95		9.35	0.352		0.368
E	10		10.28	0.393		0.404
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



PowerSO-10 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0°		8°			



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