

M56692FP

Bi-CMOS & DMOS 32BIT SERIAL-INPUT LATCHED DRIVER

FUNCTION

The M56692FP comprises a 32 bit bidirectional shift register, a 32 bit latch, and a parallel output HVO 1 – HVO32 connected to its output.

In accordance with truth table 1, the data transfer direction of shift register depends upon F/R input, and F/R being at “H” or open allows pin 9 to turn to SIN and pin 2 to turn to SOUT, and F/R being at “L” allows pin 2 to turn to SIN and pin 9 to turn to SOUT, permitting data transfer from SIN to SOUT, respectively.

Inputting data to SIN and clock pulse to $\overline{\text{CLK}}$ allows SIN signal to be put into the internal shift register when the clock changes from “H” to “L”, and shift register data to be shifted sequentially.

Serial-output SOUT is used by connecting to the next stage M56692FP SIN when more than one M56692FP is used to expand bits in the series.

In accordance with truth table 2, parallel output allows the latch to pass data through if LAT input is turned to “H”, and data to be retained if LAT input is turned to “L”. Driver output HVOn allows data from the latch to be output if BLK input is turned to “L”, and “L” to be output if BLK input is turned to “H” irrespective of data from the latch.

TRUTH TABLE

Truth table 1. Shift register section

Input		Input/output		Shift register
F/R	$\overline{\text{CLK}}$	SIN(SOUT)	SOUT(SIN)	
H	↓	IN	OUT	DATA is shifted.
H	H or L	IN	OUT	No changes.
L	↓	OUT	IN	DATA is shifted.
L	H or L	OUT	IN	No changes.

Truth table 2. Latch and driver sections

Dn	LAT	BLK	HVOn
X	X	H	Output all “L”
H	H	L	H
L	H	L	L
X	L	L	Latch's data output.

Dn=nth bit DFF retention data

HVOn=nth bit driver output

L = “L” level

H = “H” level

X = “L” level or “H” level

PIN FUNCTION DESCRIPTION

Pin name	Function
V _{DD}	Logic stage supply voltage
LGND	Logic stage ground
V _H	Output stage supply voltage
PGND	Output stage supply ground
$\overline{\text{CLK}}$	Clock input for the internal shift register. The data enter the internal shift registers and the data in the shift registers will be shifted in order by High to Low change of the clock.
SIN	Serial data input
SOUT	Serial data output
LAT	Latch input. When the LATCH is set to “H”, the data in the shift register will enter the each latch circuit. When the LATCH input is set to “L”, the data will be held.
BLK	Enable input for output control. When the BLK input is set to “L”, data in the latch circuit will appear at outputs. When the BLK input is set to “H”, all outputs will be set to “L”.
F/R	Direction Control for the internal shift register
HVO1–32	Output driver (push-pull)

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{DD}	Logic stage supply voltage		-0.3 – 7	V
V _H	Output stage supply voltage		-0.3 – 90	V
V _I	Logic inputs voltage		-0.3 – V _{DD} +0.3	V
V _O	Logic output voltage	Data output	-0.3 – V _{DD} +0.3	V
V _{HVO}	Output voltage	High supply voltage output pin	-0.3 – V _H	V
P _d	Power dissipation range	Ta ≤ 25°C	850	mW
T _{stg}	Storage temperature range		-55 – 150	°C

M56692FP**Bi-CMOS & DMOS 32BIT SERIAL-INPUT LATCHED DRIVER****RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Conditions	Ratings	Unit
V _{DD}	Supply voltage		4 – 6	V
V _H	Supply voltage		40 – 90	V
T _{opr}	Operating temperature		-40 – 85	°C

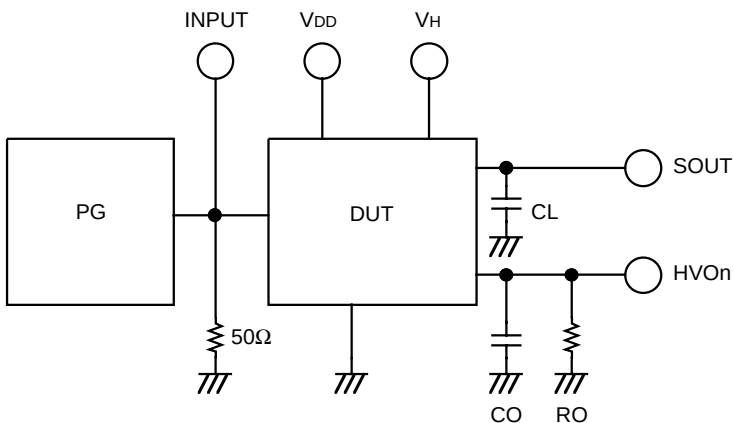
ELECTRICAL CHARACTERISTICS (V_{DD}=5V, V_H=80V and T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{DD}	Supply current 1	No load		0.4	2	mA
I _H	Supply current 2	Output all "L", no load		0	1	mA
		1 bit "H", no load		0.4	1	mA
I _{IH}	"H" input current	V _{IH} =5V input pin		0	1	μA
I _{IL}	"L" input current	V _{IL} = 0V		0	-1	μA
		SIN, LAT, CLK BLK, F/R		-250	-500	μA
V _{HVOH}	Driver output voltage	I _{HVOH} = -50mA	70	75.5		V
V _{HVOL}		I _{HVOL} = 10mA		0.5	2.5	
V _{OH}	Logic output voltage	I _{OH} = -0.1mA	4.5	4.9		V
V _{OL}		I _{OL} = 0.1mA		0.1	0.4	
I _{HVOH}	"H" output current	Duty cycle ≤ 2.5%*		-50	-100	mA
I _{HVOL}	"L" output current			10	20	mA
V _{TH}	Output protect operating voltage			3.3		V
V _{TL}				3.0		V

* Maximum numbers of Outputs High State are two at the same time.

SWITCHING CHARACTERISTICS (V_{DD}=5V, V_H=80V and T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
fCLK	Clock frequency	Duty = 45 – 55%			8	MHz
t PLH(SO)	Logic output propagation time	CL = 15pF		90	180	ns
t PHL(SO)				60	180	ns
tPLH(OUT)	Driver output propagation time	RO = 220KΩ CO = 50pF		95		ns
tPHL(OUT)				70		ns
trout	Driver output rise and fall time			35		ns
tfout				65		ns

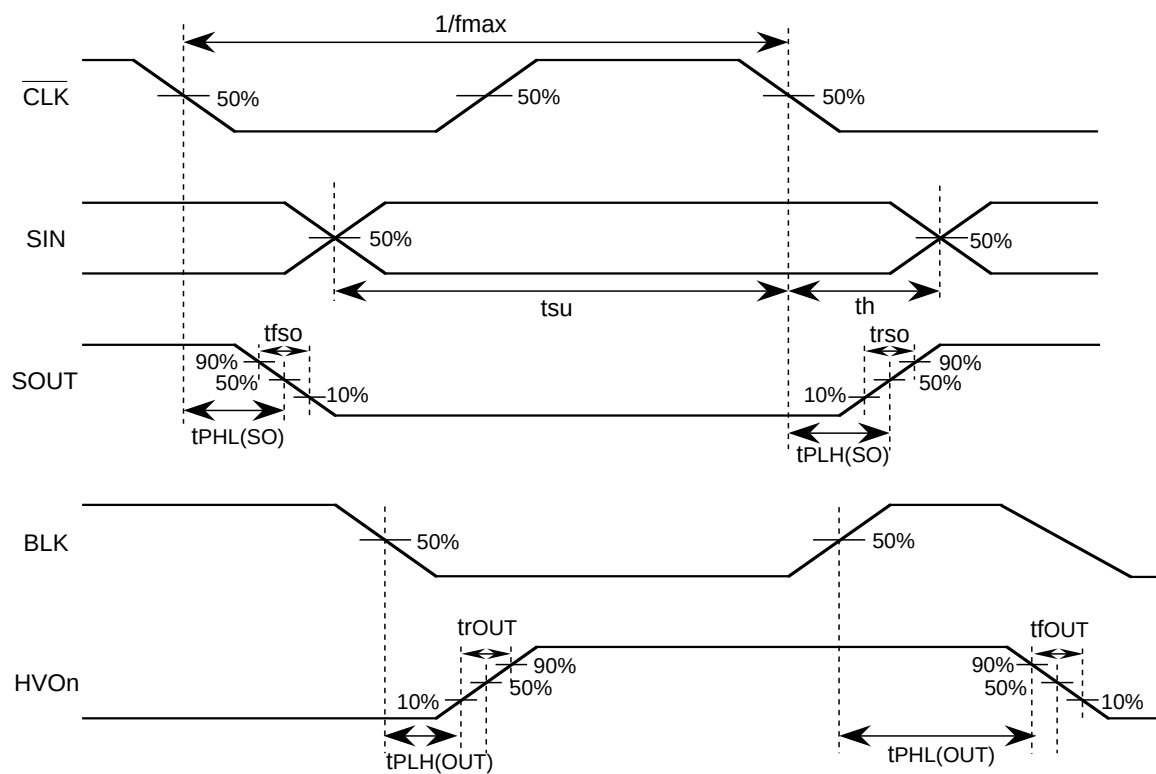
TEST CIRCUIT

- (1) Characteristics of pulse generator (PG)
tr≤20ns tf≤20ns
- (2) Capacitance CL includes connection
floating capacitance and probe input
capacitance.
: RO=220KΩ
: CO=50pF

M56692FP

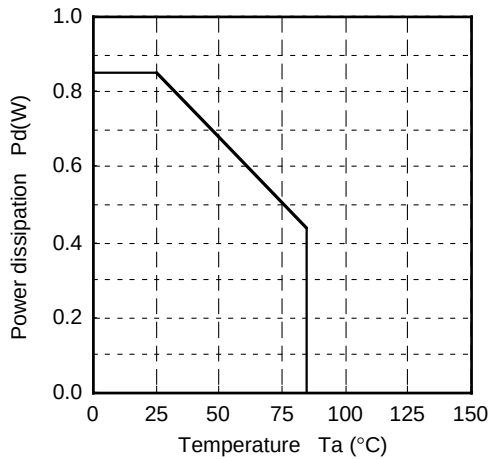
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TIMING WAVEFORM

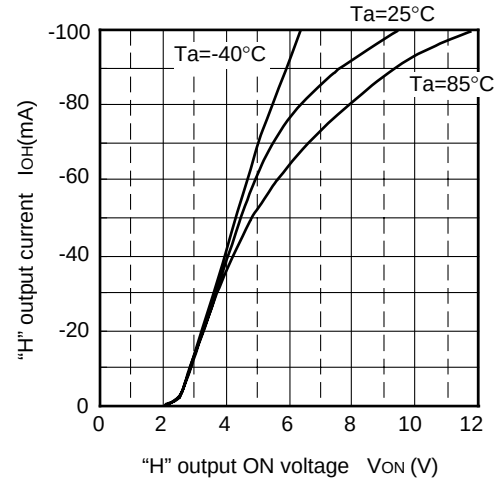


TYPICAL CHARACTERISTICS

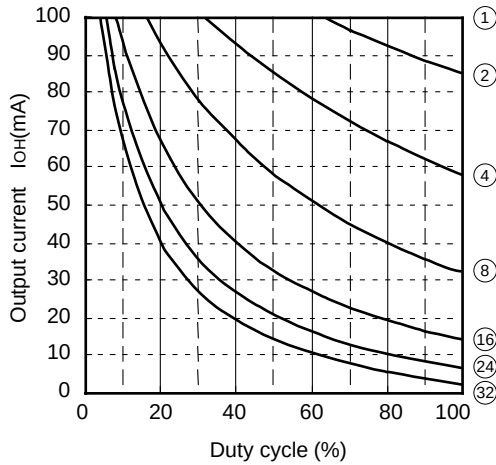
Thermal derating



Driver output $V_{ON}-I_{OH}$

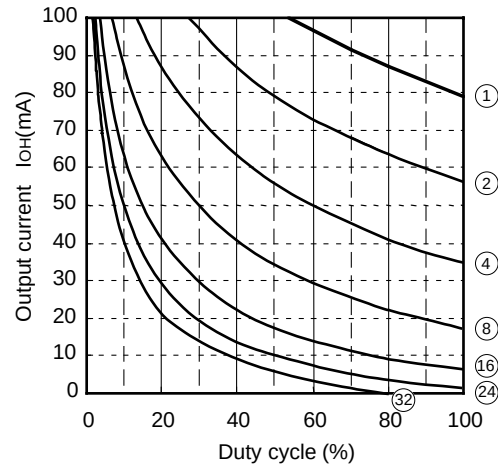


Duty cycle vs Permissible output current



- Note
- $T_a = 25$ °C
 - Repeated frequency > 100Hz
 - Figure in the circle represents the number of concurrently operating output circuits.
 - Current value denotes a numerical value per circuit.

Duty cycle vs Permissible output current



- Note
- $T_a = 85$ °C
 - Repeated frequency > 100Hz
 - Figure in the circle represents the number of concurrently operating circuits.
 - Current value denotes a numerical value per circuit.

- (Note)
1. $V_{DD} = 5$ V and $V_H = 80$ V unless otherwise noted.
 2. Thermal derating curve represents that of an individual IC unit.
 3. Allowable duty cycle output curve represents that when a standard substrate is mounted. (Standard substrate: 70x70x1.6mm glass epoxy)