

DESCRIPTION

The M5M5V108DFP,VP,KV are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple-polysilicon and double metal CMOS technology. The use of thin film transistor (TFT) load cells and CMOS periphery result in a high density and low power static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M5V108DVP,KV are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD).

FEATURES

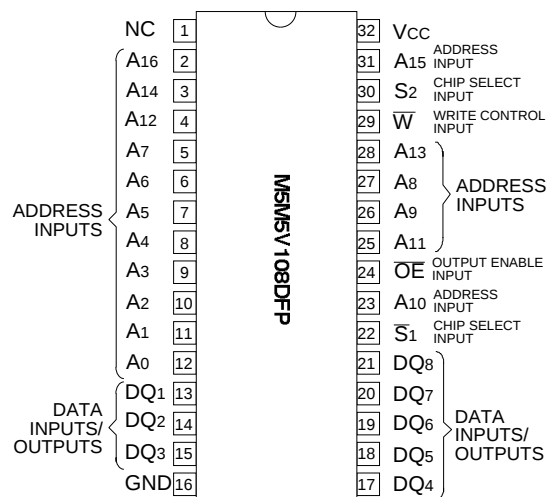
Type name	Access time (max)	V _{CC}	Power supply current	
			Active (1MHz) (max)	stand-by (max)
M5M5V108DFP,VP,KV-70H	70ns	2.7~3.6V	5mA	12μA

- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S}_1, S_2$
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package

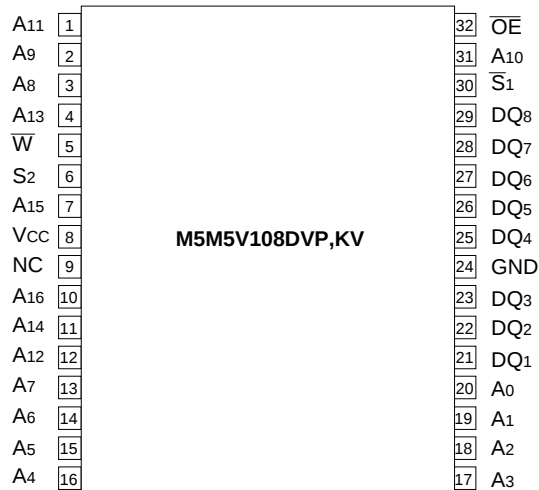
M5M5V108DFP 32pin 525mil SOP
 M5M5V108DVP,RV 32pin 8 X 20 mm² TSOP
 M5M5V108DKV,KR 32pin 8 X 13.4 mm² TSOP

APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)

Outline 32P2M-A



Outline 32P3H-E(VP), 32P3K-B(KV)

NC : NO CONNECTION

FUNCTION

The operation mode of the M5M5V108D series are determined by a combination of the device control inputs $\overline{S_1}$, S_2 , $\overline{W}$ and $\overline{OE}$.

Each mode is summarized in the function table.

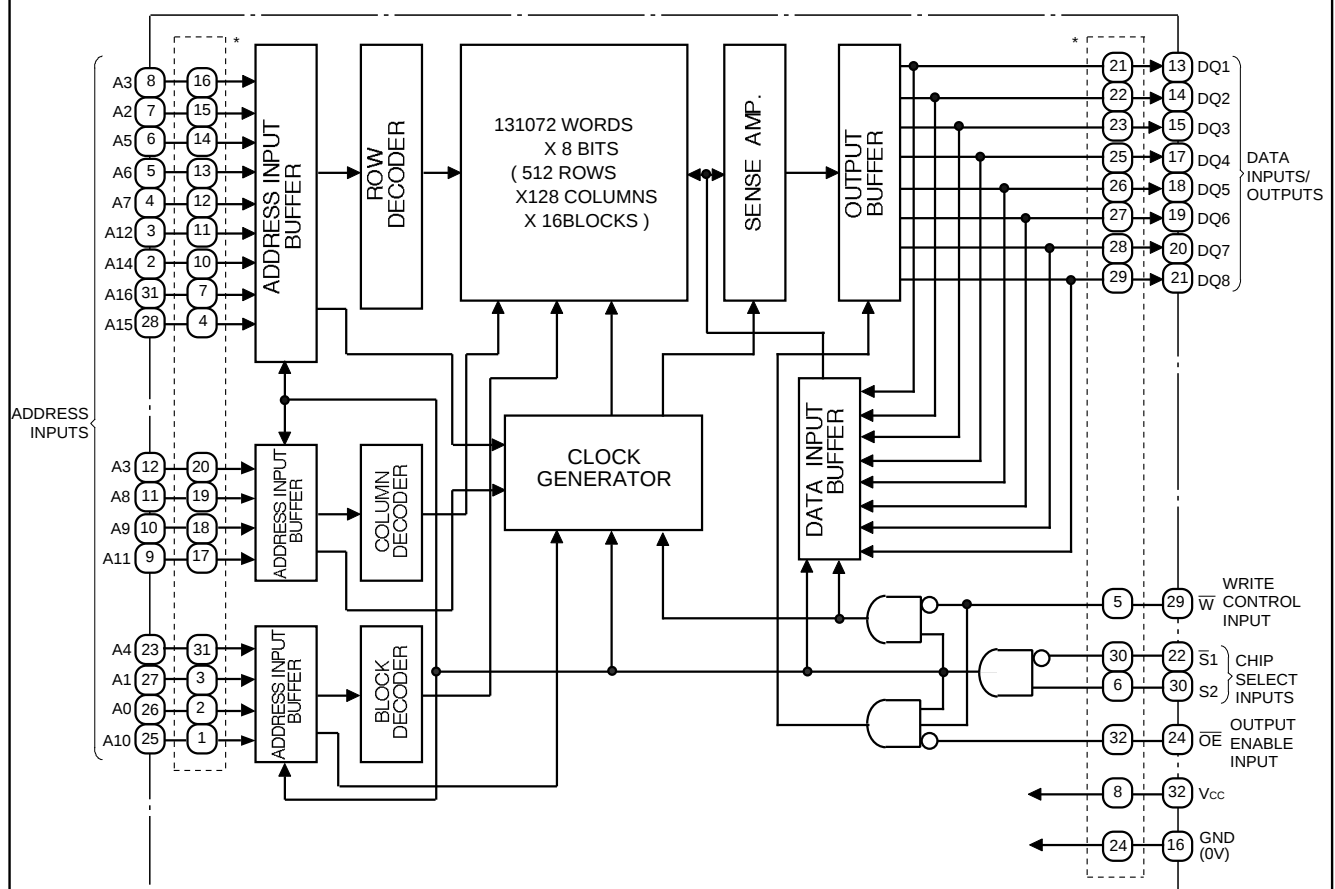
A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}=L, S_2=H$).

FUNCTION TABLE

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	I _{cc}
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ and S_2 . The power supply current is reduced as low as the stand-by current which is specified as I_{cc3} or I_{cc4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

BLOCK DIAGRAM

* Pin numbers inside dotted line show those of TSOP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	- 0.3~4.6	V
V _I	Input voltage		- 0.3~V _{cc} + 0.3 (Max 4.6)	V
V _O	Output voltage		0~V _{cc}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		- 65~150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{cc}=2.7~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.0		V _{cc} + 0.3	V
V _{IL}	Low-level input voltage		-0.3*		0.6	V
V _{OH1}	High-level output voltage 1	I _{OH} = - 0.5mA	2.4			V
V _{OH2}	High-level output voltage 2	I _{OH} = - 0.05mA	V _{cc} - 0.5			V
V _{OL}	Low-level output voltage	I _{OL} = 2mA			0.4	V
I _I	Input current	V _I =0~V _{cc}			±1	μA
I _O	Output current in off-state	$\bar{S}_1$ =V _{IH} or S ₂ =V _{IL} or $\bar{OE}$ =V _{IH} V _{I/O} =0~V _{cc}			±1	μA
I _{CC1}	Active supply current	$\bar{S}_1$ =V _{IL} , S ₂ =V _{IH} , other inputs=V _{IH} or V _{IL} Output-open(duty 100%)	70ns		35	
I _{CC2}	Active supply current		1MHz		5	
I _{CC3}	Stand-by current	1) S ₂ ≤ 0.2V other inputs=0~V _{cc} 2) $\bar{S}_1$ ≥ V _{cc} -0.2V, S ₂ ≥ V _{cc} -0.2V other inputs=0~V _{cc}	-H	~25°C	1.2	μA
				~40°C	3.6	
				~70°C	12	
I _{CC4}	Stand-by current	$\bar{S}_1$ =V _{IH} or S ₂ =V _{IL} , other inputs=0~V _{cc}			0.33	mA

* -3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE (T_a=0~70°C, unless otherwise noted)

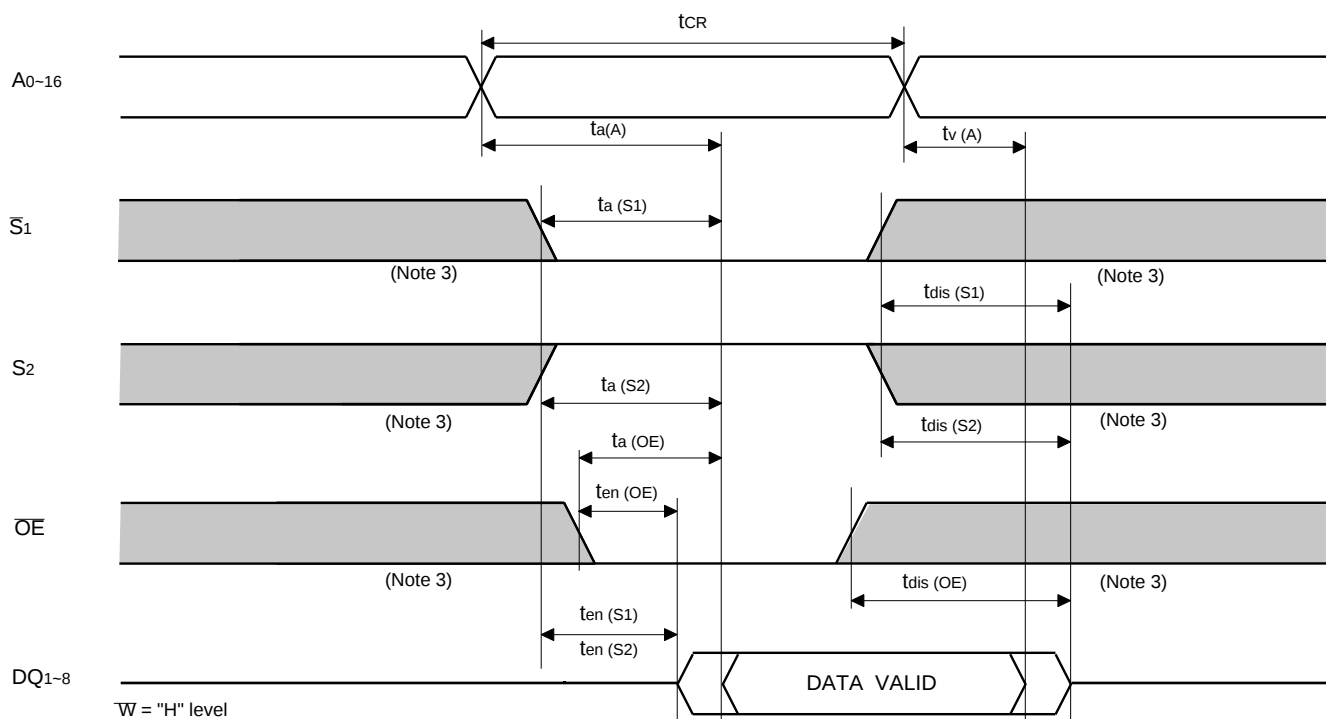
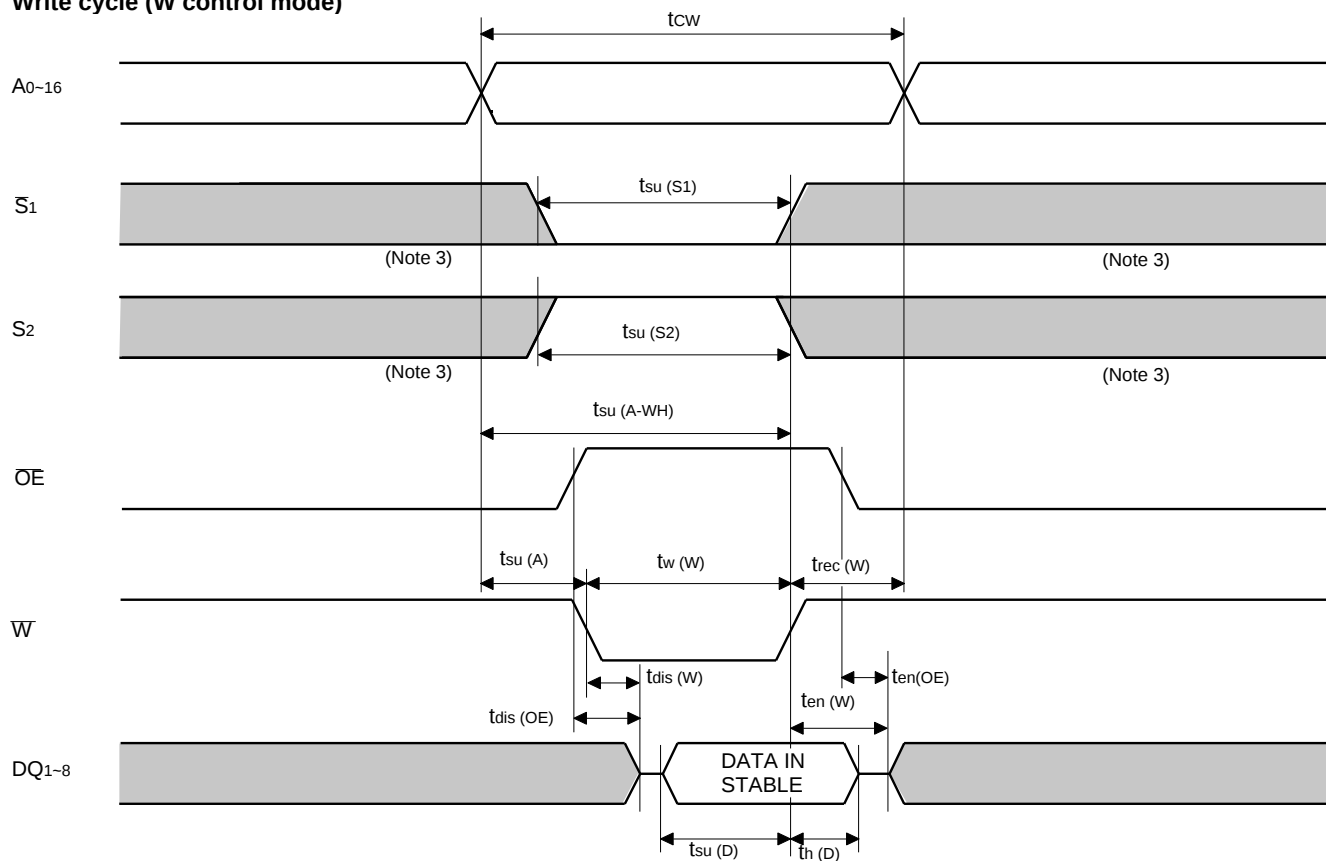
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			8	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	pF

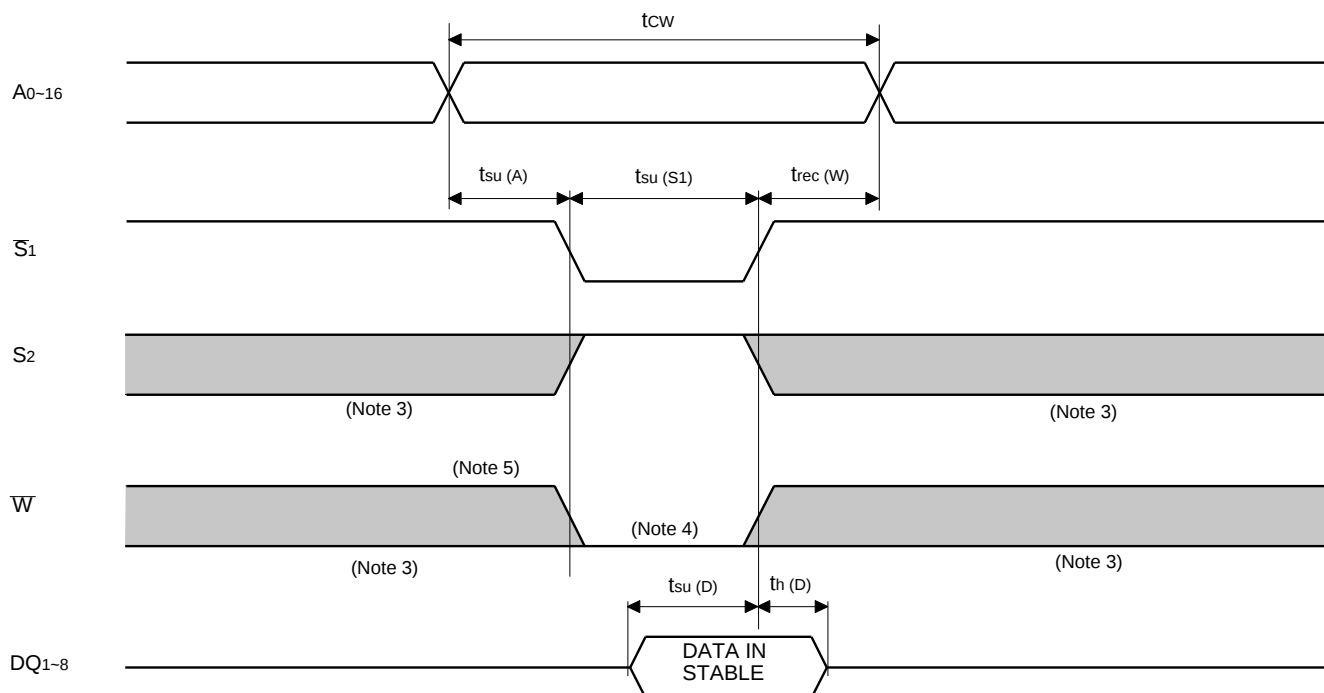
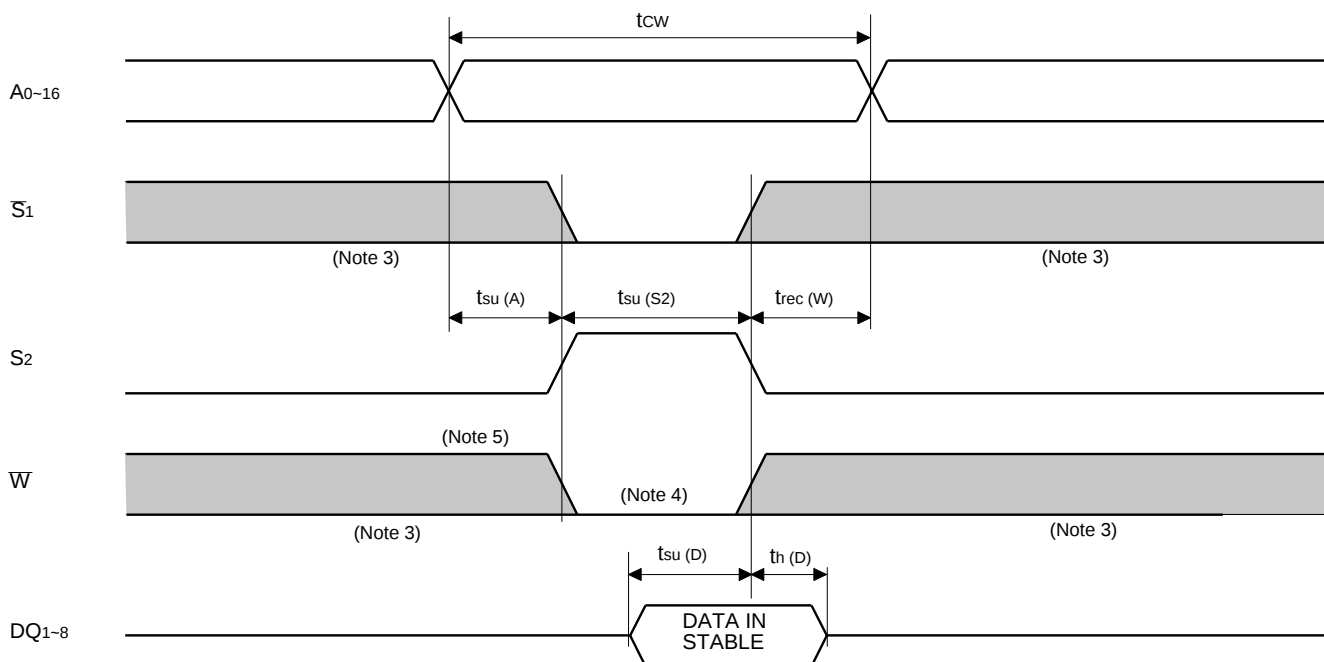
Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V_{cc} = 3V, T_a = 25°C

(4) TIMING DIAGRAMS

Read cycle

Write cycle ($\overline{W}$ control mode)

Write cycle ($\overline{S1}$ control mode)Write cycle ($\overline{S2}$ control mode)

Note 3: Hatching indicates the state is "don't care".

4: Writing is executed while $\overline{S2}$ high overlaps $\overline{S1}$ and $\overline{W}$ low.

5: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of $\overline{S2}$, the outputs are maintained in the high impedance state.

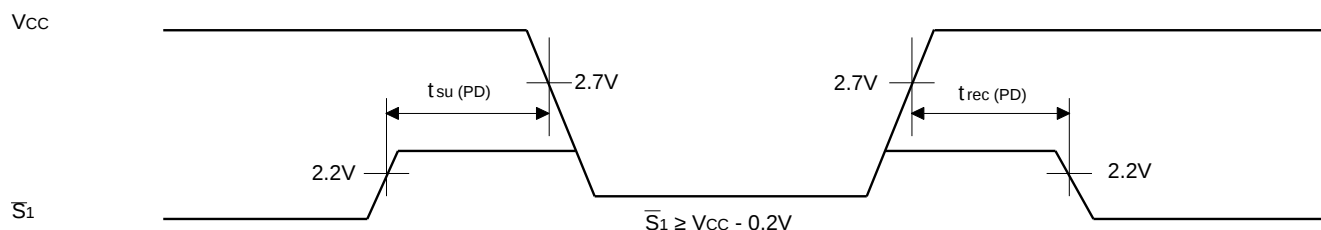
6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS**(1) ELECTRICAL CHARACTERISTICS** (Ta=0~70°C, unless otherwise noted)

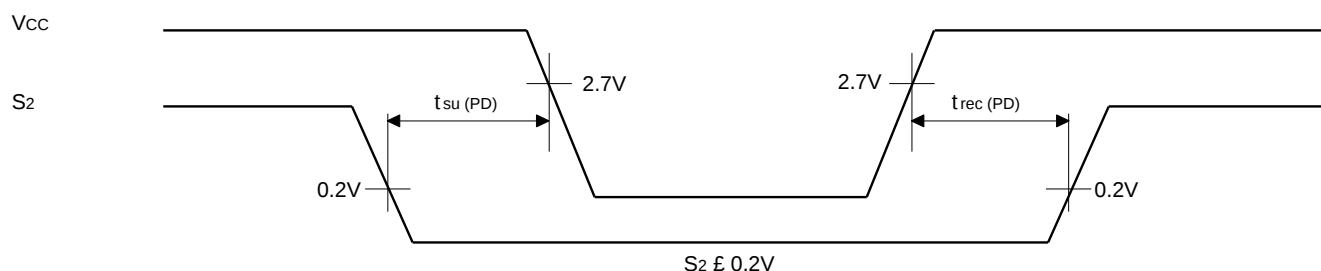
Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
VCC (PD)	Power down supply voltage				2			V
VI (S1)	Chip select input S1				2.0	Vcc(PD)		V
VI (S2)	Chip select input S2	2.7V≤Vcc(PD)					0.6	V
		Vcc(PD)<2.7V					0.2	v
ICC (PD)	Power down supply current	Vcc = 3V	1) S2 £ 0.2V, other inputs = 0~3V 2) S1 ≥ Vcc–0.2V, S2 ≥ Vcc–0.2V other inputs = 0~3V	-H	~25°C		1	µA
					~40°C		3	
					~70°C		10	

(2) TIMING REQUIREMENTS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS **$\overline{S_1}$ control mode**

Note 7: On the power down mode by controlling $\overline{S_1}$, the input level of S2 must be S2 ≥ V_{CC} - 0.2V or S2 ≤ 0.2V. The other pins(Address, I/O, $\overline{WE}$, $\overline{OE}$) can be in high impedance state.

S2 control mode

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