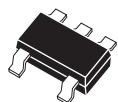


CFMS4
**SURFACE MOUNT
DUAL, COMMON BASE,
SILICON PNP TRANSISTORS**



SOT-25 CASE

CentralTM
Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CFMS4 consists of two silicon PNP transistors in a common base configuration, manufactured by the epitaxial planar process and epoxy molded in a space saving SOT-25 surface mount package. This device has been designed for small signal applications where a high breakdown voltage is required.

MARKING CODE: CFMS4

MAXIMUM RATINGS: ($T_A=25^{\circ}\text{C}$)

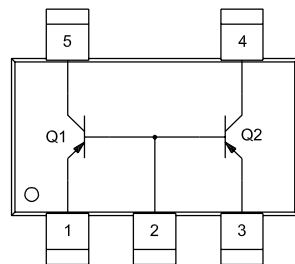
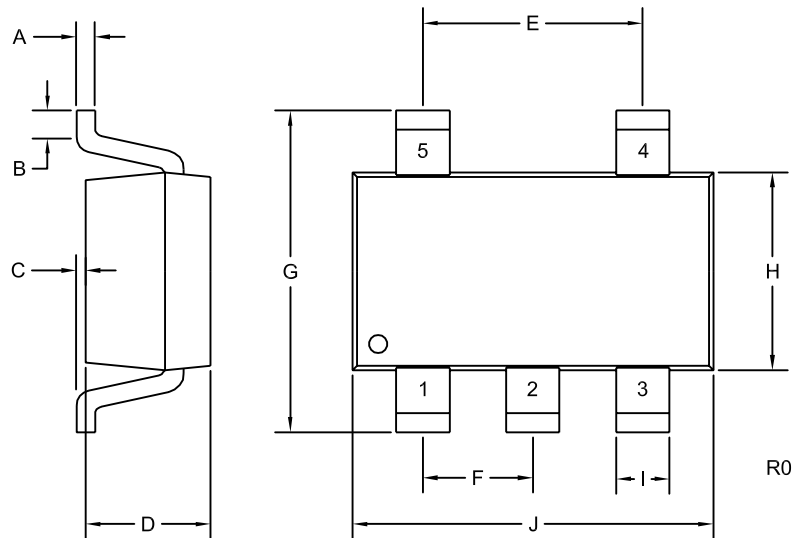
	SYMBOL		UNITS
Collector-Base Voltage	V_{CBO}	120	V
Collector-Emitter Voltage	V_{CEO}	120	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Continuous Collector Current	I_C	50	mA
Power Dissipation	P_D	350	mW
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CBO}	$V_{CB}=100\text{V}$			500	nA
I_{EBO}	$V_{EB}=4.0\text{V}$			500	nA
BV_{CBO}	$I_C=50\mu\text{A}$	120			V
BV_{CEO}	$I_C=1.0\text{mA}$	120			V
BV_{EBO}	$I_E=50\mu\text{A}$	5.0			V
$V_{CE(SAT)}$	$I_C=10\text{mA}, I_B=1.0\text{mA}$			500	mV
h_{FE}	$V_{CE}=6.0\text{V}, I_C=2.0\text{mA}$	180		820	
f_T	$V_{CE}=12\text{V}, I_E=2.0\text{mA}, f=100\text{MHz}$		140		MHz

R0 (20-July 2004)

SOT-25 CASE - MECHANICAL OUTLINE



LEAD CODE:

- 1) Emitter Q1
- 2) Base Q1, Q2
- 3) Emitter Q2
- 4) Collector Q2
- 5) Collector Q1

DIMENSIONS				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.004	0.007	0.11	0.19
B	0.016	-	0.40	-
C	-	0.004	-	0.10
D	0.039	0.047	1.00	1.20
E	0.074	0.075	1.88	1.92
F	0.037	0.038	0.93	0.97
G	0.102	0.118	2.60	3.00
H	0.059	0.067	1.50	1.70
I	0.016		0.41	
J	0.110	0.118	2.80	3.00

SOT-25 (REV: R0)

MARKING CODE: CFMS4

R0 (20-July 2004)