



1 Mb (128K x 8) Static RAM

Features

- Very high speed: 55 and 70 ns
- Wide voltage range: 2.2V to 3.6V
- Pin compatible with CY62128V
- Ultra-low active power
 - Typical active current: 0.85 mA @ $f = 1$ MHz
 - Typical active current: 5 mA @ $f = f_{MAX}$
- Ultra-low standby power
- Easy memory expansion with $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{OE}$ features
- Automatic power-down when deselected
- Packages offered in a 32-lead SOIC, a 32-lead TSOP, a 32-lead Short TSOP, and a 32-lead Reverse TSOP

Functional Description^[1]

The CY62128DV30 is a high-performance CMOS static RAM organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces

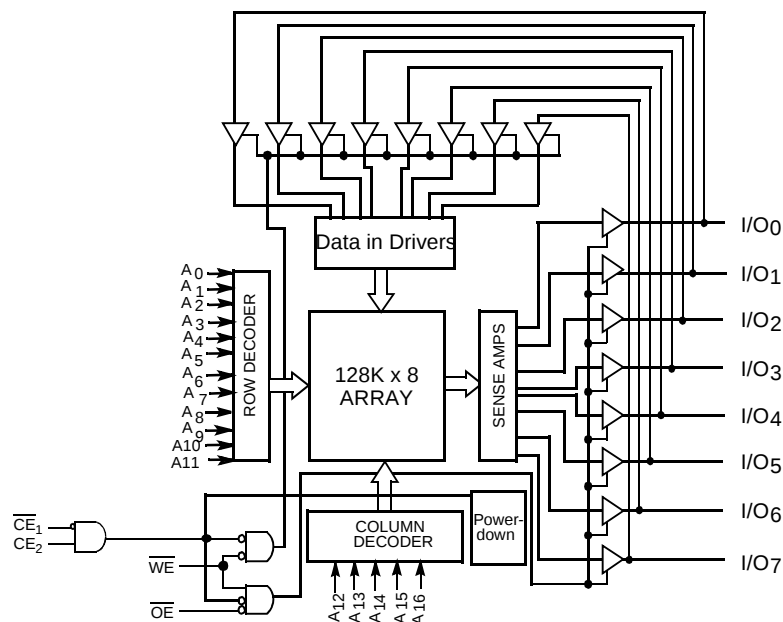
power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 ($\overline{CE}_2$) LOW. The input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when: deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 ($\overline{CE}_2$) LOW, outputs are disabled ($\overline{OE}$ HIGH), or during a write operation (Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 ($\overline{CE}_2$) HIGH and Write Enable ($\overline{WE}$) LOW).

Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) LOW with Chip Enable 2 ($\overline{CE}_2$) HIGH and Write Enable ($\overline{WE}$) LOW. Data on the eight I/O pins is then written into the location specified on the Address pin (A_0 thro. A_{16}).

Reading from the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) LOW with Chip Enable 2 ($\overline{CE}_2$) HIGH and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

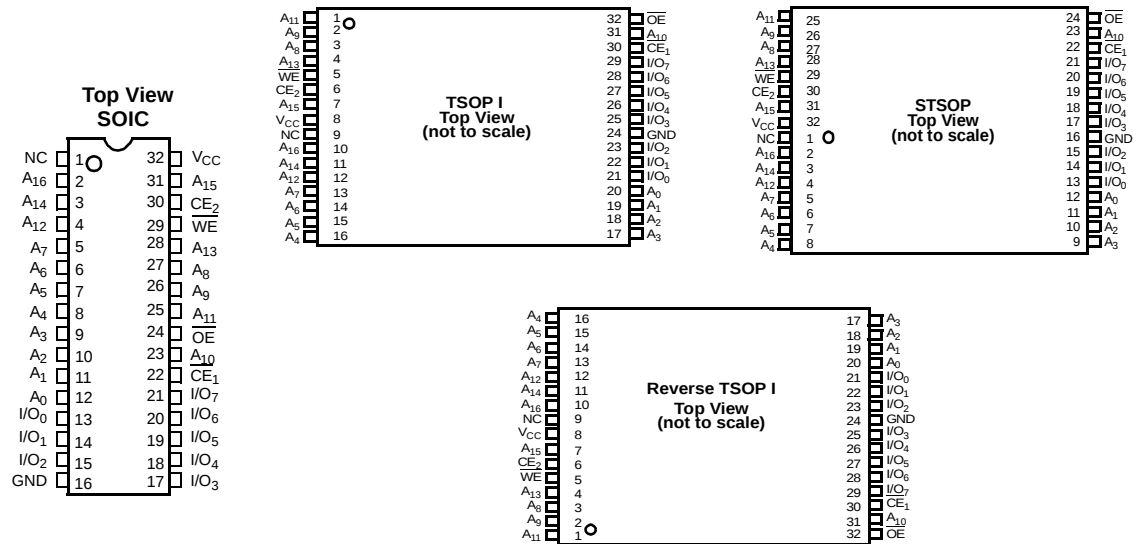
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or $\overline{CE}_2$ LOW), the outputs are disabled ($\overline{OE}$ HIGH) or during a write operation ($\overline{CE}_1$ LOW, $\overline{CE}_2$ HIGH), and $\overline{WE}$ LOW).

Logic Block Diagram



Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration^[2]

Note:

- NC pins are not connected to the die.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential -0.3V to 3.9V

DC Voltage Applied to Outputs in High-Z State^[3] -0.3V to $V_{CC} + 0.3V$

DC Input Voltage^[3] -0.3V to $V_{CC} + 0.3V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC} ^[4]
Industrial	-40°C to +85°C	2.2V to 3.6V

Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating, I _{CC} (mA)				Standby, I _{SB2} (μA)	
	f = 1 MHz		f = f _{MAX}							
	Min.	Typ.	Max.		Typ. ^[5]	Max.	Typ. ^[5]	Max.	Typ. ^[5]	Max.
CY62128DV30L	2.2	3.0	3.6	55/70	0.85	1.5	5	10	1.5	5
CY62128DV30LL				55/70	0.85	1.5	5	10	1.5	4

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		CY62128DV30-55/70			Unit
				Min.	Typ. ^[5]	Max.	
V_{OH}	Output HIGH Voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OH} = -0.1$ mA	2.0			V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OH} = -1.0$ mA	2.4			
V_{OL}	Output LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$	$I_{OL} = 0.1$ mA			0.4	V
		$2.7 \leq V_{CC} \leq 3.6$	$I_{OL} = 2.1$ mA			0.4	
V_{IH}	Input HIGH Voltage	$2.2 \leq V_{CC} \leq 2.7$		1.8		$V_{CC} + 0.3$	V
		$2.7 \leq V_{CC} \leq 3.6$		2.2		$V_{CC} + 0.3$	
V_{IL}	Input LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$		-0.3		0.6	V
		$2.7 \leq V_{CC} \leq 3.6$		-0.3		0.8	
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		-1		+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled		-1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$	$V_{CC} = 3.6V$, $I_{OUT} = 0mA$, CMOS level		5	10	mA
		$f = 1$ MHz			0.85	1.5	
I_{SB1}	Automatic CE Power-down Current – CMOS Inputs	$CE_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$, $f = f_{MAX}$ (Address and Data Only), $f = 0$ (OE, WE,)	L		1.5	5	μA
			LL		1.5	4	
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	$CE_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = 3.6V$	L		1.5	5	μA
			LL		1.5	4	

Capacitance^[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1$ MHz	8	pF
C_{OUT}	Output Capacitance	$V_{CC} = V_{CC(typ)}$	8	pF

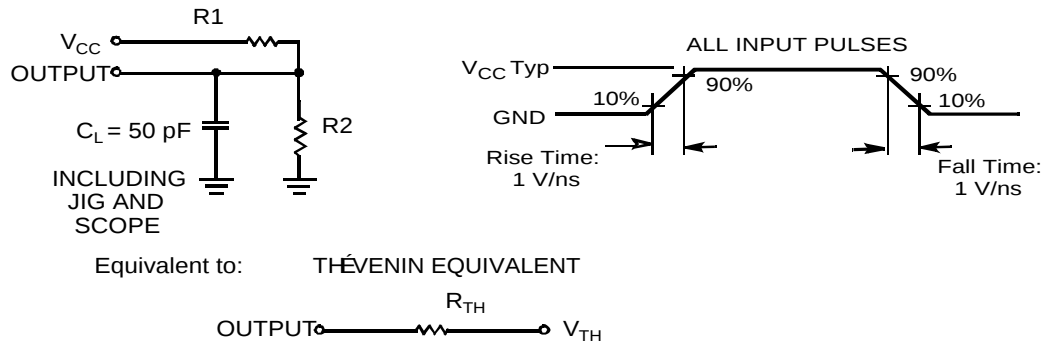
Notes:

- $V_{IL(min.)} = -2.0V$ for pulse durations less than 20 ns., $V_{IH(max.)} = V_{CC} + 0.75V$ for pulse durations less than 20 ns.
- Full device operation requires linear ramp of V_{CC} from 0V to $V_{CC(min)}$ and V_{CC} must be stable at $V_{CC(min)}$ for 500 μs .
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ C$.
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Parameter	Description	Test Conditions	SOIC	TSOP I	STSOP	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient) ^[6]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	69	93	65	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) ^[6]		34	17	15	°C/W

AC Test Loads and Waveforms

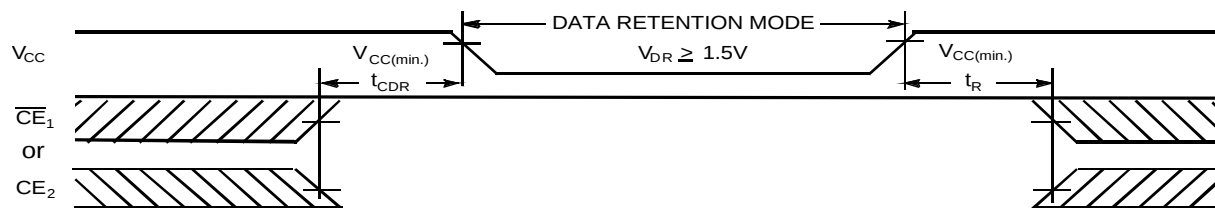


Parameters	2.5V (2.2 – 2.7V)	3.0V (2.7 – 3.6V)	Unit
$R1$	16600	1103	Ω
$R2$	15400	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.2	1.75	V

Data Retention Characteristics

Parameter	Description	Conditions	Min.	Typ. ^[5]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.5V$, $CE_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			4	μA
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0		3	ns
$t_R^{[7]}$	Operation Recovery Time		100			μs

Data Retention Waveform

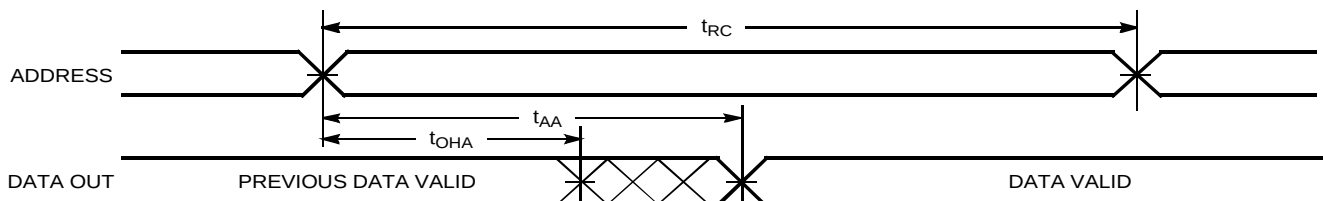


Note:

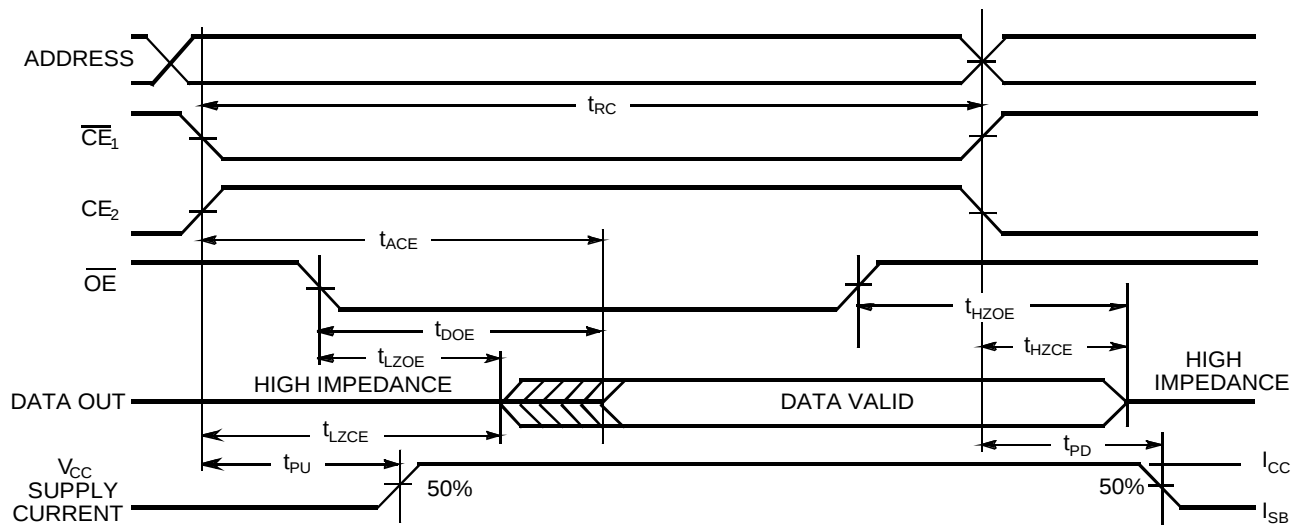
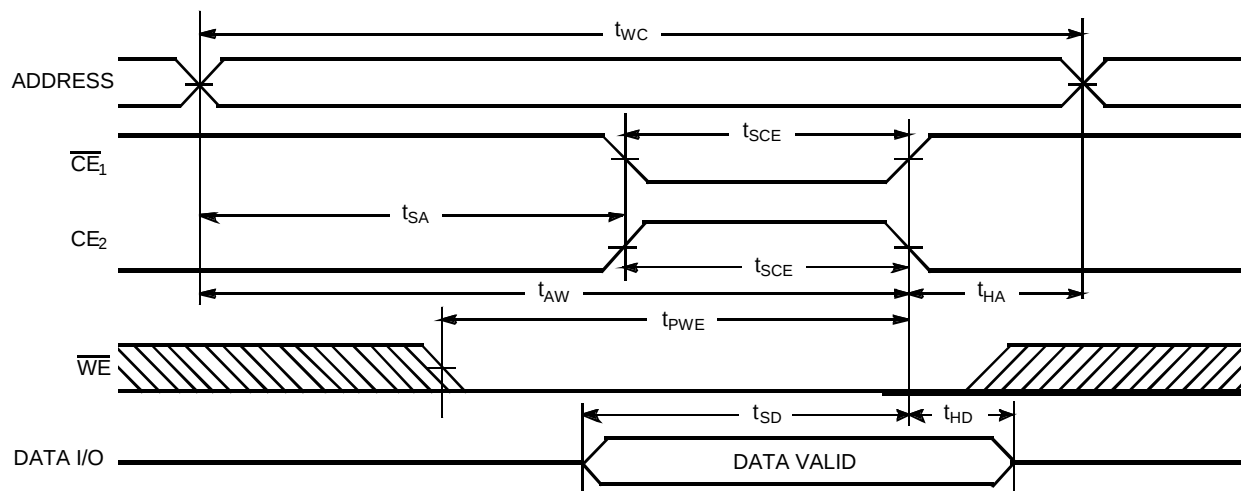
7. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} > 100$ μs .

Switching Characteristics (Over the Operating Range)^[8]

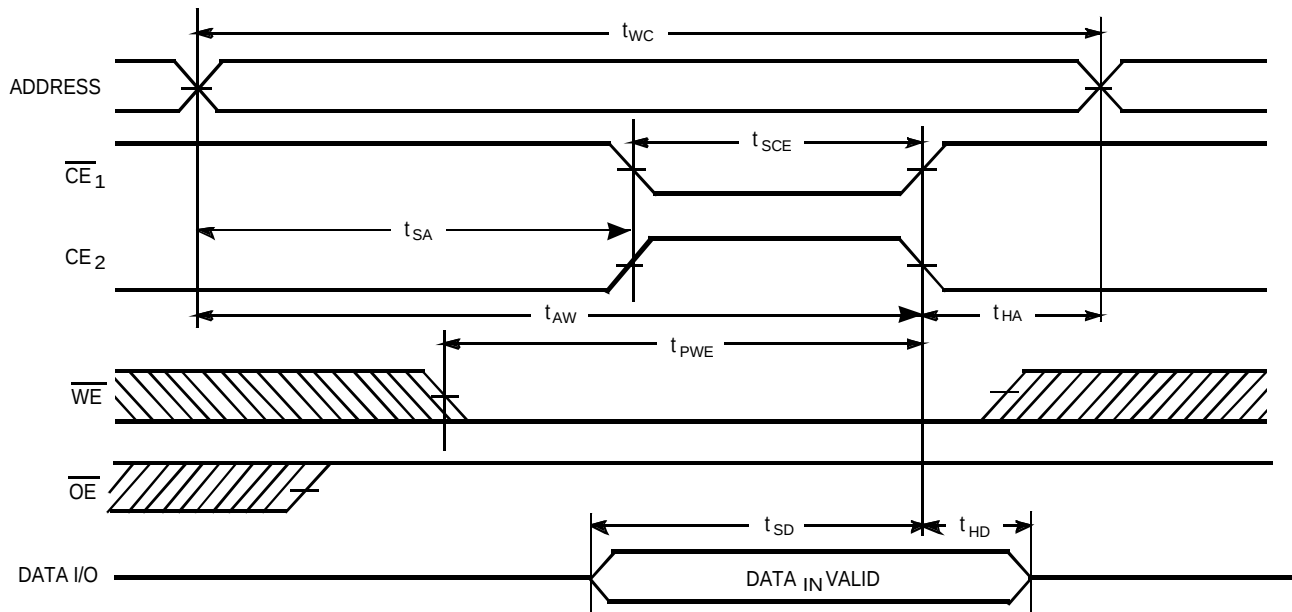
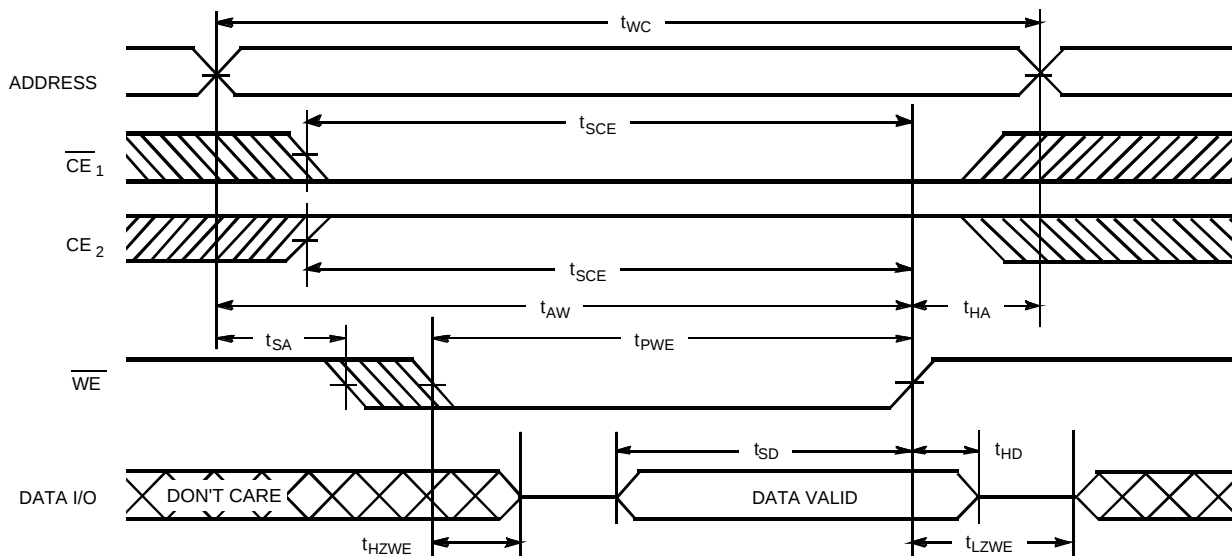
Parameter	Description	CY62128DV30-55		CY62128DV30-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	CE ₁ LOW or CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	OE LOW to Data Valid		25		35	ns
t _{LZOE}	OE LOW to Low Z ^[9]	5		5		ns
t _{HZOE}	OE HIGH to High Z ^[9,10]		20		25	ns
t _{LZCE}	CE ₁ LOW or CE ₂ HIGH to Low Z ^[9]	10		10		ns
t _{HZCE}	CE ₁ HIGH or CE ₂ LOW to High Z ^[9,10]		20		25	ns
t _{PU}	CE ₁ LOW or CE ₂ HIGH to Power-up	0		0		ns
t _{PD}	CE ₁ HIGH or CE ₂ LOW to Power-down		55		70	ns
Write Cycle ^[11]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	CE ₁ LOW or CE ₂ HIGH to Write End	40		60		ns
t _{AW}	Address Set-up to Write End	40		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	WE Pulse Width	40		50		ns
t _{SD}	Data Set-up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	WE LOW to High Z ^[9,10]		20		25	ns
t _{LZWE}	WE HIGH to Low Z ^[9]	10		10		ns

Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled)^[12, 13]

Notes:

8. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL} .
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} .
10. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
11. The internal write time of the memory is defined by the overlap of WE, $CE_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals.
12. Device is continuously selected. $\overline{OE}$, $CE_1 = V_{IL}$, $CE_2 = V_{IH}$.
13. WE is HIGH for Read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 ($\overline{OE}$ Controlled) [10, 13, 14]

Write Cycle No. 1 ($\overline{WE}$ Controlled) [11, 15, 16, 17]

Notes:

14. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.
15. Data I/O is high-impedance if $OE = V_{IH}$.
16. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

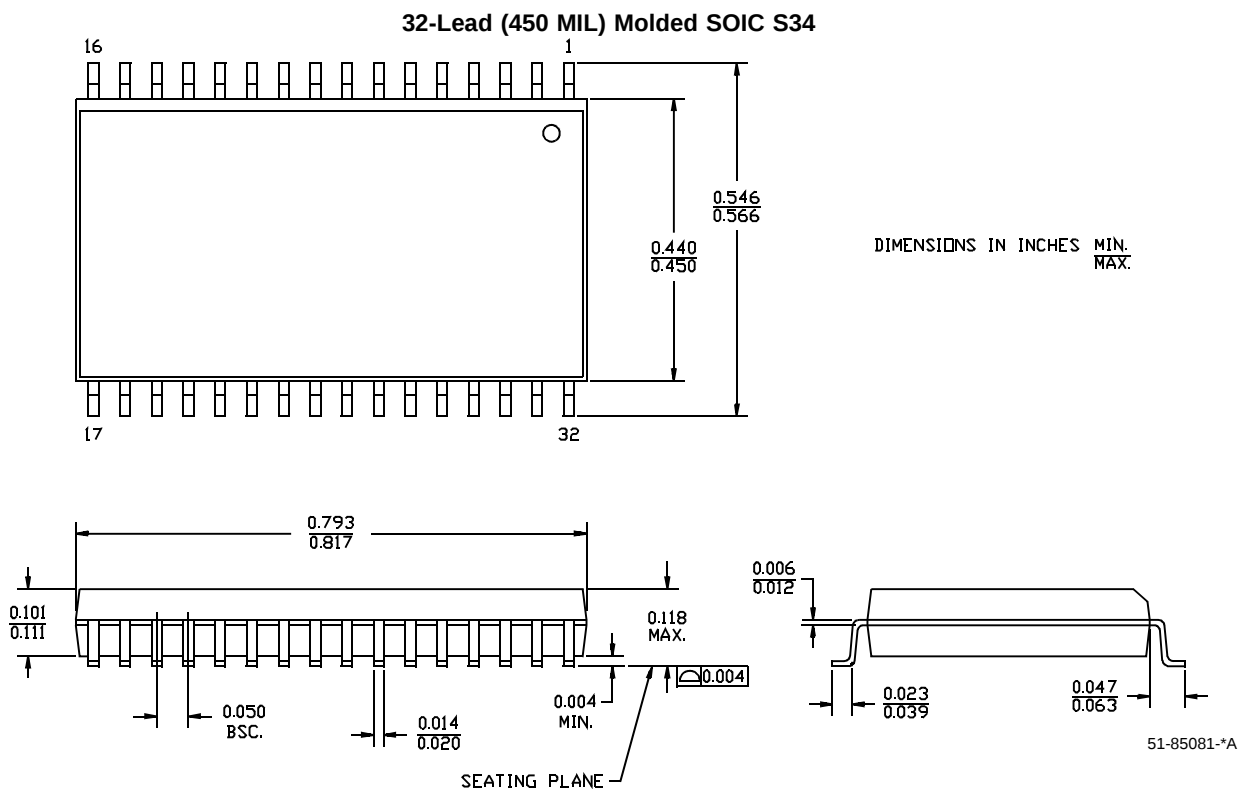
Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{CE}</>_1</>$ or $\overline{CE}</>_2</>$ Controlled) [11, 15, 16, 17]

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [10, 16, 17]

Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	I/O ₀ -I/O ₇	Mode	Power
H	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	Data In	Write	Active (I_{CC})

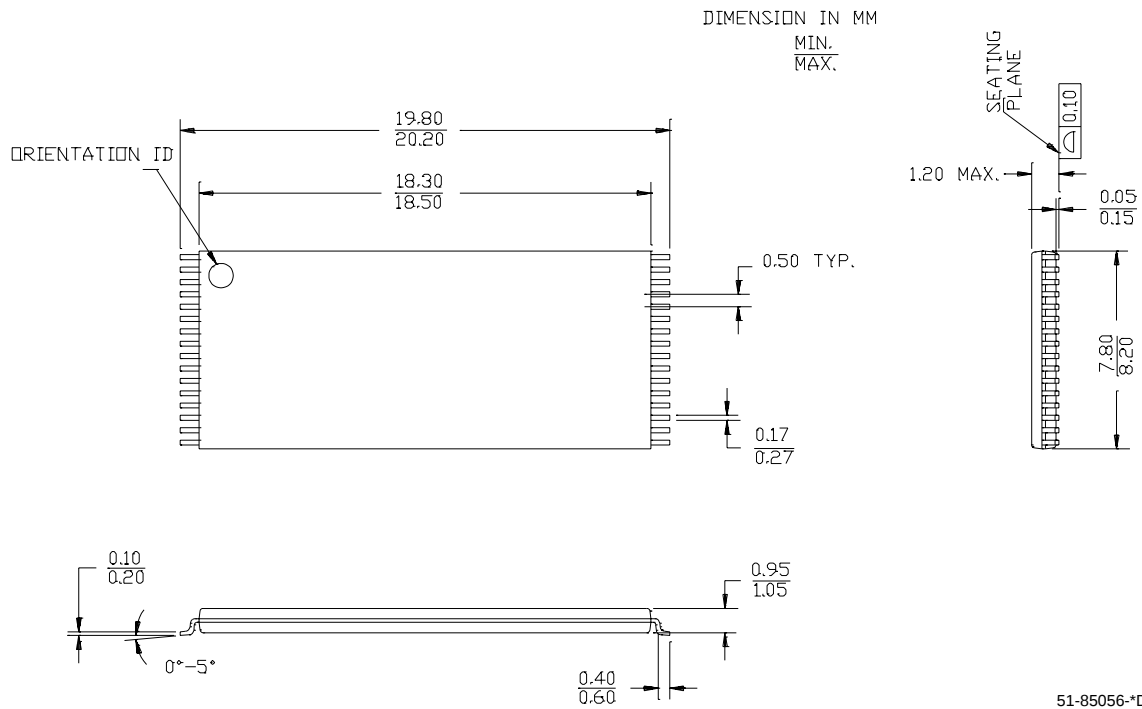
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62128DV30L-55SI	S34	32-lead SOIC	Industrial
	CY62128DV30LL-55SI	S34	32-lead SOIC	
	CY62128DV30L-55ZI	Z32	32-lead TSOP Type 1	
	CY62128DV30LL-55ZI	Z32	32-lead TSOP Type 1	
	CY62128DV30L-55ZAI	ZA32	32-lead Short TSOP Type 1	
	CY62128DV30LL-55ZAI	ZA32	32-lead Short TSOP Type 1	
	CY62128DV30L-55ZRI	ZR32	32-lead Reverse TSOP Type 1	
	CY62128DV30LL-55ZRI	ZR32	32-lead Reverse TSOP Type 1	
70	CY62128DV30L-70SI	S34	32-lead SOIC	Industrial
	CY62128DV30LL-70SI	S34	32-lead SOIC	
	CY62128DV30L-70ZI	Z32	32-lead TSOP Type 1	
	CY62128DV30LL-70ZI	Z32	32-lead TSOP Type 1	
	CY62128DV30L-70ZAI	ZA32	32-lead Short TSOP Type 1	
	CY62128DV30LL-70ZAI	ZA32	32-lead Short TSOP Type 1	
	CY62128DV30L-70ZRI	ZR32	32-lead Reverse TSOP Type 1	
	CY62128DV30LL-70ZRI	ZR32	32-lead Reverse TSOP Type 1	

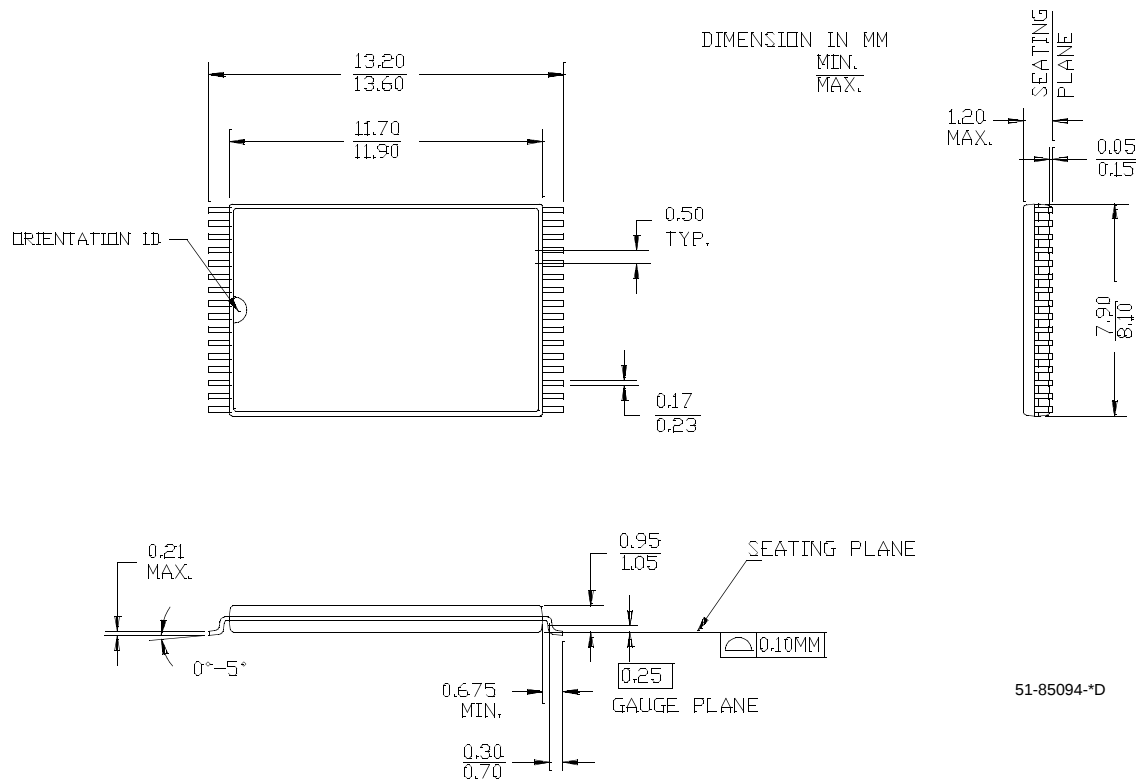
Package Diagrams

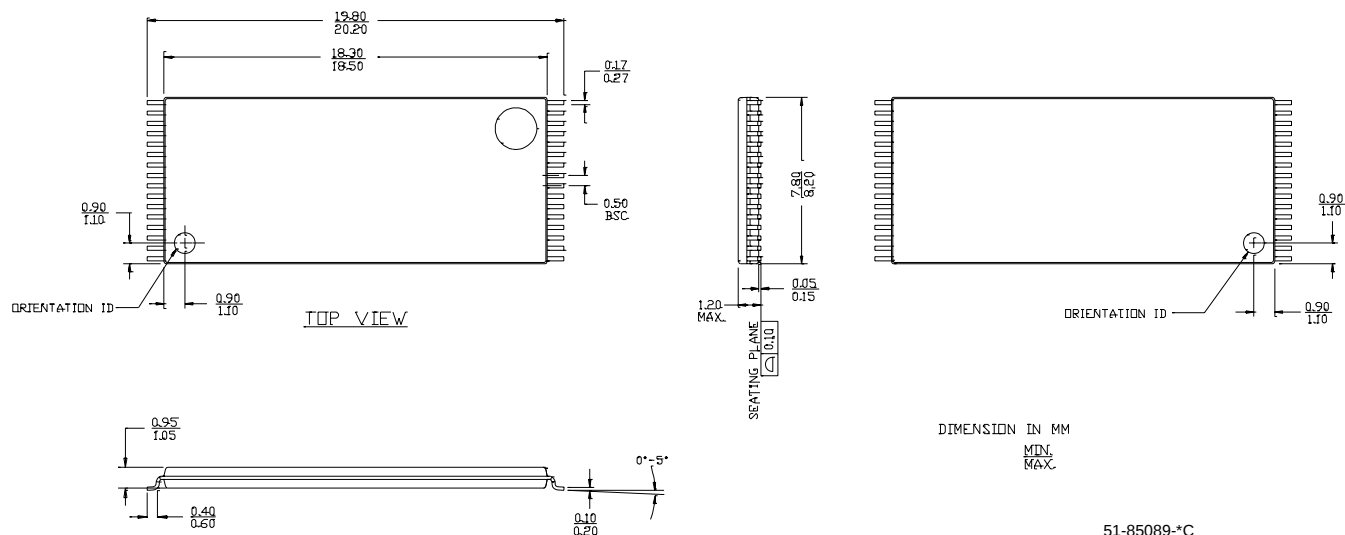


32-Lead Thin Small Outline Package Type I (8 x 20 mm) Z32



32-Lead Shrunk Thin Small Outline Package (8 x 13.4 mm) ZA32



32-Lead Reverse Thin Small Outline Package ZR32


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Document History Page

Document Title: CY62128DV30 MoBL® 1 Mb (128K x 8) Static RAM
Document Number: 38-05231

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	117691	08/27/02	JUI	New Data Sheet
*A	127314	5/27/03	MPR	Changed from Advance Information to Preliminary Changed Isb2 to 5 uA (L), 4 uA (LL) Changed lccdr to 4 uA (L), 3 uA (LL) Changed Cin from 6 pF to 8 pF
*B	128342	07/23/03	JUI	Changed from Preliminary to Final Add 70-ns speed, updated ordering information
*C	129002	08/29/03	CDY	Changed lcc 1 MHz typ from 0.5 mA to 0.85 mA