

2-Mbit (128K x 16) Static RAM

Features

- **Temperature Ranges**
 - Commercial : 0°C to 70°C
 - Industrial : -40°C to 85°C
 - Automotive : -40°C to 125°C
- **High speed: 55 ns and 70 ns**
- **70-ns speed bin offered in both Industrial and Automotive grades**
- **Wide voltage range: 2.7V-3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Package available in a standard 44-pin TSOP Type II (forward pinout) package**

Functional Description^[1]

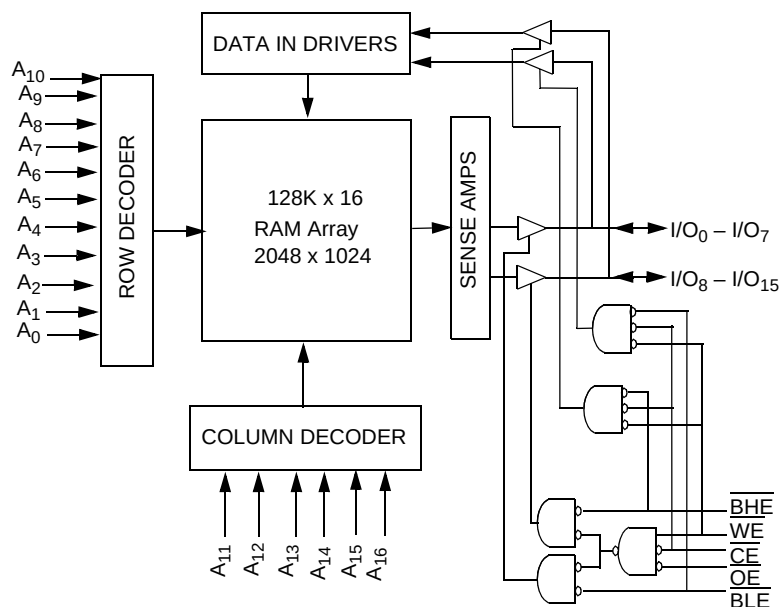
The CY62136V is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current.

This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}$ HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₆). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the Truth Table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram



Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product	V _{CC} Range (V)			Speed	Grades	Power Dissipation (Industrial)			
						Operating, I _{CC} (mA)		Standby, I _{SB2} (μA)	
	Min	Typ. ^[2]	Max			Typ. ^[2]	Maximum	Typ. ^[2]	Maximum
CY62136VLL	2.7	3.0	3.6	55	Industrial	7	20	1	15
				70	Industrial	7	15	1	15
					Automotive	7	20	1	20
CY62136VSL	2.7	3.0	3.6	55	Industrial	7	20	1	5
				70	Industrial	7	15	1	5

Pin Configurations^[3]

**TSOP II (Forward)
Top View**

A ₄	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	OE
A ₀	5	40	BHE
CE	6	39	BLE
I/O ₀	7	38	I/O ₁₅
I/O ₁	8	37	I/O ₁₄
I/O ₂	9	36	I/O ₁₃
I/O ₃	10	35	I/O ₁₂
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
I/O ₄	13	32	I/O ₁₁
I/O ₅	14	31	I/O ₁₀
I/O ₆	15	30	I/O ₉
I/O ₇	16	29	I/O ₈
WE	17	28	NC
A ₁₆	18	27	A ₈
A ₁₅	19	26	A ₉
A ₁₄	20	25	A ₁₀
A ₁₃	21	24	A ₁₁
A ₁₂	22	23	NC

Notes:

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25°C.
3. NC pins are not connected on the die

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State^[4] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[4] -0.5V to $V_{CC} + 0.5V$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature T_A ^[6]	V_{CC}
Industrial	-40°C to +85°C	2.7V to 3.6V
Automotive	-40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62136V-55			CY62136V-70			Unit	
				Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.		
V _{OH}	Output HIGH Voltage	I _{OH} = −1.0 mA	V _{CC} = 2.7V	2.4			2.4			V	
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = 2.7V			0.4			0.4	V	
V _{IH}	Input HIGH Voltage		V _{CC} = 3.6V	2.2		V _{CC} +0.5V	2.2		V _{CC} +0.5V	V	
V _{IL}	Input LOW Voltage		V _{CC} = 2.7V	−0.5		0.8	−0.5		0.8	V	
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		Industrial	−1	+1	−1		+1	μA	
				Automotive			−10		+10	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		Industrial	−1	+1	−1		+1	μA	
				Automotive			−10		+10	μA	
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} ,	V _{CC} = 3.6V, I _{OUT} = 0 mA, CMOS Levels	Industrial		7	20		7	15	mA
				Automotive					7	20	mA
		f = 1 MHz,				1	2		1	2	mA
I _{SB1}	Automatic CE Power-down Current— CMOS Inputs	CE ≥ V _{CC} −0.3V, V _{IN} ≥ V _{CC} −0.3V or V _{IN} ≤ 0.3V, f = f _{MAX}				100			100	μA	
I _{SB2}	Automatic CE Power-down Current— CMOS Inputs	CE ≥ V _{CC} −0.3V V _{IN} ≥ V _{CC} −0.3V or V _{IN} ≤ 0.3V, f = 0	V _{CC} = 3.6V	Industrial(LL)		1	15		1	15	μA
				Industrial(SL)		1	5		1	5	μA
				Automotive					1	20	μA

Thermal Resistance

Parameter	Description	Test Conditions	TSOPII	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient) ^[5]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	60	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case) ^[5]		22	°C/W

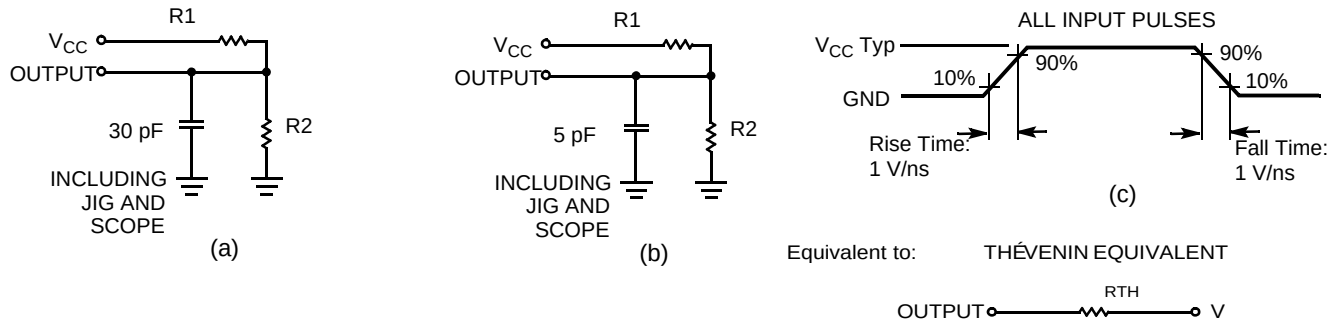
Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1 \text{ MHz}$, $V_{CC} = V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

- $V_{IL(min)}$ = -2.0V for pulse durations less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.
- T_A is the "Instant-On" case temperature.

AC Test Loads and Waveforms

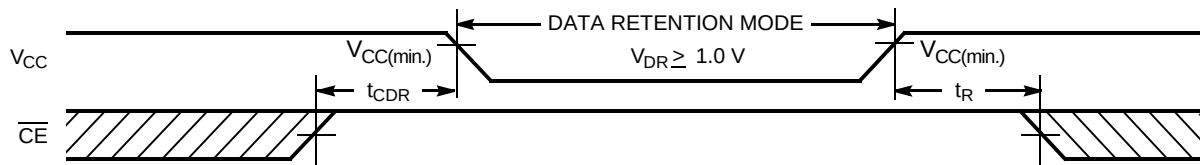


Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[8]	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		3.6	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, No input may exceed $V_{CC} + 0.3V$	LL	0.5	7.5	μA
			SL		5	
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[7]}$	Operation Recovery Time		70			ns

Data Retention Waveform



Switching Characteristics Over the Operating Range^[8]

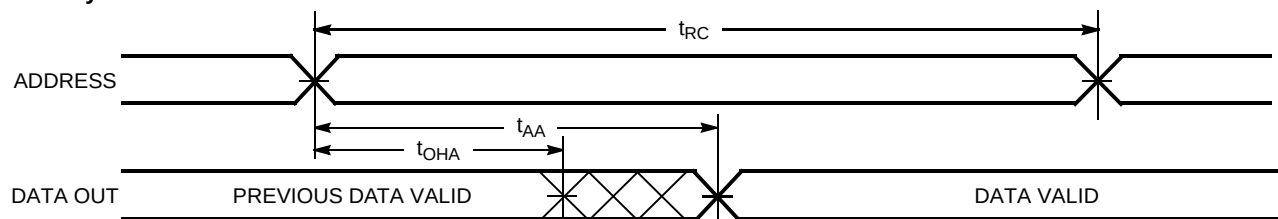
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	CE LOW to Data Valid		55		70	ns
t _{DOE}	OE LOW to Data Valid		25		35	ns
t _{LZOE}	OE LOW to Low-Z ^[9]	5		5		ns

Notes:

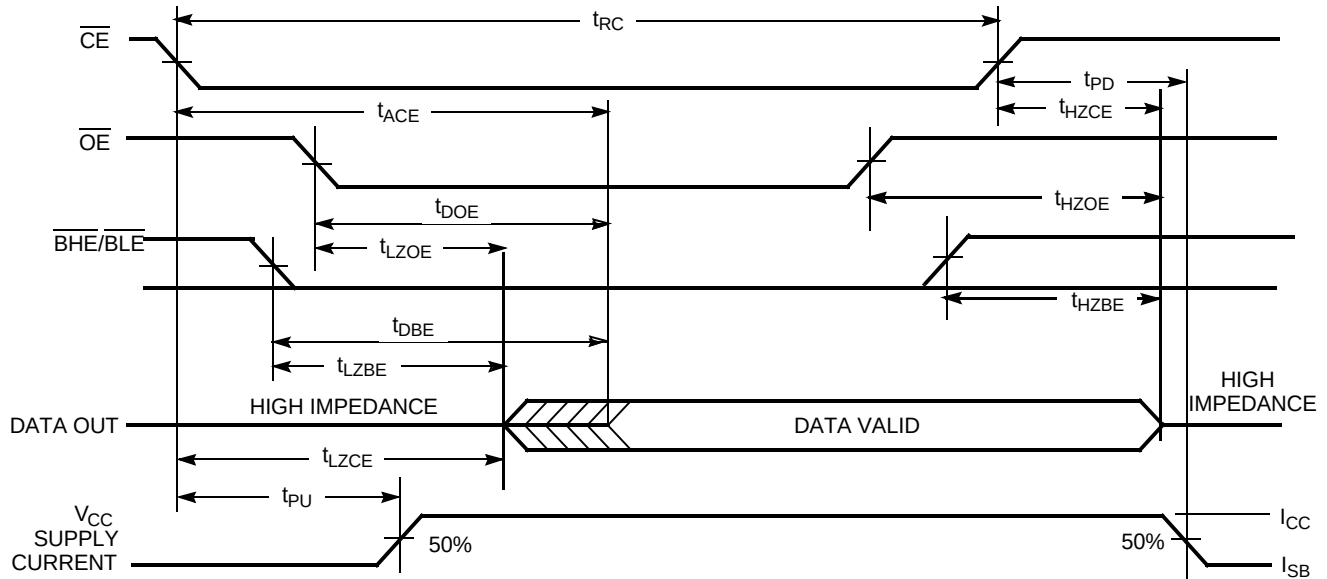
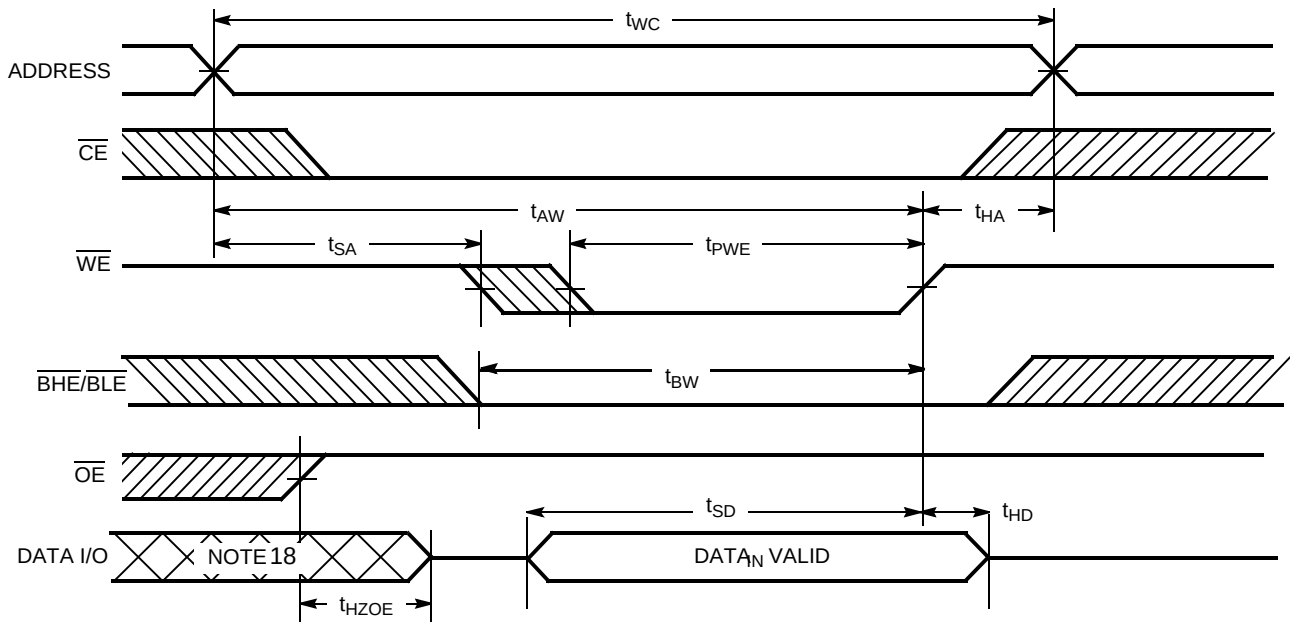
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ ms or stable at $V_{CC(min)} \geq 100$ ms.
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V_{CC} typ., and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.

Switching Characteristics Over the Operating Range (continued)^[8]

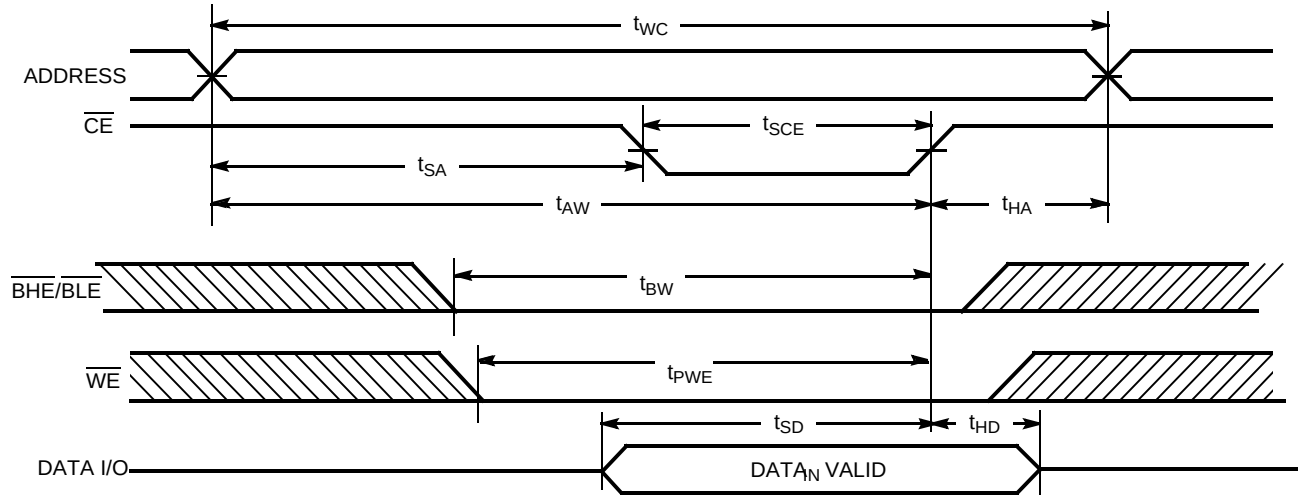
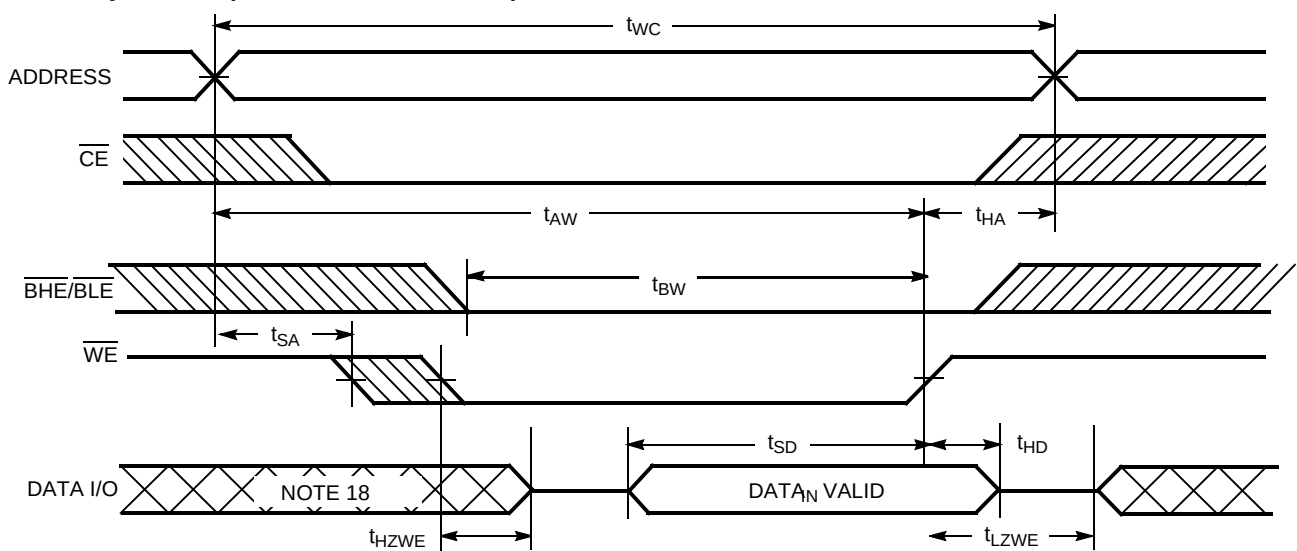
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t_{HZOE}	OE HIGH to High-Z ^[9, 10]		25		25	ns
t_{LZCE}	CE LOW to Low-Z ^[9]	10		10		ns
t_{HZCE}	CE HIGH to High-Z ^[9, 10]		25		25	ns
t_{PU}	CE LOW to Power-up	0		0		ns
t_{PD}	CE HIGH to Power-down		55		70	ns
t_{DBE}	BLE / BHE LOW to Data Valid		25		35	ns
t_{LZBE}	BLE / BHE LOW to Low-Z ^[9, 10]	5		5		ns
t_{HZBE}	BLE / BHE HIGH to High-Z ^[11]		25		25	ns
Write Cycle^[11, 12]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	CE LOW to Write End	45		60		ns
t_{AW}	Address Set-up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	WE Pulse Width	40		50		ns
t_{BW}	BLE / BHE LOW to Write End	50		60		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	WE LOW to High-Z ^[9, 10]		20		25	ns
t_{LZWE}	WE HIGH to Low-Z ^[9]	5		10		ns

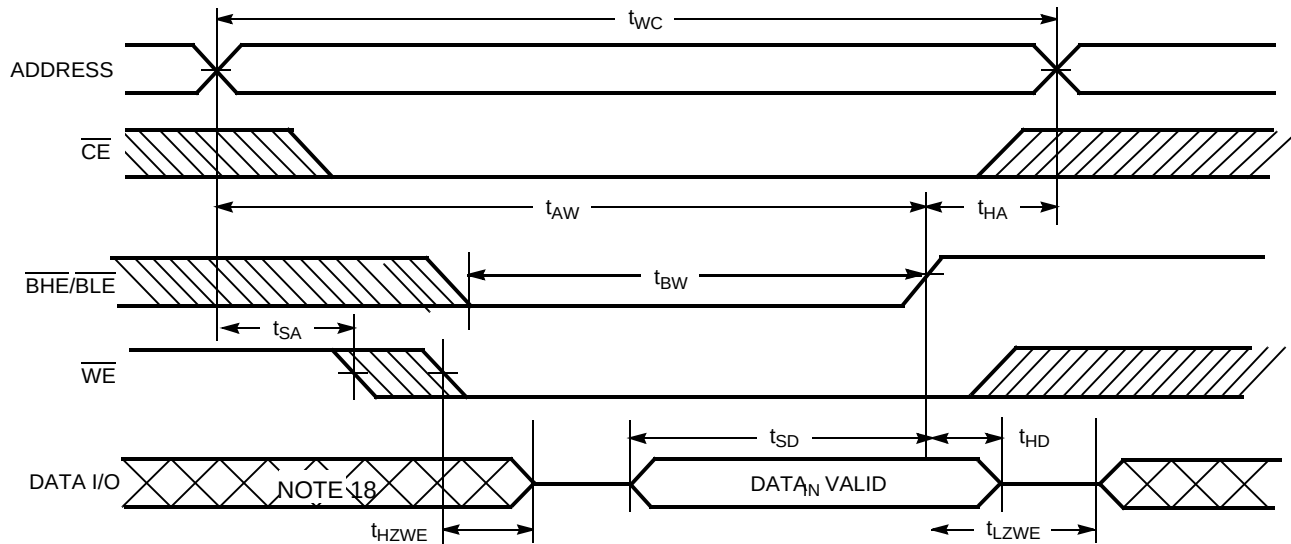
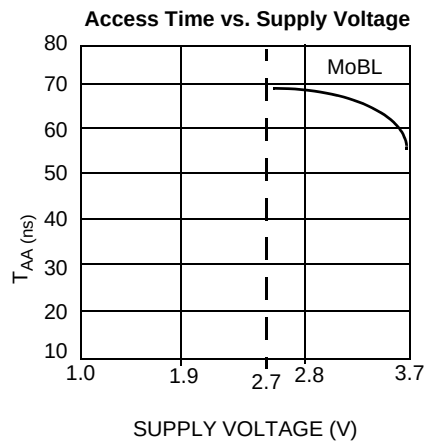
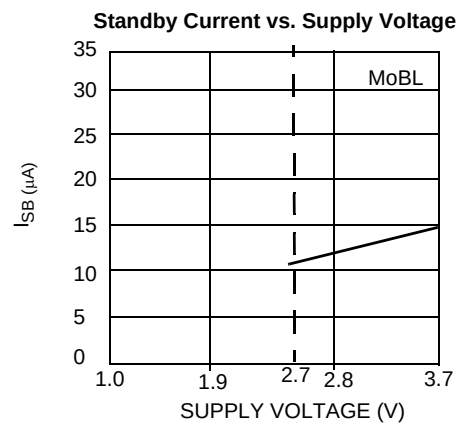
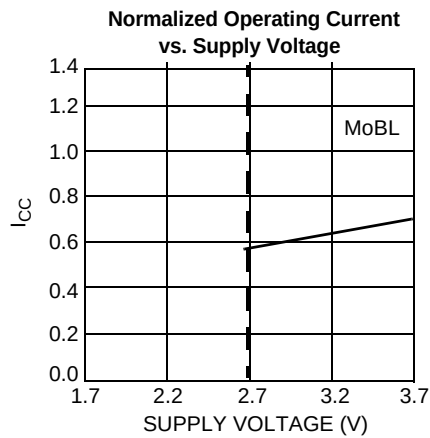
Switching Waveforms
Read Cycle No. 1^[13, 14]

Notes:

11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. The minimum write cycle time for write cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .
13. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
14. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 [14, 15]

Write Cycle No. 1 (WE Controlled) [11, 16, 17]

Notes:

15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. Data I/O is high impedance if $OE = V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) ^[11, 16, 17]

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) ^[12, 17]


Switching Waveforms (continued)
Write Cycle No. 4 (BHE/BL_E Controlled, $\overline{\text{OE}}$ LOW)^[18]

Typical DC and AC Characteristics


Truth Table

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High-Z	Read	Active (I_{CC})
L	H	L	H	H	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High-Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62136VLL-55ZSI	ZS44	44-pin TSOP II	Industrial
	CY62136VSL-55ZSI			Industrial
70	CY62136VLL-70ZSI			Industrial
	CY62136VLL-70ZSE			Automotive
	CY62136VSL-70ZSI			Industrial



44-pin TSOP II ZS44

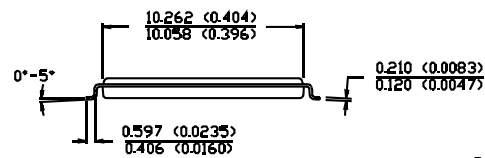
22 1 PIN 1 L.D.

11.938 (0.470)

11.735 (0.462)

23 44

Diagram of the front view of the 100-pin connector. The connector is rectangular with a top row of 100 pins and a bottom row of 100 pins. The overall height is 0.262 (0.404) and the width is 0.058 (0.396). A circular feature labeled 'EJECTOR PIN' is located on the right side.



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Document History Page

Document Title: CY62136V MoBL [®] 2-Mbit (128K x 16) Static RAM Document Number: 38-05087				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107347	05/25/01	SZV	Changed from Spec #: 38-00728 to 38-05087
*A	116509	09/04/02	GBI	Added footnote 1 Added SL power bin Deleted fBGA package; replacement fBGA package available in CY62136CV30
*B	269729	See ECN	SYT	Added Automotive Information for 70-ns Speed Bin. Added Footnotes # 3 and # 6. Corrected Typo in Electrical Characteristics for I _{CC} (Max)-55 ns from 15 to 20 mA. Added SL row for I _{SB2} in the Electrical Characteristics table. Changed Package Name from Z44 to ZS44. Replaced 'Z' with 'ZS' in the Ordering Code.