

256K x 8 Static RAM

Features

- Low voltage range:
— 2.7–3.6V
- Ultra-low active power
- Low standby power
- Easy memory expansion with $\overline{CS}_1/\overline{CS}_2$ and \overline{OE} features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power

Functional Description

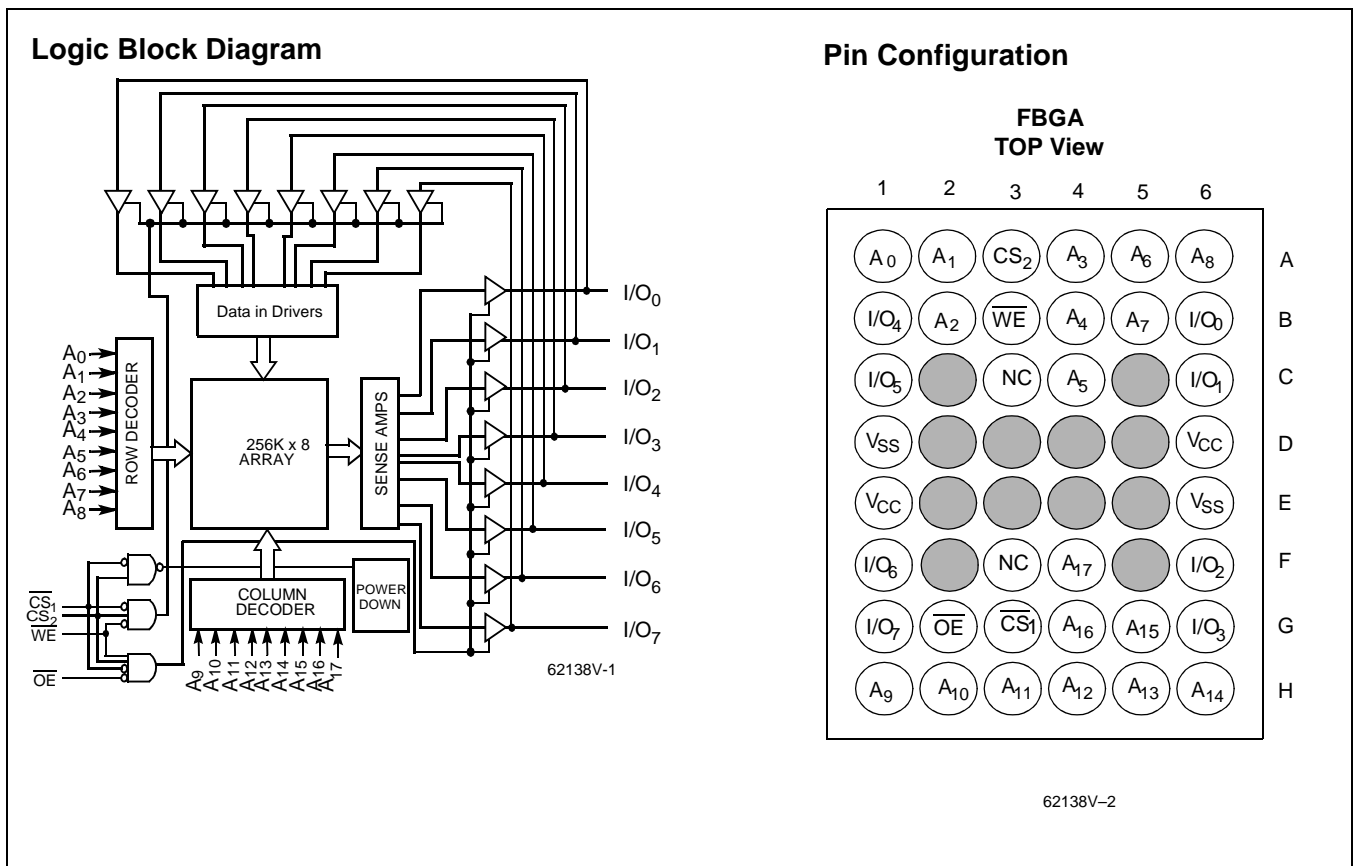
The CY62138V is a high-performance CMOS static RAM organized as 262,144 words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that reduces power consumption by 99% when addresses are not toggling. The device can be put into standby mode when deselected (\overline{CS}_1 HIGH or \overline{CS}_2 LOW).

Writing to the device is accomplished by taking Chip Enable One (\overline{CS}_1) and Write Enable (WE) inputs LOW and Chip Enable Two (\overline{CS}_2) HIGH. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₇).

Reading from the device is accomplished by taking Chip Enable One (\overline{CS}_1) and Output Enable (\overline{OE}) LOW while forcing Write Enable (WE) and Chip Enable Two (\overline{CS}_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CS}_1 HIGH or \overline{CS}_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CS}_1 LOW, \overline{CS}_2 HIGH, and WE LOW).

The CY62138V is available in a 36-ball FBGA.



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +4.6V
DC Voltage Applied to Outputs in High Z State ^[1]	-0.5V to $V_{CC} + 0.5V$

DC Input Voltage ^[1]	-0.5V to $V_{CC} + 0.5V$
Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current.....	>200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62138V	Industrial	-40°C to +85°C	2.7V to 3.6V

Product Portfolio

Product	V_{CC} Range			Speed	Power Dissipation (Industrial)			
	$V_{CC}(\text{min})$	$V_{CC}(\text{typ})$ ^[2]	$V_{CC}(\text{max})$		Operating (I_{CC})		Standby (I_{SB2})	
					Typ. ^[2]	Maximum	Typ. ^[2]	Maximum
CY62138V	2.7V	3.0V	3.6V	70 ns	7 mA	15 mA	1 μ A	15 μ A

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62138V			Unit
				Min.	Typ. ^[2]	Max.	
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0 \text{ mA}$	$V_{CC} = 2.7V$	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$	$V_{CC} = 2.7V$			0.4	V
V_{IH}	Input HIGH Voltage		$V_{CC} = 3.6V$	2.2		$V_{CC} + 0.5V$	V
V_{IL}	Input LOW Voltage		$V_{CC} = 2.7V$	-0.5		0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$		-1	± 1	+1	μ A
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled		-1	+1	+1	μ A
I_{CC}	V_{CC} Operating Supply Current	$I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{RC}$, CMOS Levels	$V_{CC} = 3.6V$		7	15	mA
		$I_{OUT} = 0 \text{ mA}$, $f = 1 \text{ MHz}$, CMOS Levels			1	2	mA
I_{SB1}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = f_{MAX}$				100	μ A
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$	$V_{CC} = 3.6V$	LL		1	15 μ A

Notes:

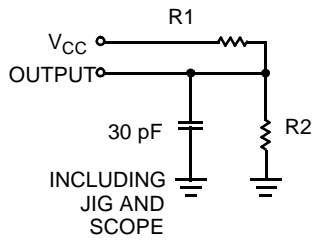
- $V_{IL}(\text{min}) = -2.0V$ for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC} \text{ Typ}$, $T_A = 25^\circ\text{C}$.

Capacitance^[3]

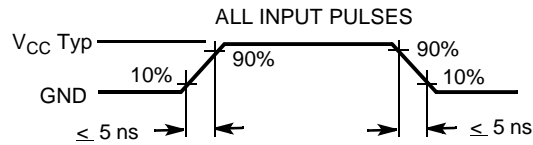
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = V_{CC}(\text{typ})$	6	pF
C_{OUT}	Output Capacitance		8	pF

Note:

- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


62138V-3



62138V-4

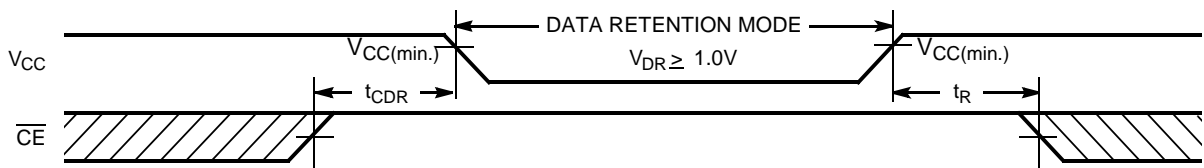
Equivalent to: THÉVENIN EQUIVALENT



Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[4]	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		3.6	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$ $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ No input may exceed $V_{CC} + 0.3V$	LL	0.1	5	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns
t_R	Operation Recovery Time		100			μs

Data Retention Waveform^[5]


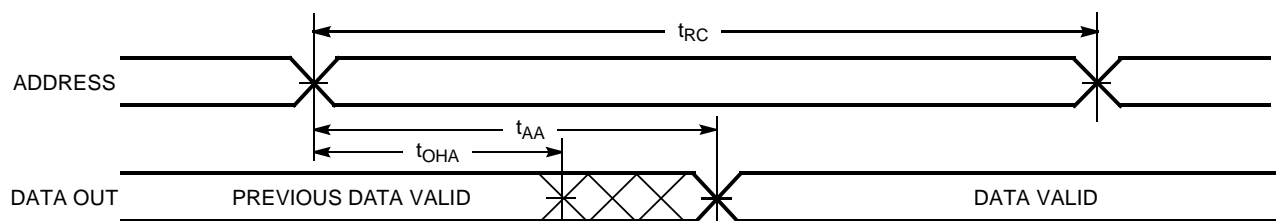
62128V-5

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V_{CC} typ., and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- CE is the combination of both CS_1 and CS_2 .

Switching Characteristics Over the Operating Range^[4]

Parameter	Description	70 ns		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	\overline{CE} LOW to Data Valid		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		35	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[6]	5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		25	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	10		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		25	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		70	ns
WRITE CYCLE^[8, 9]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	\overline{CE} LOW to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	\overline{WE} Pulse Width	50		ns
t_{SD}	Data Set-Up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		25	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	10		ns

Switching Waveforms
Read Cycle No. 1^[10, 11]


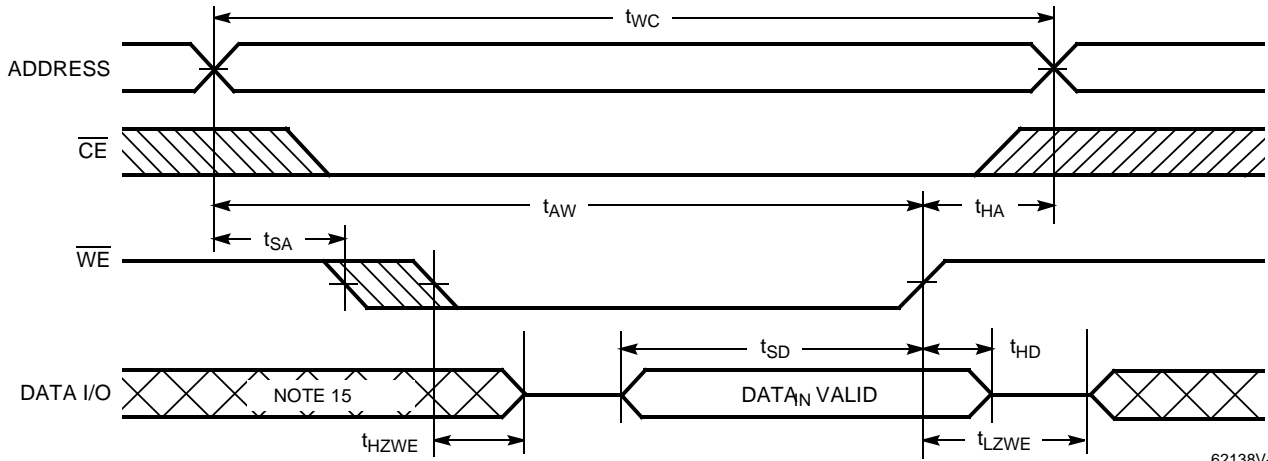
C62138V-5

Notes:

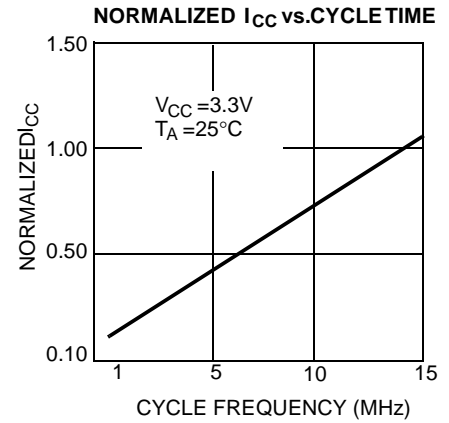
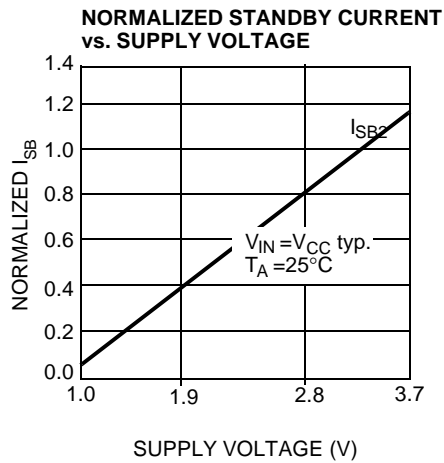
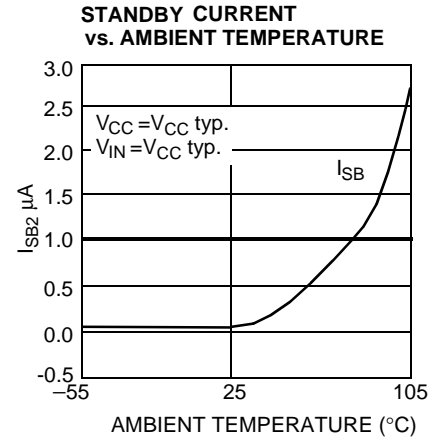
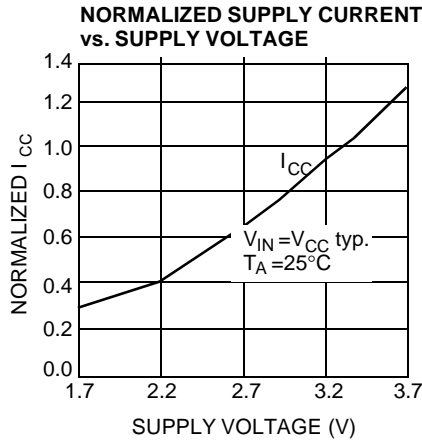
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} ; t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .
10. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
11. \overline{WE} is HIGH for read cycle.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [5, 9, 14]



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Typical DC and AC Characteristics

Truth Table

CS₁	CS₂	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	L	X	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})



Document Title: CY62138V MoBL™ 256K x 8 Static RAM Document Number: 38-05088				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107348	06/12/01	SZV	Change from Spec #: 38-00729 to 38-05088