



## 128K x 16 Static RAM

### Features

- 3.0 – 3.6V Operation
- High speed
  - $t_{AA} = 12, 15 \text{ ns}$
- CMOS for optimum speed/power
- Low active power
  - 684 mW (Max.)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in 44-pin TSOP II

### Functional Description

The CY7C1011BV33 is a high-performance CMOS static RAM organized as 131,072 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable

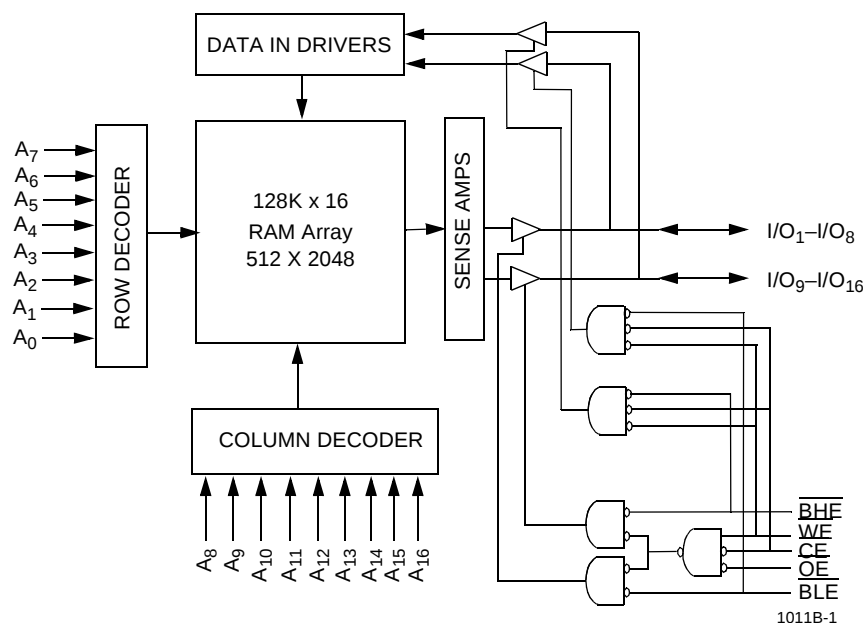
( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_1$  through  $I/O_8$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_9$  through  $I/O_{16}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_1$  to  $I/O_8$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_9$  to  $I/O_{16}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

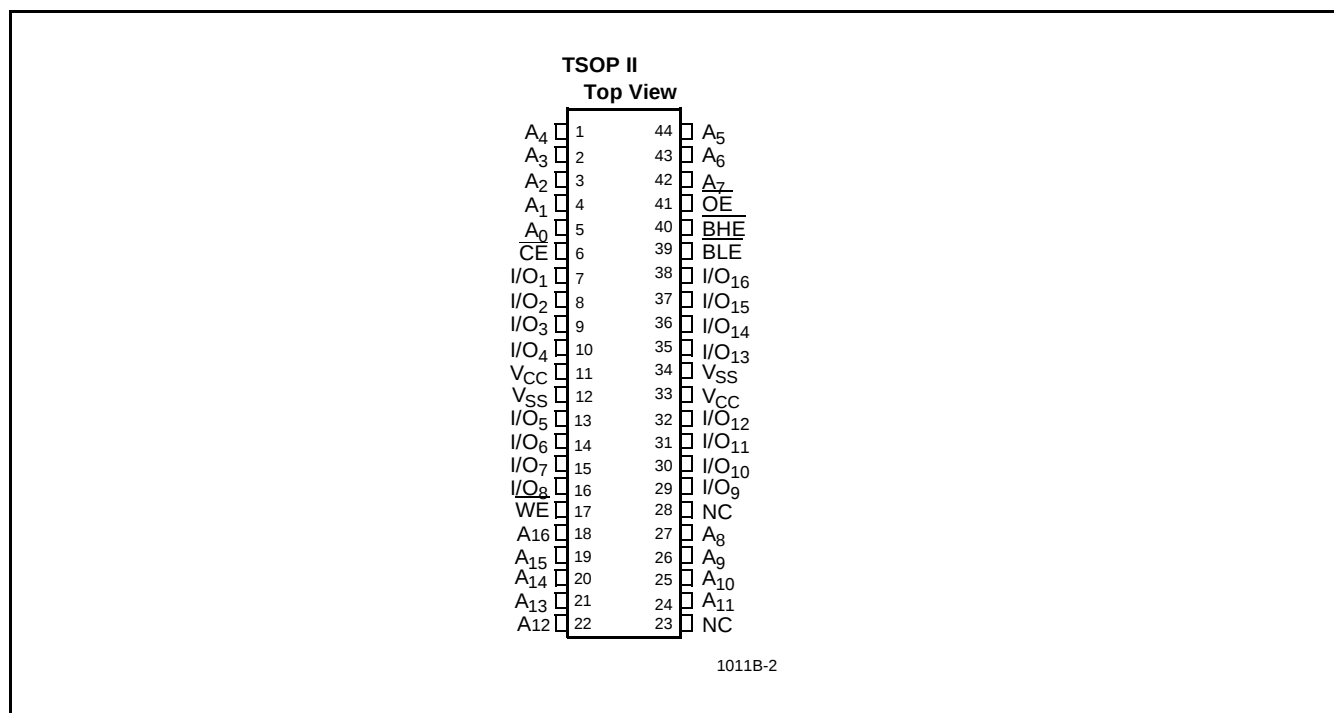
The input/output pins ( $I/O_1$  through  $I/O_{16}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1011BV33 is available in standard 44-pin TSOP Type II package.

### Logic Block Diagram



## Pin Configuration



## Selection Guide

|                                   |            | 1011BV33-12 | 1011BV33-15 |
|-----------------------------------|------------|-------------|-------------|
| Maximum Access Time (ns)          | Commercial | 12          | 15          |
| Maximum Operating Current (mA)    | Commercial | 190         | 170         |
| Maximum CMOS Standby Current (mA) | Commercial | 10          | 10          |
|                                   |            |             |             |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs  
in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub>+0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub>+0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

## Operating Range

| Range      | Ambient Temperature <sup>[2]</sup> | V <sub>CC</sub> |
|------------|------------------------------------|-----------------|
| Commercial | 0°C to +70°C                       | 3.3V ± 10%      |
| Industrial | -40°C to +85°C                     | 3.3V ± 10%      |

## Electrical Characteristics Over the Operating Range

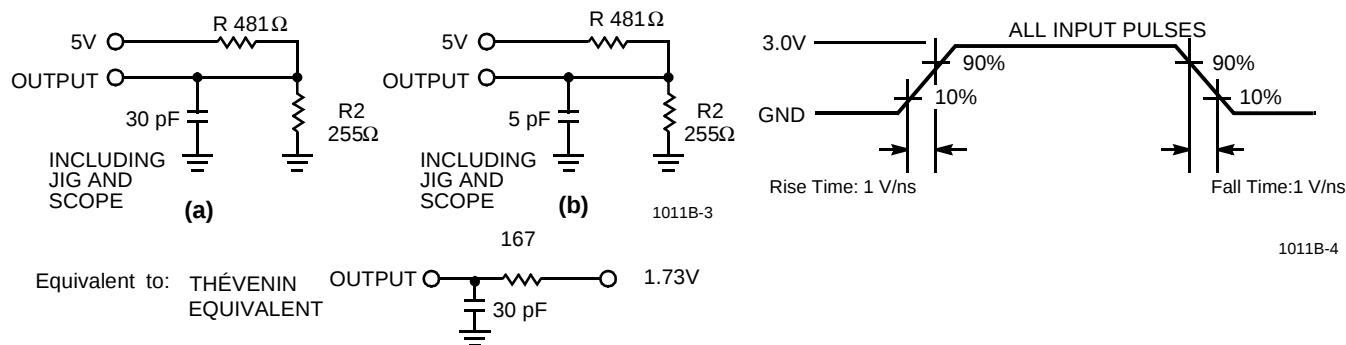
| Parameter       | Description         | Test Conditions                                      | 1011BV33-12 |      | 1011BV33-15 |      | Unit |
|-----------------|---------------------|------------------------------------------------------|-------------|------|-------------|------|------|
|                 |                     |                                                      | Min.        | Max. | Min.        | Max. |      |
| V <sub>OH</sub> | Output HIGH Voltage | V <sub>CC</sub> = Min.,<br>I <sub>OH</sub> = -4.0 mA | 2.4         |      | 2.4         |      | V    |
| V <sub>OL</sub> | Output LOW Voltage  | V <sub>CC</sub> = Min.,<br>I <sub>OL</sub> = 8.0 mA  |             | 0.4  |             | 0.4  | V    |

**Electrical Characteristics** Over the Operating Range (continued)

| Parameter | Description                                  | Test Conditions                                                                                               | 1011BV33-12 |      | 1011BV33-15 |      | Unit    |
|-----------|----------------------------------------------|---------------------------------------------------------------------------------------------------------------|-------------|------|-------------|------|---------|
|           |                                              |                                                                                                               | Min.        | Max. | Min.        | Max. |         |
| $V_{IH}$  | Input HIGH Voltage                           |                                                                                                               | 2.2         |      | 2.2         |      | V       |
| $V_{IL}$  | Input LOW Voltage <sup>[1]</sup>             |                                                                                                               | -0.3        | 0.8  | -0.3        | 0.8  | V       |
| $I_{IX}$  | Input Load Current                           | $GND \leq V_I \leq V_{CC}$                                                                                    | -1          | +1   | -1          | +1   | $\mu A$ |
| $I_{OZ}$  | Output Leakage Current                       | $GND \leq V_I \leq V_{CC}$ ,<br>Output Disabled                                                               | -1          | +1   | -1          | +1   | $\mu A$ |
| $I_{OS}$  | Output Short Circuit Current <sup>[3]</sup>  | $V_{CC} = \text{Max.}$ ,<br>$V_{OUT} = GND$                                                                   |             | -300 |             | -300 | mA      |
| $I_{CC}$  | $V_{CC}$ Operating Supply Current            | $V_{CC} = \text{Max.}$ ,<br>$I_{OUT} = 0 \text{ mA}$ ,<br>$f = f_{MAX} = 1/t_{RC}$                            |             | 190  |             | 170  | mA      |
| $I_{SB1}$ | Automatic CE Power-Down Current —TTL Inputs  | Max. $V_{CC}$ ,<br>$CE \geq V_{IH}$<br>$V_{IN} \geq V_{IH}$ or<br>$V_{IN} \leq V_{IL}$ ,<br>$f = f_{MAX}$     |             | 40   |             | 40   | mA      |
| $I_{SB2}$ | Automatic CE Power-Down Current —CMOS Inputs | Max. $V_{CC}$ ,<br>$CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ ,<br>or $V_{IN} \leq 0.3V$ , $f = 0$ |             | 10   |             | 10   | mA      |
|           |                                              | L                                                                                                             |             | 0.5  |             | 0.5  |         |

**Capacitance<sup>[4]</sup>**

| Parameter | Description        | Test Conditions                                               | Max. | Unit |
|-----------|--------------------|---------------------------------------------------------------|------|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ C$ , $f = 1 \text{ MHz}$ ,<br>$V_{CC} = 5.0V$ | 8    | pF   |
| $C_{OUT}$ | Output Capacitance |                                                               | 8    | pF   |

**AC Test Loads and Waveforms**

**Notes:**

- $V_{IL}(\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- $T_A$  is the "instant on" case temperature.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**Switching Characteristics<sup>[5]</sup> Over the Operating Range**

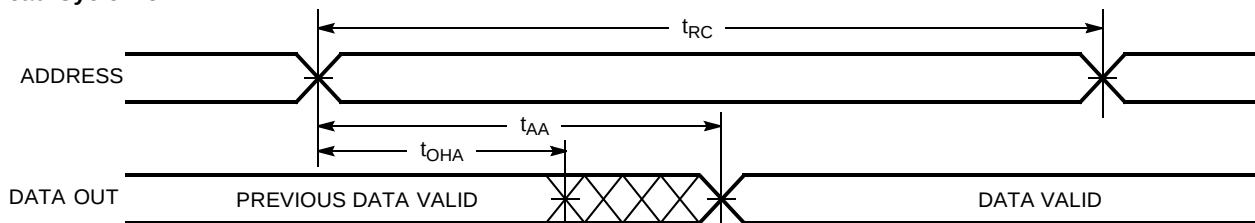
| Parameter         | Description                         | 1011BV33-12 |      | 1011BV33-15 |      | Unit |
|-------------------|-------------------------------------|-------------|------|-------------|------|------|
|                   |                                     | Min.        | Max. | Min.        | Max. |      |
| READ CYCLE        |                                     |             |      |             |      |      |
| t <sub>RC</sub>   | Read Cycle Time                     | 12          |      | 15          |      | ns   |
| t <sub>AA</sub>   | Address to Data Valid               |             | 12   |             | 15   | ns   |
| t <sub>OHA</sub>  | Data Hold from Address Change       | 3           |      | 3           |      | ns   |
| t <sub>ACE</sub>  | CE LOW to Data Valid                |             | 12   |             | 15   | ns   |
| t <sub>DOE</sub>  | OE LOW to Data Valid                |             | 6    |             | 7    | ns   |
| t <sub>LZOE</sub> | OE LOW to Low Z <sup>[6]</sup>      | 0           |      | 0           |      | ns   |
| t <sub>HZOE</sub> | OE HIGH to High Z <sup>[6, 7]</sup> |             | 6    |             | 7    | ns   |
| t <sub>LZCE</sub> | CE LOW to Low Z <sup>[6]</sup>      | 3           |      | 3           |      | ns   |
| t <sub>HZCE</sub> | CE HIGH to High Z <sup>[6, 7]</sup> |             | 6    |             | 7    | ns   |
| t <sub>PU</sub>   | CE LOW to Power-Up                  | 0           |      | 0           |      | ns   |
| t <sub>PD</sub>   | CE HIGH to Power-Down               |             | 12   |             | 15   | ns   |
| t <sub>DBE</sub>  | Byte Enable to Data Valid           |             | 6    |             | 7    | ns   |
| t <sub>LZBE</sub> | Byte Enable to Low Z                | 0           |      | 0           |      | ns   |
| t <sub>HZBE</sub> | Byte Disable to High Z              |             | 6    |             | 7    | ns   |

**Notes:**

4. Tested initially and after any design or process changes that may affect these parameters.
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
6. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
7.  $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.

**Switching Characteristics<sup>[5]</sup> Over the Operating Range**

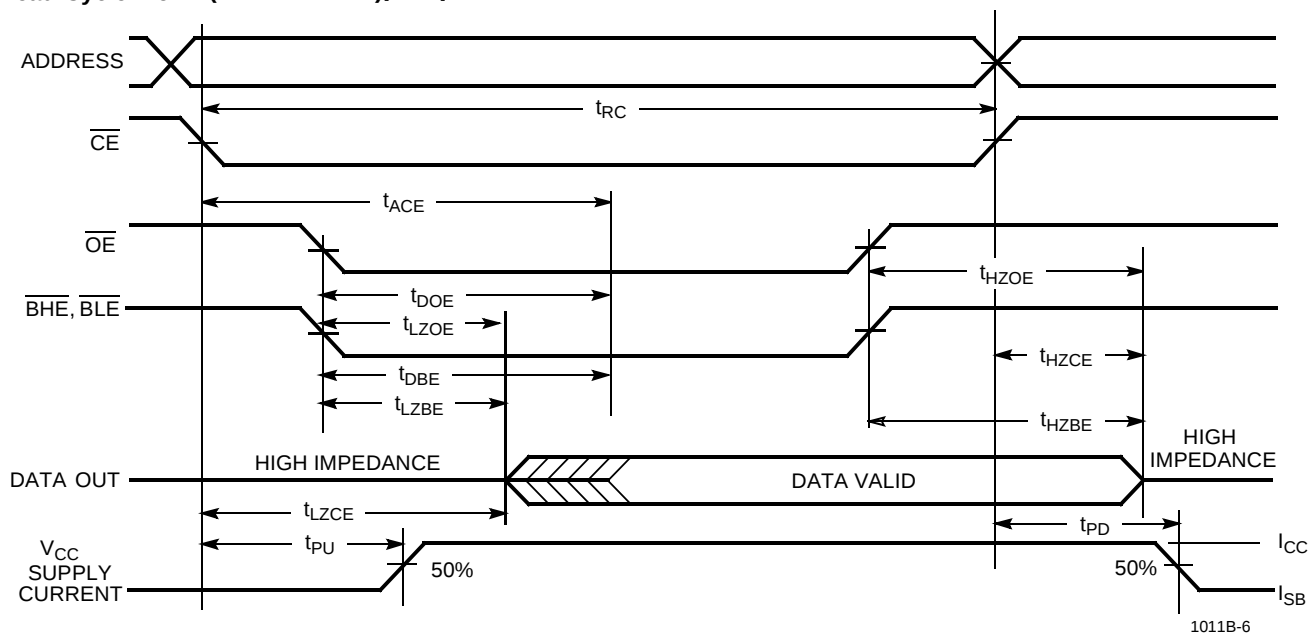
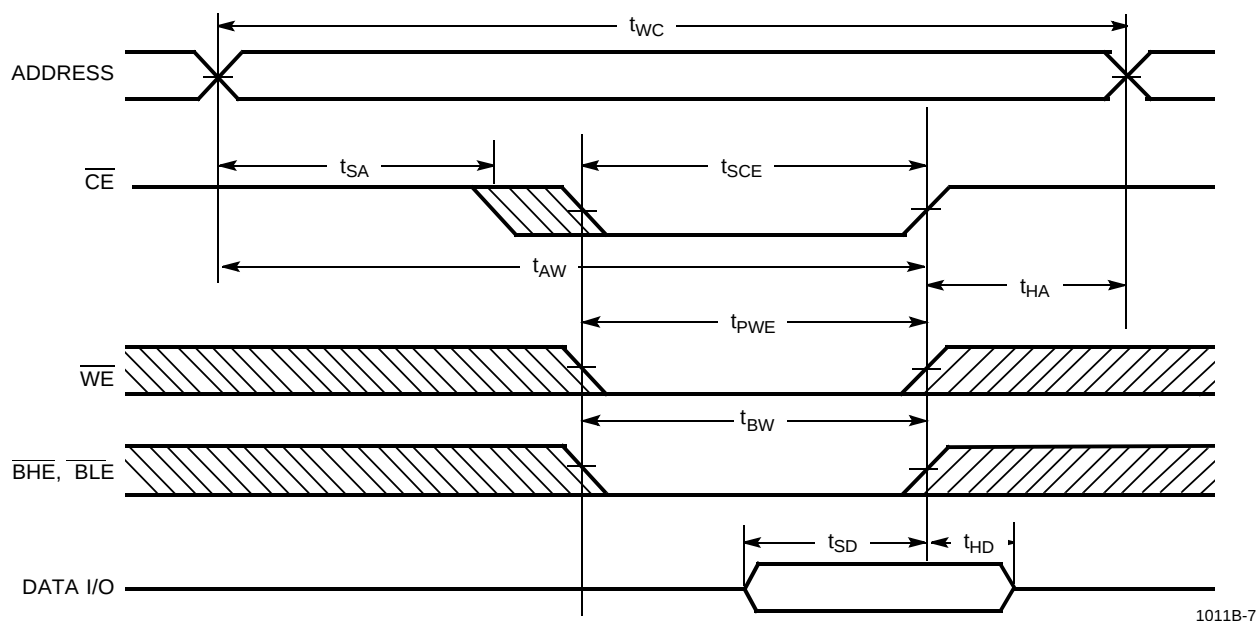
| Parameter                  | Description                        | 1011BV33-12 |      | 1011BV33-15 |      | Unit |
|----------------------------|------------------------------------|-------------|------|-------------|------|------|
|                            |                                    | Min.        | Max. | Min.        | Max. |      |
| WRITE CYCLE <sup>[8]</sup> |                                    |             |      |             |      |      |
| t <sub>WC</sub>            | Write Cycle Time                   | 12          |      | 15          |      | ns   |
| t <sub>SCE</sub>           | CE LOW to Write End                | 10          |      | 12          |      | ns   |
| t <sub>AW</sub>            | Address Set-Up to Write End        | 10          |      | 12          |      | ns   |
| t <sub>HA</sub>            | Address Hold from Write End        | 0           |      | 0           |      | ns   |
| t <sub>SA</sub>            | Address Set-Up to Write Start      | 0           |      | 0           |      | ns   |
| t <sub>PWE</sub>           | WE Pulse Width                     | 10          |      | 12          |      | ns   |
| t <sub>SD</sub>            | Data Set-Up to Write End           | 7           |      | 8           |      | ns   |
| t <sub>HD</sub>            | Data Hold from Write End           | 0           |      | 0           |      | ns   |
| t <sub>LZWE</sub>          | WE HIGH to Low Z <sup>[6]</sup>    | 3           |      | 3           |      | ns   |
| t <sub>HZWE</sub>          | WE LOW to High Z <sup>[6, 7]</sup> |             | 6    |             | 7    | ns   |
| t <sub>BW</sub>            | Byte Enable to End of Write        | 10          |      | 12          |      | ns   |

**Switching Waveforms**
**Read Cycle No. 1<sup>[9, 10]</sup>**


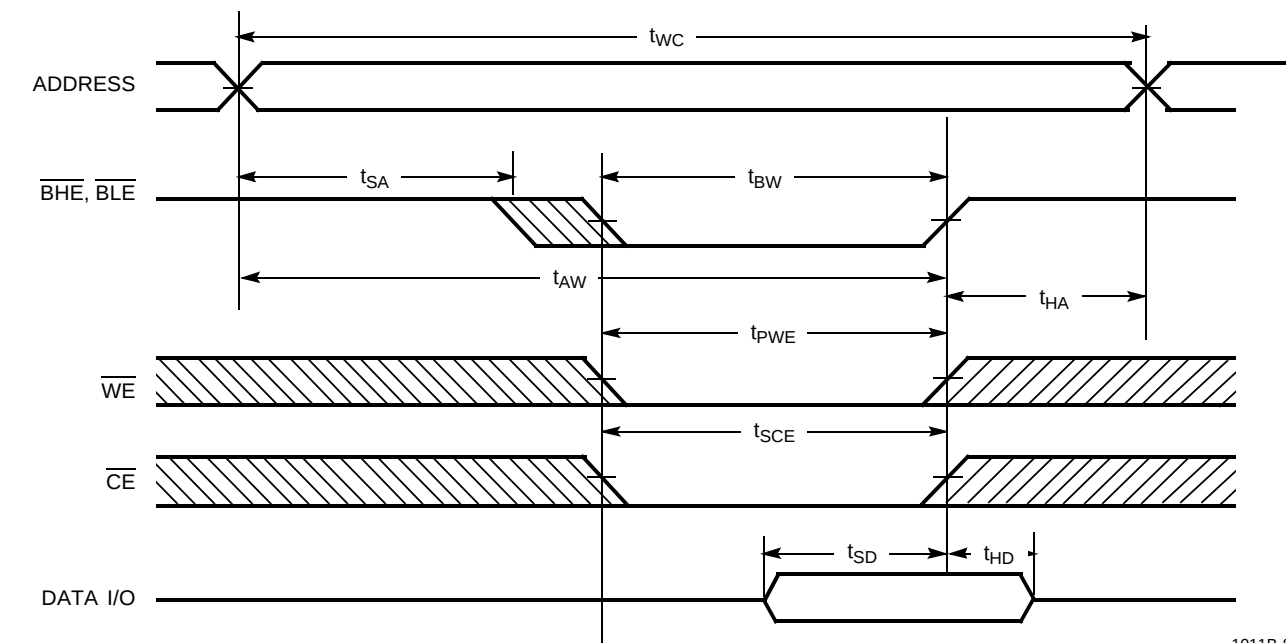
1011B-5

**Note:**

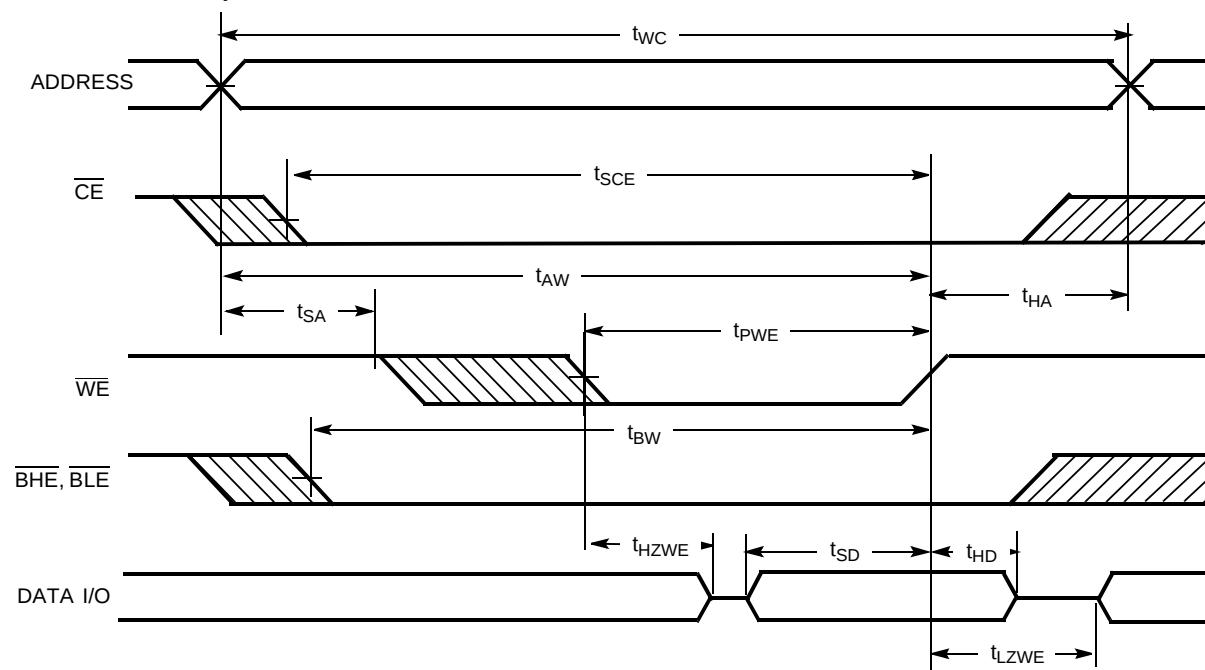
8. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}$  /  $\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}$  /  $\overline{BLE}$  must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. Device is continuously selected. OE, CE, BHE and/or BLE =  $V_{IL}$ .
10. WE is HIGH for read cycle.

**Switching Waveforms (continued)**
**Read Cycle No. 2 ( $\overline{OE}$  Controlled)[10, 11]**

**Write Cycle No. 1 ( $\overline{CE}$  Controlled) [12, 13]**

**Notes:**

11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
12. Data I/O is high impedance if  $\overline{OE}$  or BHE and/or BLE =  $V_{IH}$ .
13. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**


1011B-8

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)**


1011B-10

**Truth Table**

| CE | OE | WE | BLE | BHE | I/O <sub>1</sub> –I/O <sub>8</sub> | I/O <sub>9</sub> –I/O <sub>16</sub> | Mode                       | Power                      |
|----|----|----|-----|-----|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H  | X  | X  | X   | X   | High Z                             | High Z                              | Power-Down                 | Standby (I <sub>SB</sub> ) |
| L  | L  | H  | L   | L   | Data Out                           | Data Out                            | Read - All bits            | Active (I <sub>CC</sub> )  |
|    |    |    | L   | H   | Data Out                           | High Z                              | Read - Lower bits only     | Active (I <sub>CC</sub> )  |
|    |    |    | H   | L   | High Z                             | Data Out                            | Read - Upper bits only     | Active (I <sub>CC</sub> )  |
| L  | X  | L  | L   | L   | Data In                            | Data In                             | Write - All bits           | Active (I <sub>CC</sub> )  |
|    |    |    | L   | H   | Data In                            | High Z                              | Write - Lower bits only    | Active (I <sub>CC</sub> )  |
|    |    |    | H   | L   | High Z                             | Data In                             | Write - Upper bits only    | Active (I <sub>CC</sub> )  |
| L  | H  | H  | X   | X   | High Z                             | High Z                              | Selected, Outputs Disabled | Active (I <sub>CC</sub> )  |
| L  | X  | X  | H   | H   | High Z                             | High Z                              | Selected, Outputs Disabled | Active (I <sub>CC</sub> )  |

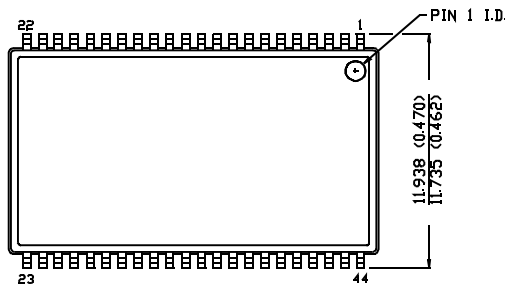
## Ordering Information

| Speed (ns) | Ordering Code     | Package Name | Package Type         | Operating Range |
|------------|-------------------|--------------|----------------------|-----------------|
| 12         | CY7C1011BV33-12ZI | Z44          | 44-Lead TSOP Type II | Industrial      |
|            | CY7C1011BV33-12ZC | Z44          | 44-Lead TSOP Type II | Commercial      |
| 15         | CY7C1011BV33-15ZC | Z44          | 44-Lead TSOP Type II | Commercial      |
|            | CY7C1011BV33-15ZI | Z44          | 44-Lead TSOP Type II | Industrial      |

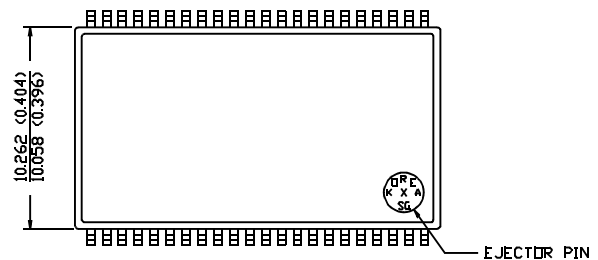
## Package Diagrams

### 44-Pin TSOP II Z44

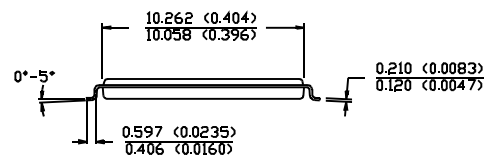
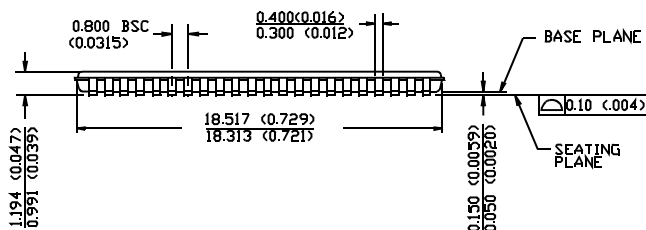
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A

| <b>Document Title: CY7C1011BV33 128K X 16 Static RAM</b><br><b>Document Number: 38-05021</b> |                |                   |                        |                                                                                                                    |
|----------------------------------------------------------------------------------------------|----------------|-------------------|------------------------|--------------------------------------------------------------------------------------------------------------------|
| <b>REV.</b>                                                                                  | <b>ECN NO.</b> | <b>Issue Date</b> | <b>Orig. of Change</b> | <b>Description of Change</b>                                                                                       |
| **                                                                                           | 106652         | 04/26/01          | MPR                    | New Data Sheet                                                                                                     |
| *A                                                                                           | 107728         | 07/11/01          | DFP                    | Remove SOJ TQFP Packages. Remove 8, 10 ns. changed Low Active Power to 684. Change words/array/ added 2 addresses. |