



**CY7C1019BV33**

**CY7C1018BV33**

## 128K x 8 Static RAM

### Features

- **High speed**  
—  $t_{AA} = 10 \text{ ns}$
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **Easy memory expansion with CE and OE options**
- **Functionally equivalent to CY7C1019V33 and/or CY7C1018V33**

### Functional Description

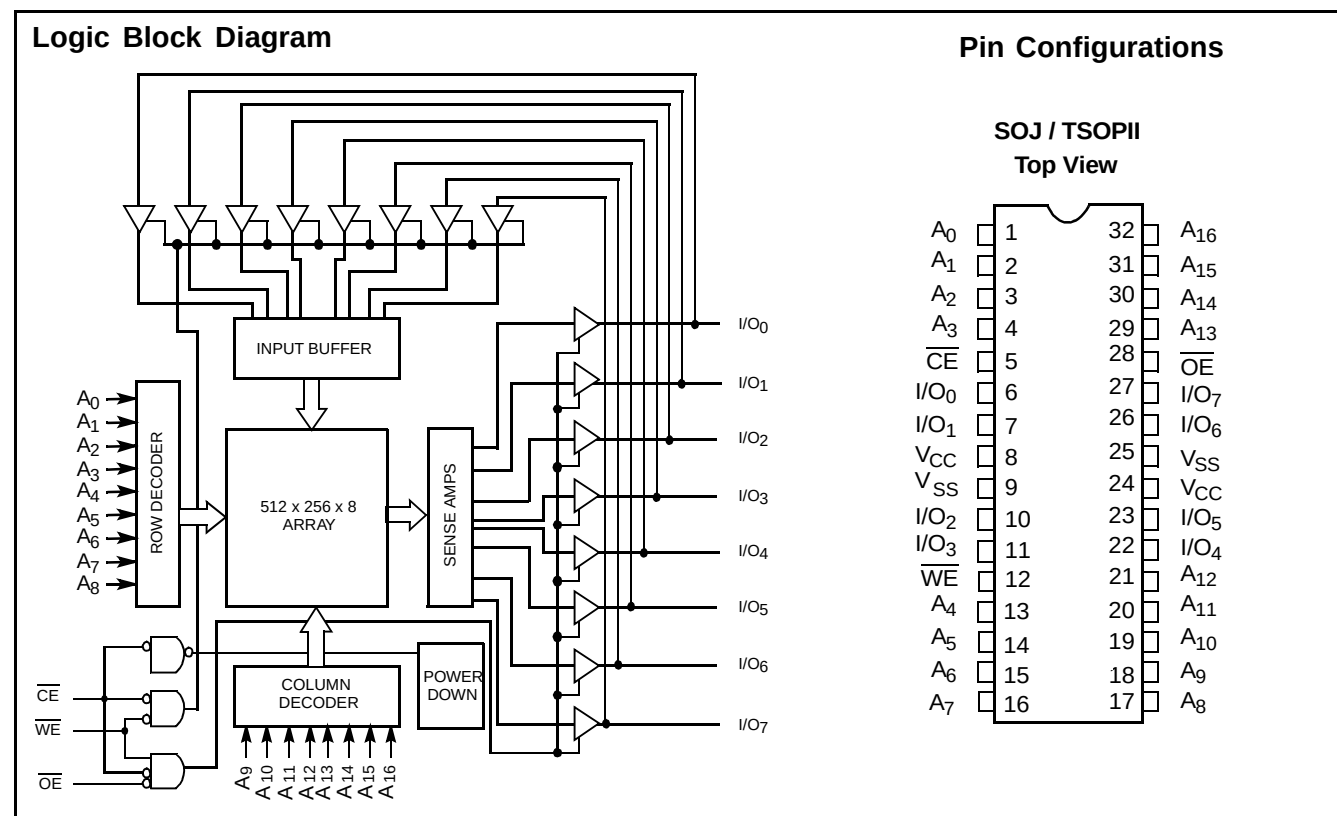
The CY7C1019BV33/CY7C1018BV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (CE), an active LOW Output Enable (OE), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1019BV33 is available in standard 32-pin TSOP Type II and 400-mil-wide package. The CY7C1018BV33 is available in a standard 300-mil-wide package.



### Selection Guide

|                                |   | 7C1019BV33-10<br>7C1018BV33-10 | 7C1019BV33-12<br>7C1018BV33-12 | 7C1019BV33-15<br>7C1018BV33-15 |
|--------------------------------|---|--------------------------------|--------------------------------|--------------------------------|
| Maximum Access Time (ns)       |   | 10                             | 12                             | 15                             |
| Maximum Operating Current (mA) |   | 175                            | 160                            | 145                            |
| Maximum Standby Current (mA)   |   | 5                              | 5                              | 5                              |
|                                | L | —                              | 0.5                            | 0.5                            |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs  
in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature <sup>[2]</sup> | $V_{CC}$   |
|------------|------------------------------------|------------|
| Commercial | 0°C to +70°C                       | 3.3V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description                                   | Test Conditions                                                                                                       | 7C1019BV33-10<br>7C1018BV33-10 |                | 7C1019BV33-12<br>7C1018BV33-12 |                | 7C1019BV33-15<br>7C1018BV33-15 |                | Unit |
|-----------|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|--------------------------------|----------------|--------------------------------|----------------|--------------------------------|----------------|------|
|           |                                               |                                                                                                                       | Min.                           | Max.           | Min.                           | Max.           | Min.                           | Max.           |      |
| $V_{OH}$  | Output HIGH Voltage                           | $V_{CC} = \text{Min.},$<br>$I_{OH} = -4.0 \text{ mA}$                                                                 | 2.4                            |                | 2.4                            |                | 2.4                            |                | V    |
| $V_{OL}$  | Output LOW Voltage                            | $V_{CC} = \text{Min.},$<br>$I_{OL} = 8.0 \text{ mA}$                                                                  |                                | 0.4            |                                | 0.4            |                                | 0.4            | V    |
| $V_{IH}$  | Input HIGH Voltage                            |                                                                                                                       | 2.2                            | $V_{CC} + 0.3$ | 2.2                            | $V_{CC} + 0.3$ | 2.2                            | $V_{CC} + 0.3$ | V    |
| $V_{IL}$  | Input LOW Voltage <sup>[1]</sup>              |                                                                                                                       | -0.3                           | 0.8            | -0.3                           | 0.8            | -0.3                           | 0.8            | V    |
| $I_{IX}$  | Input Load Current                            | $GND \leq V_I \leq V_{CC}$                                                                                            | -1                             | +1             | -1                             | +1             | -1                             | +1             | μA   |
| $I_{OZ}$  | Output Leakage Current                        | $GND \leq V_I \leq V_{CC},$<br>Output Disabled                                                                        | -5                             | +5             | -5                             | +5             | -5                             | +5             | μA   |
| $I_{CC}$  | $V_{CC}$ Operating Supply Current             | $V_{CC} = \text{Max.},$<br>$I_{OUT} = 0 \text{ mA},$<br>$f = f_{MAX} = 1/t_{RC}$                                      |                                | 175            |                                | 160            |                                | 145            | mA   |
| $I_{SB1}$ | Automatic CE Power-Down Current — TTL Inputs  | Max. $V_{CC}, \overline{CE} \geq V_{IH}$<br>$V_{IN} \geq V_{IH}$ or<br>$V_{IN} \leq V_{IL}, f = f_{MAX}$              |                                | 20             |                                | 20             |                                | 20             | mA   |
| $I_{SB2}$ | Automatic CE Power-Down Current — CMOS Inputs | Max. $V_{CC},$<br>$\overline{CE} \geq V_{CC} - 0.3V,$<br>$V_{IN} \geq V_{CC} - 0.3V,$<br>or $V_{IN} \leq 0.3V, f = 0$ |                                | 5              |                                | 5              |                                | 5              | mA   |
|           |                                               | L                                                                                                                     |                                | —              |                                | 0.5            |                                | 0.5            |      |

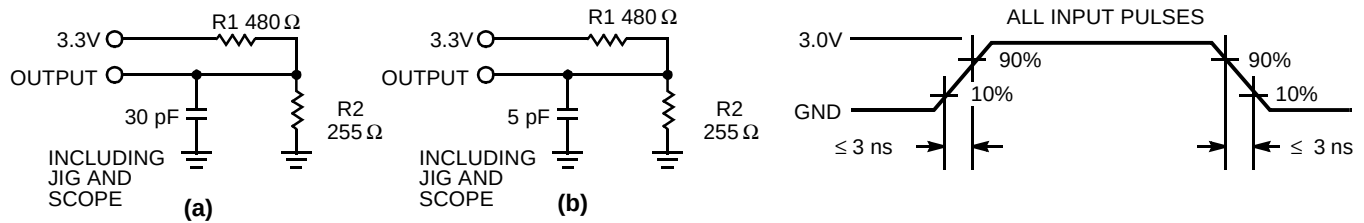
## Capacitance<sup>[3]</sup>

| Parameter | Description        | Test Conditions                                                 | Max. | Unit |
|-----------|--------------------|-----------------------------------------------------------------|------|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$<br>$V_{CC} = 5.0V$ | 6    | pF   |
| $C_{OUT}$ | Output Capacitance |                                                                 | 8    | pF   |

### Notes:

- $V_{IL}(\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- $T_A$  is the "Instant On" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT  
 OUTPUT — 167 Ω — 1.73V

## Switching Characteristics<sup>[4]</sup> Over the Operating Range

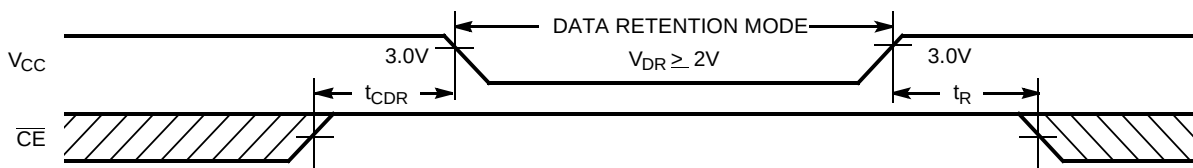
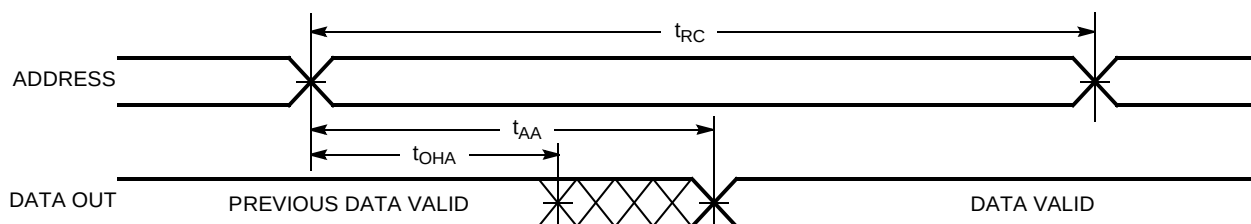
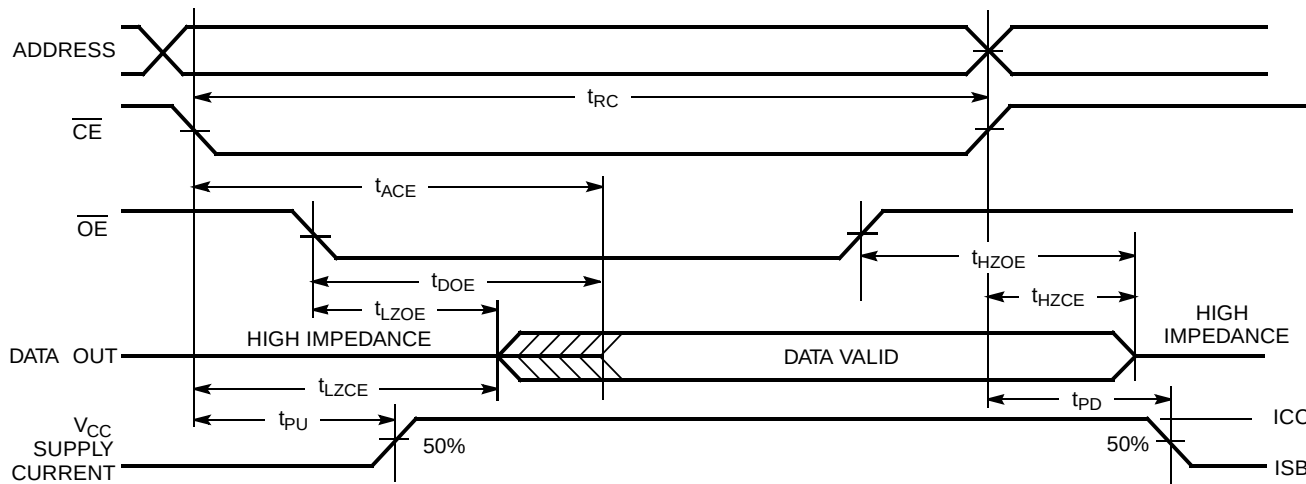
| Parameter                     | Description                                      | 7C1019BV33-10<br>7C1018BV33-10 |      | 7C1019BV33-12<br>7C1018BV33-12 |      | 7C1019BV33-15<br>7C1018BV33-15 |      | Unit |
|-------------------------------|--------------------------------------------------|--------------------------------|------|--------------------------------|------|--------------------------------|------|------|
|                               |                                                  | Min.                           | Max. | Min.                           | Max. | Min.                           | Max. |      |
| READ CYCLE                    |                                                  |                                |      |                                |      |                                |      |      |
| t <sub>RC</sub>               | Read Cycle Time                                  | 10                             |      | 12                             |      | 15                             |      | ns   |
| t <sub>AA</sub>               | Address to Data Valid                            |                                | 10   |                                | 12   |                                | 15   | ns   |
| t <sub>OHA</sub>              | Data Hold from Address Change                    | 3                              |      | 3                              |      | 3                              |      | ns   |
| t <sub>ACE</sub>              | $\overline{CE}$ LOW to Data Valid                |                                | 10   |                                | 12   |                                | 15   | ns   |
| t <sub>DOE</sub>              | $\overline{OE}$ LOW to Data Valid                |                                | 5    |                                | 6    |                                | 7    | ns   |
| t <sub>LZOE</sub>             | $\overline{OE}$ LOW to Low Z                     | 0                              |      | 0                              |      | 0                              |      | ns   |
| t <sub>HZOE</sub>             | $\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup> |                                | 5    |                                | 6    |                                | 7    | ns   |
| t <sub>LZCE</sub>             | $\overline{CE}$ LOW to Low Z <sup>[6]</sup>      | 3                              |      | 3                              |      | 3                              |      | ns   |
| t <sub>HZCE</sub>             | $\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup> |                                | 5    |                                | 6    |                                | 7    | ns   |
| t <sub>PU</sub>               | $\overline{CE}$ LOW to Power-Up                  | 0                              |      | 0                              |      | 0                              |      | ns   |
| t <sub>PD</sub>               | $\overline{CE}$ HIGH to Power-Down               |                                | 10   |                                | 12   |                                | 15   | ns   |
| WRITE CYCLE <sup>[7, 8]</sup> |                                                  |                                |      |                                |      |                                |      |      |
| t <sub>WC</sub>               | Write Cycle Time                                 | 10                             |      | 12                             |      | 15                             |      | ns   |
| t <sub>SCE</sub>              | $\overline{CE}$ LOW to Write End                 | 8                              |      | 9                              |      | 10                             |      | ns   |
| t <sub>AW</sub>               | Address Set-Up to Write End                      | 7                              |      | 8                              |      | 10                             |      | ns   |
| t <sub>HA</sub>               | Address Hold from Write End                      | 0                              |      | 0                              |      | 0                              |      | ns   |
| t <sub>SA</sub>               | Address Set-Up to Write Start                    | 0                              |      | 0                              |      | 0                              |      | ns   |
| t <sub>PWE</sub>              | $\overline{WE}$ Pulse Width                      | 7                              |      | 8                              |      | 10                             |      | ns   |
| t <sub>SD</sub>               | Data Set-Up to Write End                         | 5                              |      | 6                              |      | 8                              |      | ns   |
| t <sub>HD</sub>               | Data Hold from Write End                         | 0                              |      | 0                              |      | 0                              |      | ns   |
| t <sub>LZWE</sub>             | $\overline{WE}$ HIGH to Low Z <sup>[6]</sup>     | 3                              |      | 3                              |      | 3                              |      | ns   |
| t <sub>HZWE</sub>             | $\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>  |                                | 5    |                                | 6    |                                | 7    | ns   |

### Notes:

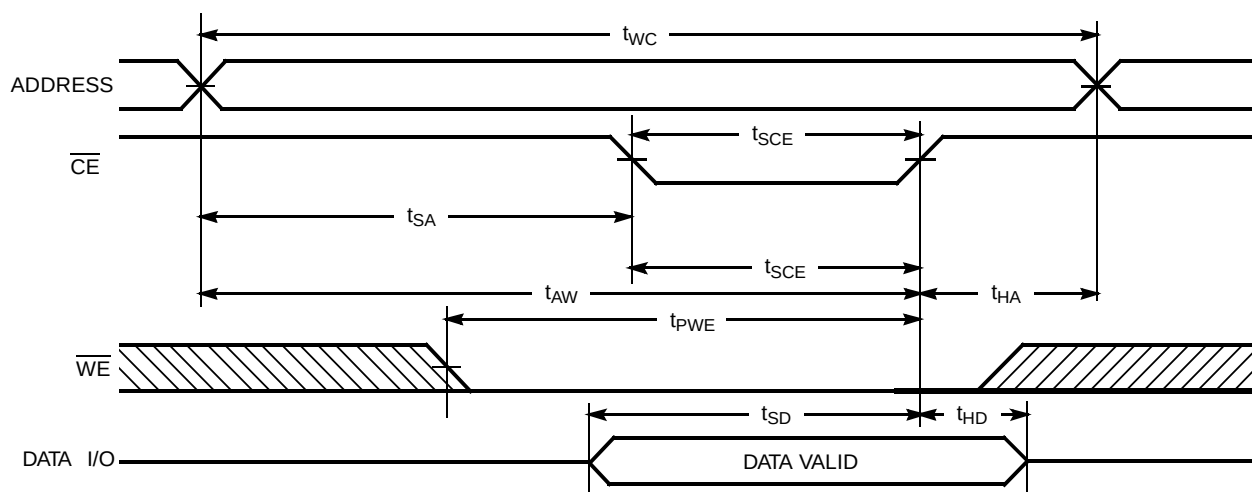
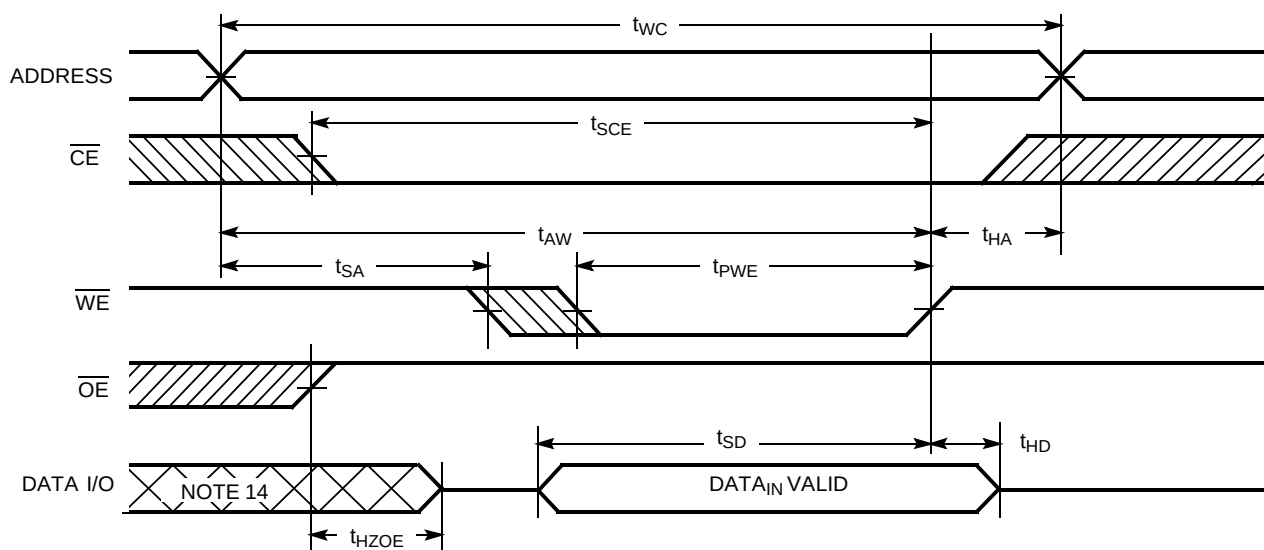
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Data Retention Characteristics** Over the Operating Range (L Version Only)

| Parameter       | Description                          | Conditions                                              | Min. | Max. | Unit    |
|-----------------|--------------------------------------|---------------------------------------------------------|------|------|---------|
| $V_{DR}$        | $V_{CC}$ for Data Retention          | No input may exceed $V_{CC} + 0.5V$                     | 2.0  |      | V       |
| $I_{CCDR}$      | Data Retention Current               | $V_{CC} = V_{DR} = 2.0V$ ,<br>$CE \geq V_{CC} - 0.3V$ , |      | 150  | $\mu A$ |
| $t_{CDR}^{[3]}$ | Chip Deselect to Data Retention Time | $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$       | 0    |      | ns      |
| $t_R$           | Operation Recovery Time              |                                                         | 200  |      | $\mu s$ |

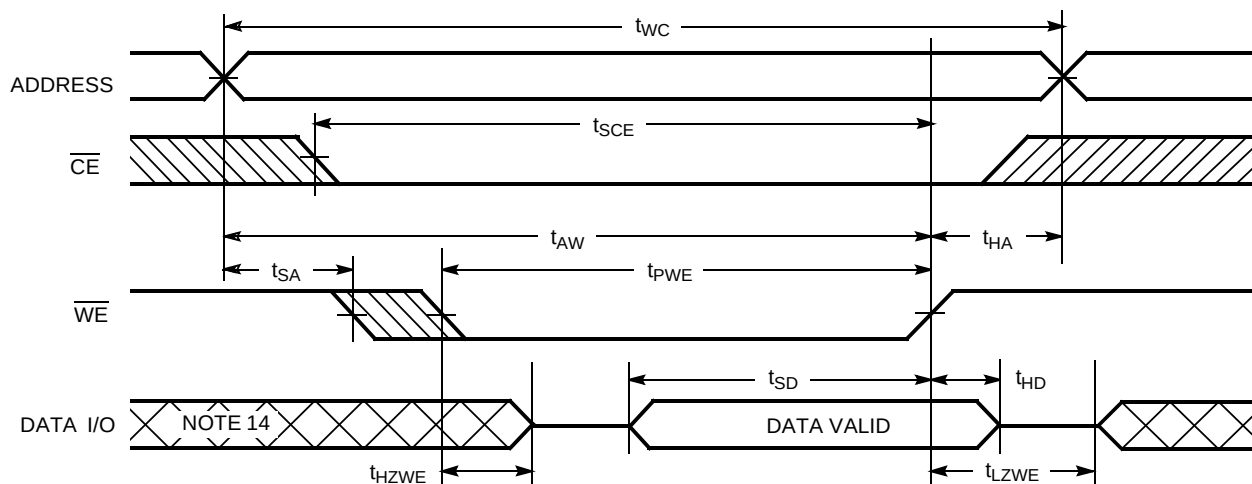
**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1<sup>[9, 10]</sup>**

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[10, 11]</sup>**

**Notes:**

9. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
10.  $\overline{WE}$  is HIGH for read cycle.
11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[12, 13]</sup>**

**Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  HIGH During Write)<sup>[12, 13]</sup>**

**Notes:**

12. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
13. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.
14. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[13]</sup>**

**Truth Table**

| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | I/O <sub>0</sub> -I/O <sub>7</sub> | Mode                       | Power                       |
|------------------------|------------------------|------------------------|------------------------------------|----------------------------|-----------------------------|
| H                      | X                      | X                      | High Z                             | Power-Down                 | Standby ( $I_{\text{SB}}$ ) |
| X                      | X                      | X                      | High Z                             | Power-Down                 | Standby ( $I_{\text{SB}}$ ) |
| L                      | L                      | H                      | Data Out                           | Read                       | Active ( $I_{\text{CC}}$ )  |
| L                      | X                      | L                      | Data In                            | Write                      | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | H                      | High Z                             | Selected, Outputs Disabled | Active ( $I_{\text{CC}}$ )  |

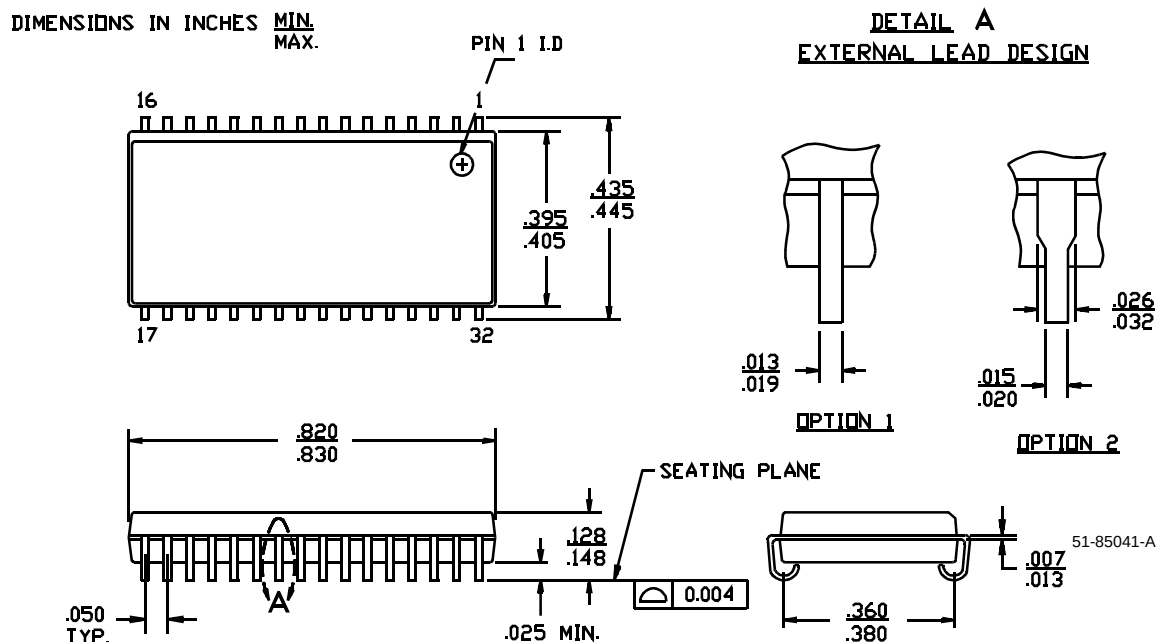
**Ordering Information**

| Speed (ns) | Ordering Code      | Package Name | Package Type               | Operating Range |
|------------|--------------------|--------------|----------------------------|-----------------|
| 10         | CY7C1018V33-10VC   | V32          | 32-Lead 300-Mil Molded SOJ | Commercial      |
|            | CY7C1019BV33-10VC  | V33          | 32-Lead 400-Mil Molded SOJ |                 |
|            | CY7C1019BV33-10ZC  | ZS32         | 32-Lead TSOP Type II       |                 |
| 12         | CY7C1018BV33-12VC  | V32          | 32-Lead 300-Mil Molded SOJ |                 |
|            | CY7C1018BV33L-12VC | V32          | 32-Lead 300-Mil Molded SOJ |                 |
|            | CY7C1019BV33-12VC  | V33          | 32-Lead 400-Mil Molded SOJ |                 |
|            | CY7C1019BV33-12ZC  | ZS32         | 32-Lead TSOP Type II       |                 |
|            | CY7C1019BV33L-12VC | V33          | 32-Lead 400-Mil Molded SOJ |                 |
|            | CY7C1019BV33L-12ZC | ZS32         | 32-Lead TSOP Type II       |                 |
| 15         | CY7C1018BV33-15VC  | V32          | 32-Lead 300-Mil Molded SOJ |                 |
|            | CY7C1018BV33L-15VC | V32          | 32-Lead 300-Mil Molded SOJ |                 |
|            | CY7C1018BV33-15VI  | V32          | 32-Lead 300-Mil Molded SOJ |                 |
|            | CY7C1019BV33-15VC  | V33          | 32-Lead 400-Mil Molded SOJ |                 |
|            | CY7C1019BV33-15ZC  | ZS32         | 32-Lead TSOP Type II       |                 |
|            | CY7C1019BV33L-15VC | V33          | 32-Lead 400-Mil Molded SOJ |                 |
|            | CY7C1019BV33L-15ZC | ZS32         | 32-Lead TSOP Type II       |                 |
|            | CY7C1019BV33-15VI  | V33          | 32-Lead 400-Mil Molded SOJ |                 |
|            | CY7C1019BV33-15ZI  | ZS32         | 32-Lead TSOP Type II       | Industrial      |

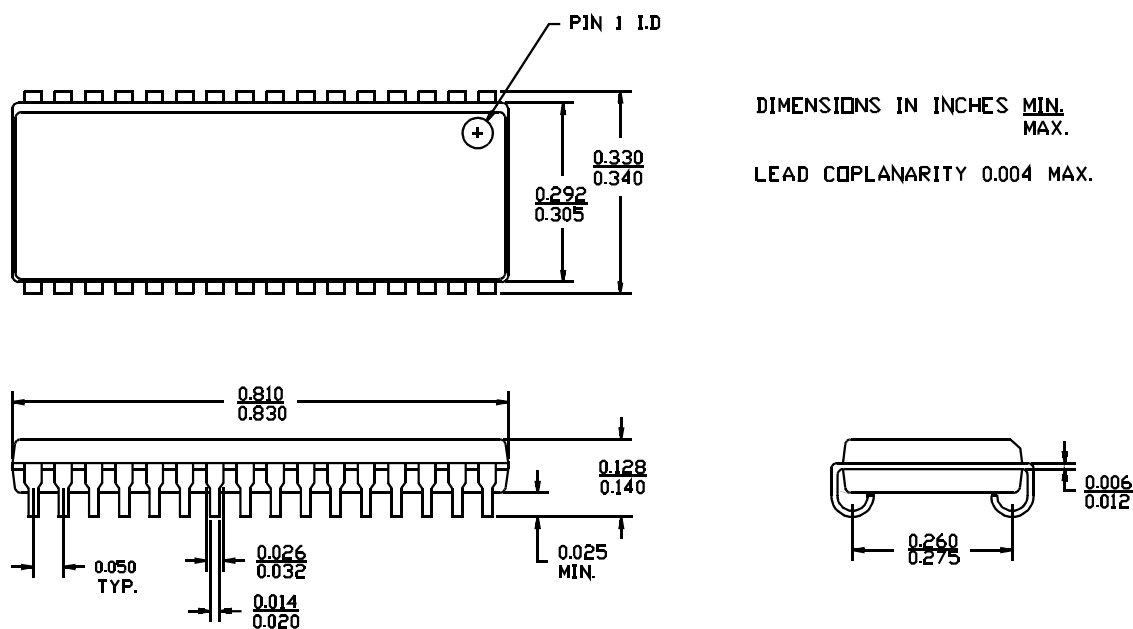
Document #: 38-01053-\*B

# Package Diagram

## 32-Lead (400-Mil) Molded SOJ V33



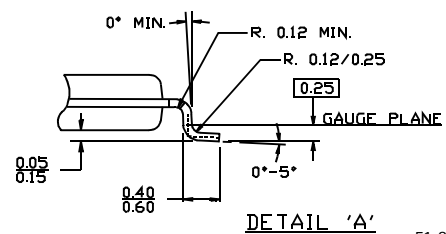
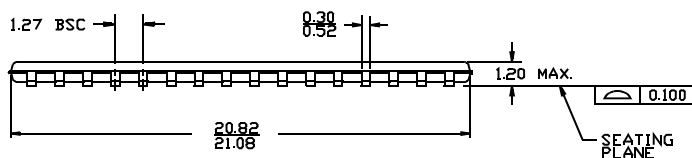
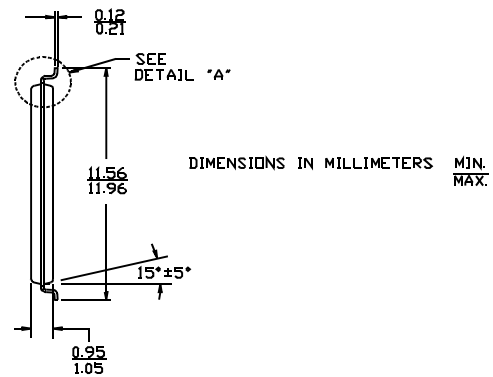
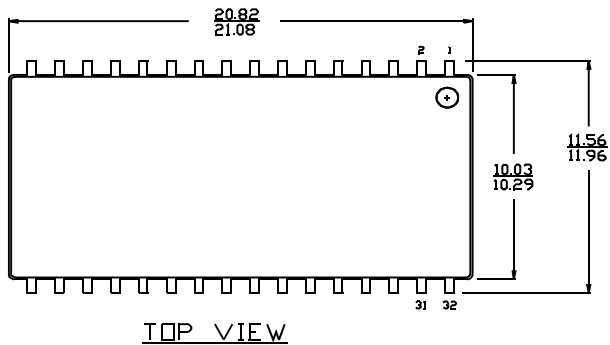
## 32-Lead (300-Mil) Molded SOJ V32





Package Diagram

32-Lead TSOP II ZS32



51-85095