

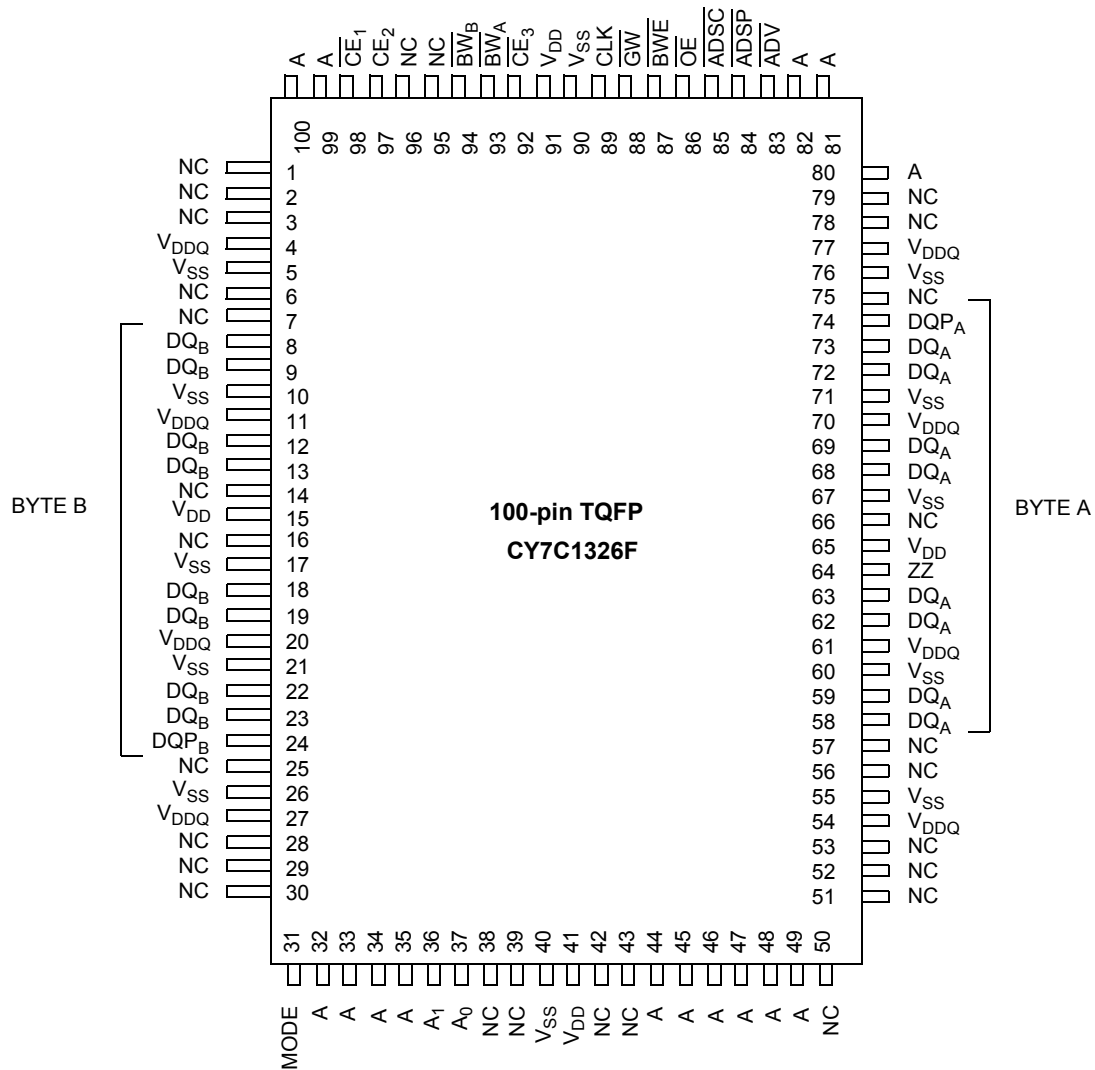


2-Mb (128K x 18) Pipelined Sync SRAM

Selection Guide

	133 MHz	100 MHz	Unit
Maximum Access Time	4.0	4.5	ns
Maximum Operating Current	225	205	mA
Maximum CMOS Standby Current	40	40	mA

Pin Configuration



Pin Definitions

Name	TQFP	I/O	Description
A ₀ , A ₁ , A	37,36, 32,33,34, 35,44,45, 46,47,48, 49,80,81, 82,99, 100	Input- Synchronous	Address Inputs used to select one of the 128K address locations. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE ₁ , CE ₂ , and CE ₃ are sampled active. A _[1:0] feed the 2-bit counter.
BW _A , BW _B	93,94	Input- Synchronous	Byte Write Select Inputs, active LOW. Qualified with BWE to conduct Byte Writes to the SRAM. Sampled on the rising edge of CLK.
GW	88	Input- Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global Write is conducted (ALL bytes are written, regardless of the values on BW _[A:B] and BWE).
BWE	87	Input- Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a Byte Write.
CLK	89	Input- Clock	Clock Input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
CE ₁	98	Input- Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE ₂ and CE ₃ to select/deselect the device. ADSP is ignored if CE ₁ is HIGH.
CE ₂	97	Input- Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with CE ₁ and CE ₃ to select/deselect the device.
CE ₃	92	Input- Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE ₁ and CE ₂ to select/deselect the device. Not connected for BGA. Where referenced, CE ₃ is assumed active throughout this document for BGA.
OE	86	Input- Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. OE is masked during the first clock of a Read cycle when emerging from a deselected state.
ADV	83	Input- Synchronous	Advance Input signal, sampled on the rising edge of CLK, active LOW. When asserted, it automatically increments the address in a burst cycle.
ADSP	84	Input- Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK, active LOW. When asserted LOW, A is captured in the address registers. A _[1:0] are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when CE ₁ is deasserted HIGH.
ADSC	85	Input- Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK, active LOW. When asserted LOW, A is captured in the address registers. A _[1:0] are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ	64	Input- Asynchronous	ZZ "Sleep" Input, active HIGH. This input, when HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQ _A , DQ _B DQP _A , DQP _B	58,59,62, 63,68,69, 72,73 8,9,12,13, 18,19,22, 23 74,24	I/O- Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by "A" during the previous clock rise of the Read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP _[A:B] are placed in a three-state condition.
V _{DD}	15,41,65, 91	Power Supply	Power supply inputs to the core of the device.

Pin Definitions (continued)

Name	TQFP	I/O	Description
V _{SS}	5,10,17, 21,26,40, 55,60,67, 71,76,90	Ground	Ground for the device.
V _{DDQ}	4,11,20, 27,54,61, 70,77	I/O Ground	Ground for the I/O circuitry.
MODE	31	Input- Static	Selects Burst Order. When tied to GND selects linear burst sequence. When tied to V _{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up.
NC	1,2,3,6,7, 14,16,25, 28,29,30, 38,39,42, 43,50,51, 52,53,56, 57,66,75, 78,79,95, 96		No Connects. Not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1326F supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BW_[A:B]) inputs. A Global Write Enable (GW) overrides all Byte Write inputs and writes data to all four bytes. All Writes are simplified with on-chip synchronous self-timed Write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. ADSP is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) $\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ are all asserted active, and (3) the Write signals (GW, BWE) are all deserted HIGH. ADSP is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the Address Register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the

Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within t_{CO} if OE is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single Read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output will three-state immediately.

Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) $\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The Write signals (GW, BWE, and BW_[A:B]) and ADV inputs are ignored during this first cycle.

ADSP-triggered Write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQ inputs is written into the corresponding address location in the memory array. If GW is HIGH, then the Write operation is controlled by BWE and BW_[A:B] signals. The CY7C1326F provides Byte Write capability that is described in the Write Cycle Descriptions table. Asserting the Byte Write Enable input (BWE) with the selected Byte Write (BW_[A:B]) input, will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1326F is a common I/O device, the Output Enable ($\overline{OE}$) must be deserted HIGH before presenting data to the DQ inputs. Doing so will three-state the output drivers. As a safety precaution, DQs are automatically three-stated whenever a Write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by ADSC

ADSC Write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) CE₁, CE₂, CE₃ are all asserted active, and (4) the appropriate combination of the Write inputs (GW, BWE, and BW_[A,B]) are asserted active to conduct a Write to the desired byte(s). ADSC-triggered Write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The ADV input is ignored during this cycle. If a global Write is conducted, the data presented to DQ is written into the corresponding address location in the memory core. If a Byte Write is conducted, only the selected bytes are written. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1326F is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQ inputs. Doing so will three-state the output drivers. As a safety precaution, DQs are automatically three-stated whenever a Write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1326F provides a two-bit wraparound counter, fed by A_[1:0], that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting ADV LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I _{DDZZ}	Snooze mode standby current	ZZ ≥ V _{DD} – 0.2V		40	mA
t _{ZZS}	Device operation to ZZ	ZZ ≥ V _{DD} – 0.2V		2t _{CYC}	ns
t _{ZZREC}	ZZ recovery time	ZZ ≤ 0.2V	2t _{CYC}		ns
t _{ZZI}	ZZ Active to snooze current	This parameter is sampled		2t _{CYC}	ns
t _{RZZI}	ZZ Inactive to exit snooze current	This parameter is sampled	0		ns

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A _[1:0]	Second Address A _[1:0]	Third Address A _[1:0]	Fourth Address A _[1:0]
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A _[1:0]	Second Address A _[1:0]	Third Address A _[1:0]	Fourth Address A _[1:0]
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CE₁, CE₂, CE₃, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Truth Table^[2, 3, 4, 5, 6, 7]

Next Cycle	Add. Used	ZZ	$\overline{CE}_3$	$\overline{CE}_2$	$\overline{CE}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DQ	Write
Unselected	None	L	X	X	H	X	L	X	X	Three-State	X
Unselected	None	L	H	X	L	L	X	X	X	Three-State	X
Unselected	None	L	X	L	L	L	X	X	X	Three-State	X
Unselected	None	L	H	X	L	H	L	X	X	Three-State	X
Unselected	None	L	X	L	L	H	L	X	X	Three-State	X
Begin Read	External	L	L	H	L	L	X	X	X	Three-State	X
Begin Read	External	L	L	H	L	H	L	X	X	Three-State	Read
Continue Read	Next	L	X	X	X	H	H	L	H	Three-State	Read
Continue Read	Next	L	X	X	X	H	H	L	L	DQ	Read
Continue Read	Next	L	X	X	H	X	H	L	H	Three-State	Read
Continue Read	Next	L	X	X	H	X	H	L	L	DQ	Read
Suspend Read	Current	L	X	X	X	H	H	H	H	Three-State	Read
Suspend Read	Current	L	X	X	X	H	H	H	L	DQ	Read
Suspend Read	Current	L	X	X	H	X	H	H	H	Three-State	Read
Suspend Read	Current	L	X	X	H	X	H	H	L	DQ	Read
Begin Write	Current	L	X	X	X	H	H	H	X	Three-State	Write
Begin Write	Current	L	X	X	H	X	H	H	X	Three-State	Write
Begin Write	External	L	L	H	L	H	H	X	X	Three-State	Write
Continue Write	Next	L	X	X	X	H	H	H	X	Three-State	Write
Continue Write	Next	L	X	X	H	X	H	H	X	Three-State	Write
Suspend Write	Current	L	X	X	X	H	H	H	X	Three-State	Write
Suspend Write	Current	L	X	X	H	X	H	H	X	Three-State	Write
ZZ "Sleep"	None	H	X	X	X	X	X	X	X	Three-State	X

Truth Table for Read/Write^[2, 3]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X
Read	H	L	H	H
Write Byte A – (DQ _A and DQP _A)	H	L	H	L
Write Byte B – (DQ _B and DQP _B)	H	L	L	H
Write Bytes B, A	H	L	L	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

Notes:

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.
- $\overline{WRITE} = L$ when any one or more Byte Write Enable signals ($\overline{BW}_A$, $\overline{BW}_B$) and $\overline{BWE} = L$ or $\overline{GW} = L$. $\overline{WRITE} = H$ when all Byte Write Enable signals ($\overline{BW}_A$, $\overline{BW}_B$), $\overline{BWE}$, $\overline{GW} = H$.
- The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
- $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ are available only in the TQFP package. BGA package has only 2 chip selects $\overline{CE}_1$ and $\overline{CE}_2$.
- The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_{[A:B]}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the Write cycle to allow the outputs to Three-State. $\overline{OE}$ is a don't care for the remainder of the Write cycle.
- $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during Write cycles. During a Read cycle all data bits are Three-State when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage on V_{DD} Relative to GND -0.5V to +4.6V

DC Voltage Applied to Outputs
in Three-State -0.5V to $V_{DDQ} + 0.5V$

DC Input Voltage -0.5V to $V_{DD} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V -5%/+10%	3.3V -5% to V_{DD}

Electrical Characteristics Over the Operating Range^[8, 9]

Parameter	Description	Test Conditions	Min.	Max.	Unit	
V _{DD}	Power Supply Voltage		3.135	3.6	V	
V _{DDQ}	I/O Supply Voltage		3.135	V _{DD}	V	
V _{OH}	Output HIGH Voltage	V _{DDQ} = 3.3V, V _{DD} = Min., I _{OH} = −4.0 mA	2.4		V	
V _{OL}	Output LOW Voltage	V _{DDQ} = 3.3V, V _{DD} = Min., I _{OL} = 8.0 mA		0.4	V	
V _{IH}	Input HIGH Voltage ^[8]	V _{DDQ} = 3.3V	2.0	V _{DD} + 0.3V	V	
V _{IL}	Input LOW Voltage ^[8]	V _{DDQ} = 3.3V	−0.3	0.8	V	
I _X	Input Load Current except ZZ and MODE	GND ≤ V _I ≤ V _{DDQ}	−5	5	μA	
	Input Current of MODE	Input = V _{SS}	−30		μA	
		Input = V _{DD}		5	μA	
	Input Current of ZZ	Input = V _{SS}	−5		μA	
		Input = V _{DD}		30	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{DDQ} , Output Disabled	−5	5	μA	
I _{DD}	V _{DD} Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{CYC}	7.5-ns cycle, 133 MHz		225	mA
			10-ns cycle, 100 MHz		205	mA
I _{SB1}	Automatic CS Power-down Current—TTL Inputs	V _{DD} = Max, Device Deselected, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} = 1/t _{CYC}	7.5-ns cycle, 133 MHz		90	mA
			10-ns cycle, 100 MHz		80	mA
I _{SB2}	Automatic CS Power-down Current—CMOS Inputs	V _{DD} = Max, Device Deselected, V _{IN} ≤ 0.3V or V _{IN} ≥ V _{DDQ} − 0.3V, f = 0	All speeds		40	mA
I _{SB3}	Automatic CS Power-down Current—CMOS Inputs	V _{DD} = Max, Device Deselected, or V _{IN} ≤ 0.3V or V _{IN} ≥ V _{DDQ} − 0.3V, f = f _{MAX} = 1/t _{CYC}	7.5-ns cycle, 133 MHz		75	mA
			10-ns cycle, 100 MHz		65	mA
I _{SB4}	Automatic CS Power-down Current—TTL Inputs	V _{DD} = Max, Device Deselected, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = 0	All speeds		45	mA

Notes:

8. Overshoot: $V_{IH}(AC) < V_{DD} + 1.5V$ (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2V$ (Pulse width less than $t_{CYC}/2$).

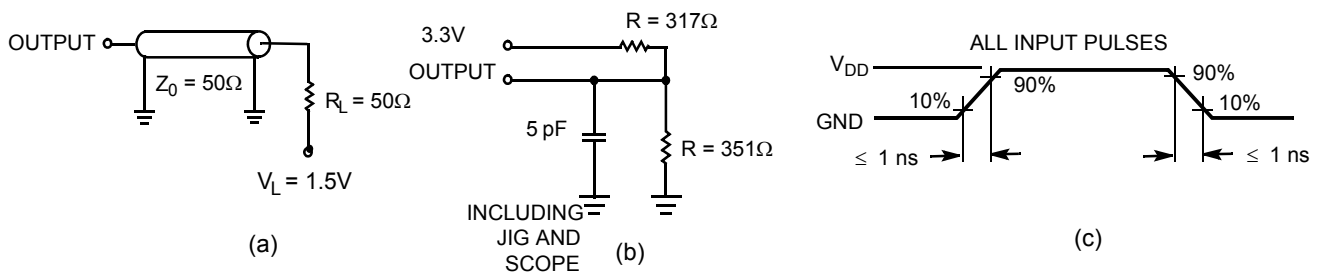
9. $T_{Power-up}$: Assumes a linear ramp from 0V to $V_{DD}(\text{min.})$ within 200 ms. During this time $V_{IH} \leq V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

Thermal Resistance^[10]

Parameter	Description	Test Conditions	TQFP Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	41.83	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		9.99	°C/W

Capacitance^[10]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 3.3\text{V}$, $V_{DDQ} = 3.3\text{V}$	5	pF
C_{CLK}	Clock Input Capacitance		5	pF
$C_{I/O}$	Input/Output Capacitance		5	pF

AC Test Loads and Waveforms
3.3V I/O Test Load

Note:

10. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics Over the Operating Range^[11, 12]

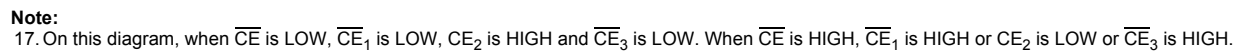
Parameter	Description	133 MHz		100 MHz		Unit
		Min.	Max	Min.	Max	
t _{POWER}	V _{DD} (Typical) to the First Access ^[13]	1		1	1	ms
Clock						
t _{CYC}	Clock Cycle Time	7.5		10		ns
t _{CH}	Clock HIGH	3.0		3.5		ns
t _{CL}	Clock LOW	3.0		3.5		ns
Output Times						
t _{CO}	Data Output Valid after CLK Rise		4.0		4.5	ns
t _{DOH}	Data Output Hold after CLK Rise	2.0		2.0		ns
t _{CLZ}	Clock to Low-Z ^[14, 15, 16]	0		0		ns
t _{CHZ}	Clock to High-Z ^[14, 15, 16]		4.0		4.5	ns
t _{OEV}	$\overline{OE}$ LOW to Output Valid		4.5		4.5	ns
t _{OELZ}	$\overline{OE}$ LOW to Output Low-Z ^[14, 15, 16]	0		0		ns
t _{OEHZ}	$\overline{OE}$ HIGH to Output High-Z ^[14, 15, 16]		4.0		4.5	ns
Set-up Times						
t _{AS}	Address Set-up before CLK Rise	1.5		1.5		ns
t _{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ Set-up before CLK Rise	1.5		1.5		ns
t _{ADVS}	$\overline{ADV}$ Set-up before CLK Rise	1.5		1.5		ns
t _{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:B]}$ Set-up before CLK Rise	1.5		1.5		ns
t _{DS}	Data Input Set-up before CLK Rise	1.5		1.5		ns
t _{CES}	Chip Enable Set-Up before CLK Rise	1.5		1.5		ns
Hold Times						
t _{AH}	Address Hold after CLK Rise	0.5		0.5		ns
t _{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold after CLK Rise	0.5		0.5		ns
t _{ADVH}	$\overline{ADV}$ Hold after CLK Rise	0.5		0.5		ns
t _{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:B]}$ Hold after CLK Rise	0.5		0.5		ns
t _{DH}	Data Input Hold after CLK Rise	0.5		0.5		ns
t _{CEH}	Chip Enable Hold after CLK Rise	0.5		0.5		ns

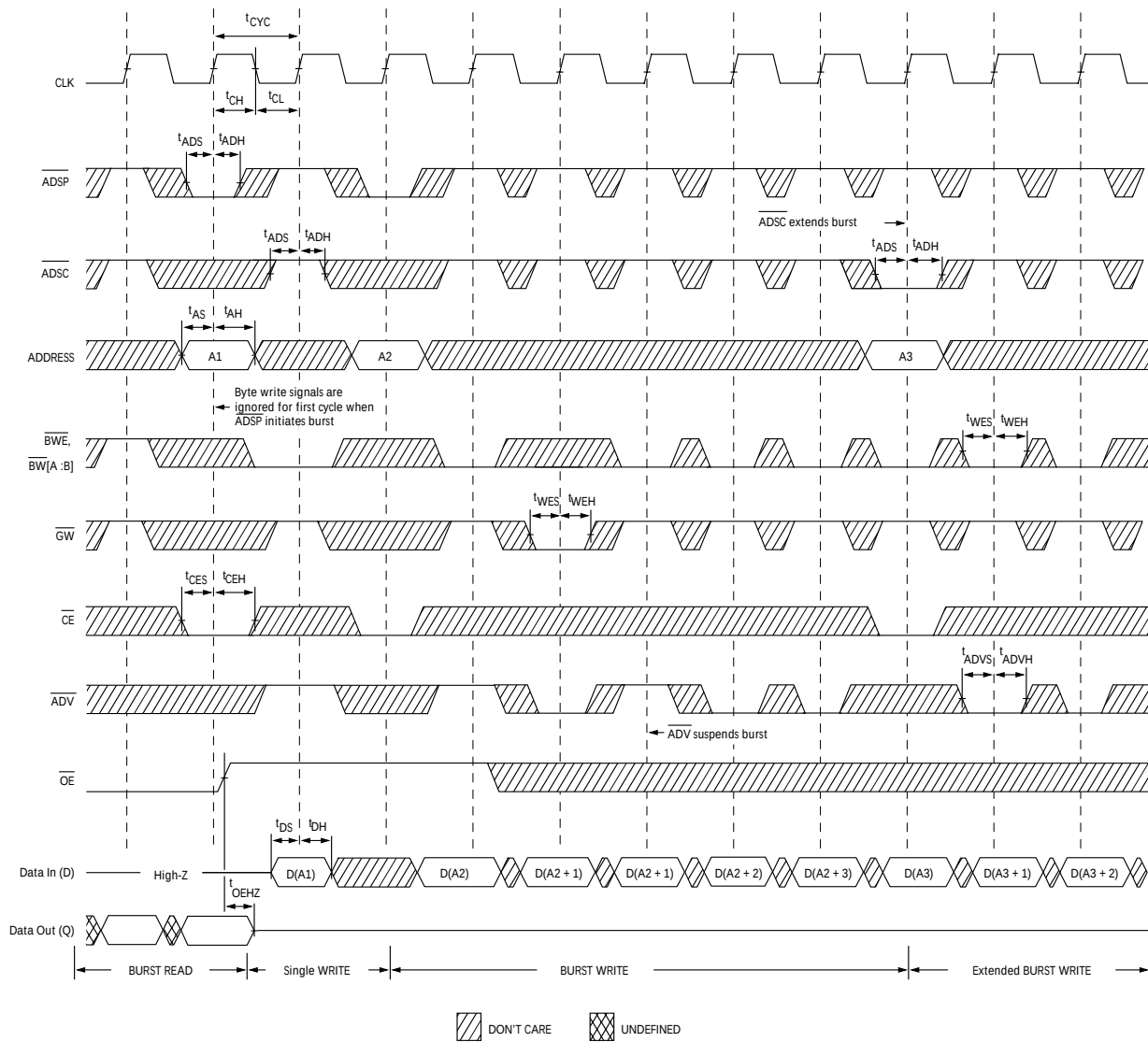
Notes:

11. Timing reference level is 1.5V when V_{DDQ} = 3.3V.
12. Test conditions shown in (a) of AC Test Loads unless otherwise noted.
13. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially before a Read or Write operation can be initiated.
14. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
15. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
16. This parameter is sampled and not 100% tested.

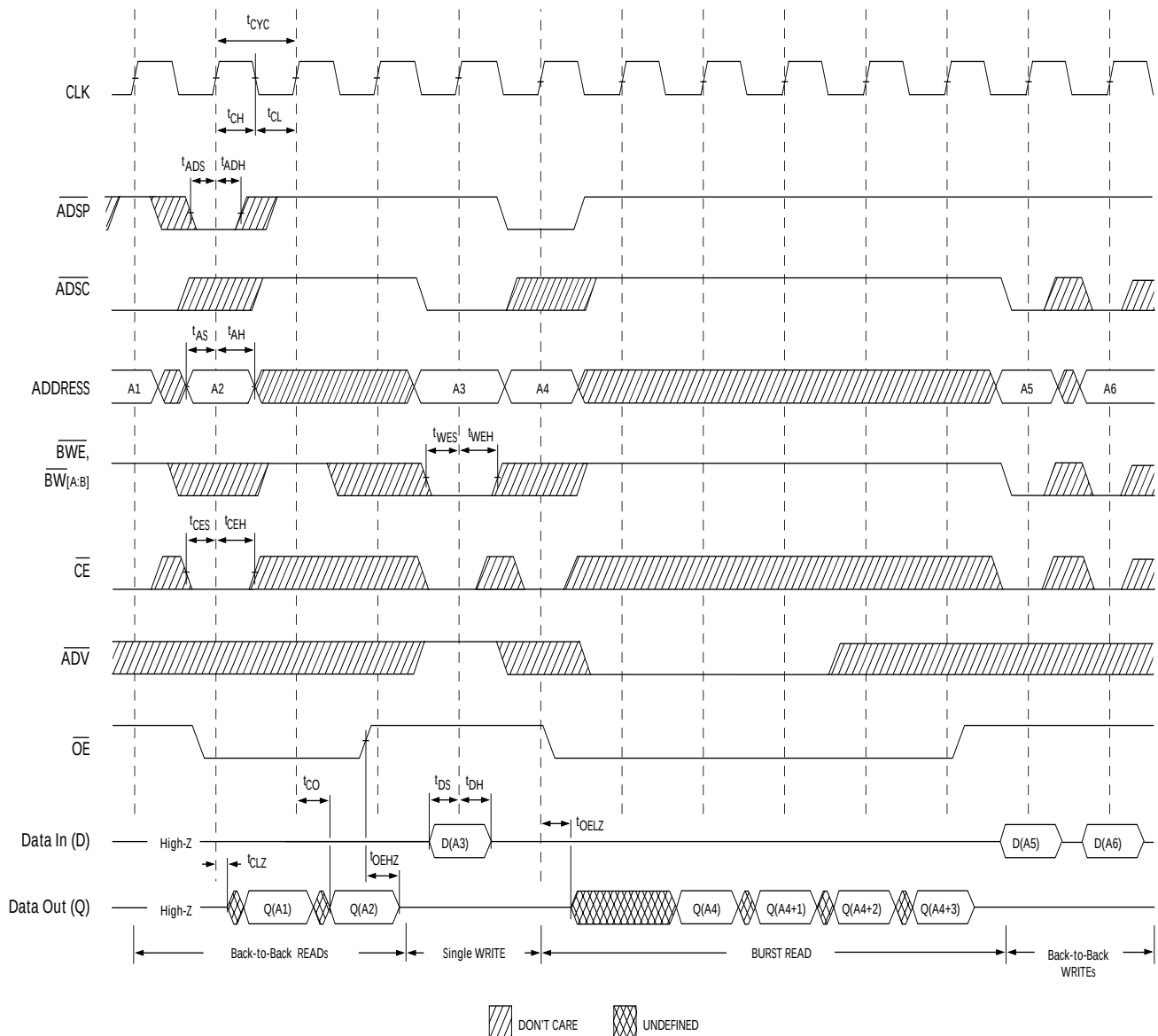


Read Cycle Timing^[17]

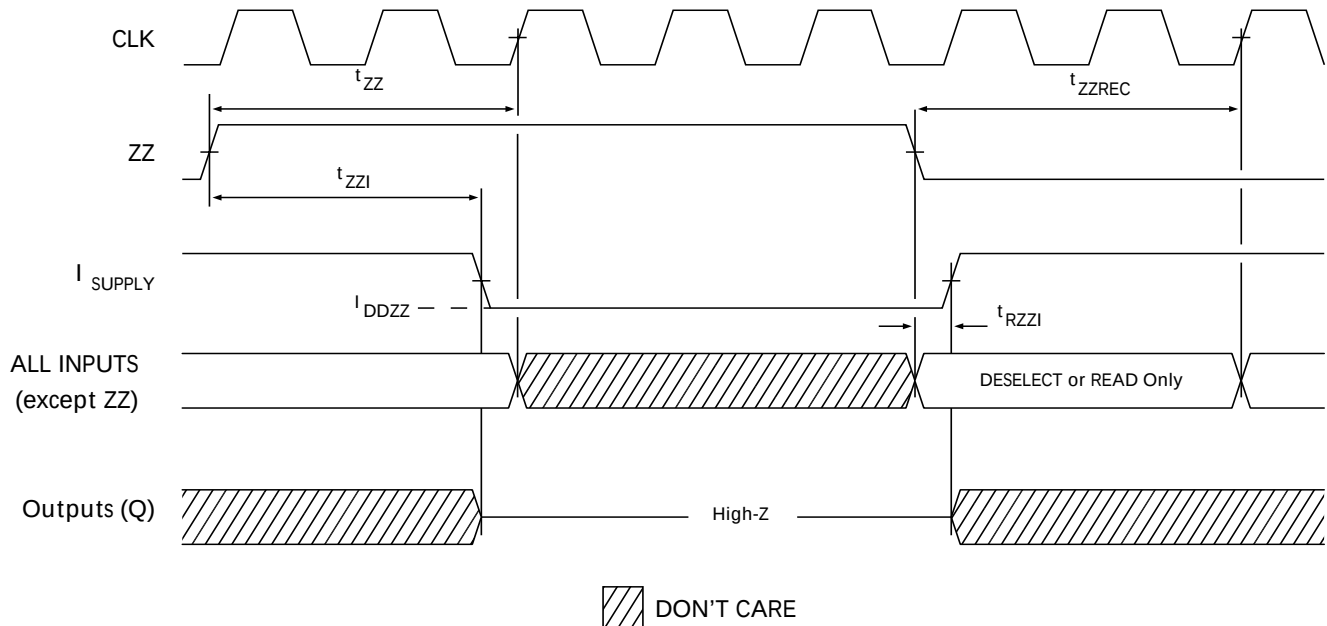


Switching Waveforms (continued)
Write Cycle Timing^[17, 18]

Note:

18. Full width Write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_{[A:B]}$ LOW.

Switching Waveforms (continued)
Read/Write Cycle Timing^[17, 19, 20]

Notes:

19. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$, or $\overline{ADV}$ cycle is performed.
 20. $\overline{GW}$ is HIGH.

Switching Waveforms (continued)
ZZ Mode Timing^[21, 22]

Notes:

21. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
 22. I/Os are in High-Z when exiting ZZ sleep mode.

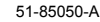
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C1326F-100AC	A101	100-Lead Thin Quad Flat Pack	Commercial

Please contact your local Cypress sales representative for availability of the 133-MHz speed grade option.



DIMENSIONS ARE IN MILLIMETERS.



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