3.3V, 125-MHz, Multi-Output Zero Delay Buffer

Features

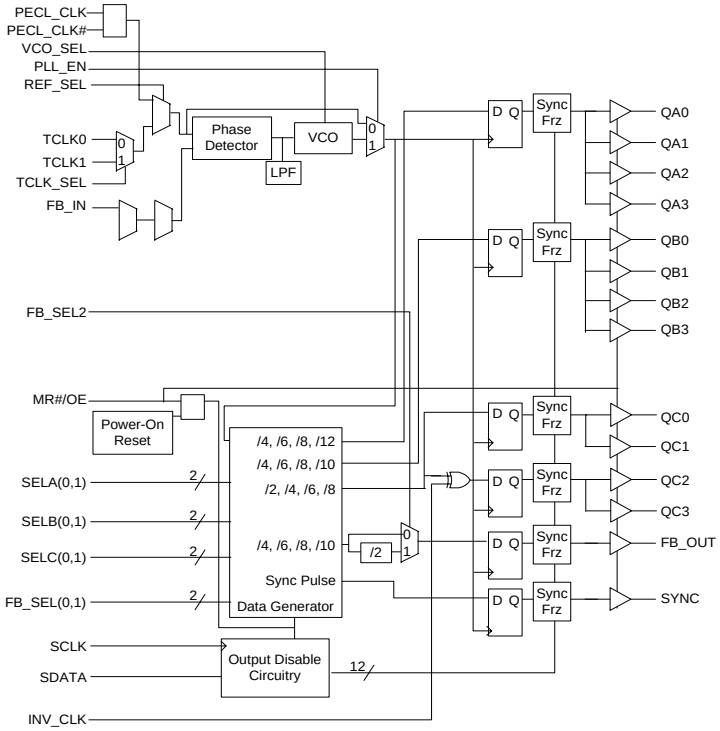
- **Output frequency up to 125 MHz**
- **12 clock outputs: frequency configurable**
- **350 ps max output-to-output skew**
- **Configurable output disable**
- **Two reference clock inputs for dynamic toggling**
- **Oscillator or PECL reference input**
- **Spread spectrum-compatible**
- **Glitch-free output clocks transitioning**
- **3.3V power supply**
- **Pin-compatible with MPC973**
- **Industrial temperature range: –40°C to +85°C**
- **52-pin TQFP package**

Table 1. Frequency Table[1]

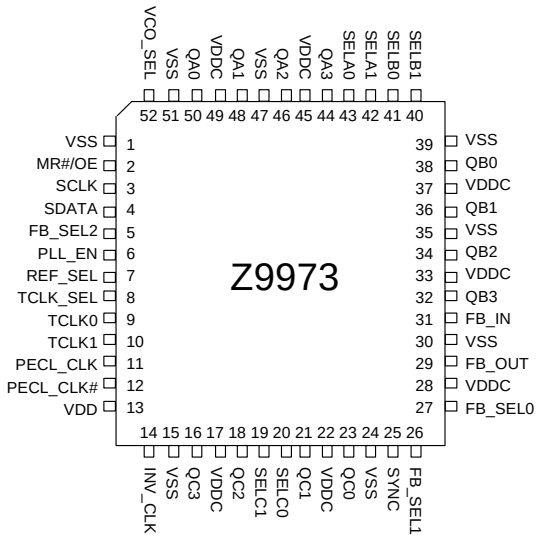
VC0_SEL	FB_SEL2	FB_SEL1	FB_SEL0	F_{VC0}
0	0	0	0	8x
0	0	0	1	12x
0	0	1	0	16x
0	0	1	1	20x
0	1	0	0	16x
0	1	0	1	24x
0	1	1	0	32x
0	1	1	1	40x
1	0	0	0	4x
1	0	0	1	6x
1	0	1	0	8x
1	0	1	1	10x
1	1	0	0	8x
1	1	0	1	12x
1	1	1	0	16x
1	1	1	1	20x

Note:
1. x = the reference input frequency, 200 MHz < F_{VCO} < 480 MHz.

Block Diagram



Pin Configuration



Pin Description [2]

Pin Number	Pin Name	PWR	I/O	Type	Pin Description
11	PECL_CLK		I	PU	**PECL Clock Input**.
12	PECL_CLK#		I	PD	**PECL Clock Input**.
9	TCLK0		I	PU	**External Reference/Test Clock Input**.
10	TCLK1		I	PU	**External Reference/Test Clock Input**.
44, 46, 48, 50	QA(3:0)	VDDC	O		**Clock Outputs**. See *Table 2* for frequency selections.
32, 34, 36, 38	QB(3:0)	VDDC	O		**Clock Outputs**. See *Table 2* for frequency selections.
16, 18, 21, 23	QC(3:0)	VDDC	O		**Clock Outputs**. See *Table 2* for frequency selections.
29	FB_OUT	VDDC	O		**Feedback Clock Output**. Connect to FB_IN for normal operation. The divider ratio for this output is set by FB_SEL(0:2). See *Table 1*. A bypass delay capacitor at this output will control Input Reference/ Output Banks phase relationships.
25	SYNC	VDDC	O		**Synchronous Pulse Output**. This output is used for system synchronization. The rising edge of the output pulse is in sync with both the rising edges of QA (0:3) and QC(0:3) output clocks regardless of the divider ratios selected.
42, 43	SELA(1,0)		I	PU	**Frequency Select Inputs**. These inputs select the divider ratio at QA(0:3) outputs. See *Table 2*.
40, 41	SELB(1,0)		I	PU	**Frequency Select Inputs**. These inputs select the divider ratio at QB(0:3) outputs. See *Table 2*.
19, 20	SELC(1,0)		I	PU	**Frequency Select Inputs**. These inputs select the divider ratio at QC(0:3) outputs. See *Table 2*.
5, 26, 27	FB_SEL(2:0)		I	PU	**Feedback Select Inputs**. These inputs select the divide ratio at FB_OUT output. See *Table 1*.
52	VCO_SEL		I	PU	**VCO Divider Select Input**. When set LOW, the VCO output is divided by 2. When set HIGH, the divider is bypassed. See *Table 1*.
31	FB_IN		I	PU	**Feedback Clock Input**. Connect to FB_OUT for accessing the phase-locked loop (PLL).
6	PLL_EN		I	PU	**PLL Enable Input**. When asserted HIGH, PLL is enabled. And when LOW, PLL is bypassed.
7	REF_SEL		I	PU	**Reference Select Input**. When HIGH, the crystal oscillator is selected. And when LOW, TCLK (0,1) is the reference clock.
8	TCLK_SEL		I	PU	**TCLK Select Input**. When LOW, TCLK0 is selected and when HIGH TCLK1 is selected.
2	MR#/OE		I	PU	**Master Reset/Output Enable Input**. When asserted LOW, resets all of the internal flip-flops and also disables all of the outputs. When pulled HIGH, releases the internal flip-flops from reset and enables all of the outputs.
14	INV_CLK		I	PU	**Inverted Clock Input**. When set HIGH, QC(2,3) outputs are inverted. When set LOW, the inverter is bypassed.
3	SCLK		I	PU	**Serial Clock Input**. Clocks data at SDATA into the internal register.
4	SDATA		I	PU	**Serial Data Input**. Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.
17, 22, 28, 33,37, 45, 49	VDDC				**3.3V Power Supply for Output Clock Buffers**.
13	VDD				**3.3V Supply for PLL**.
1, 15, 24, 30, 35, 39, 47, 51	VSS				**Common Ground**.

Note:

2. A bypass capacitor (0.1 μF) should be placed as close as possible to each positive power (< 0.2”). If these bypass capacitors are not close to the pins, their high-frequency filtering characteristics will be cancelled by the lead inductance of the traces.

Functional Description

The Z9973 has an integrated PLL that provides low-skew and low-jitter clock outputs for high-performance microprocessors. Three independent banks of four outputs as well as an independent PLL feedback output, FB_OUT, provide exceptional flexibility for possible output configurations. The PLL is ensured stable operation given that the VCO is configured to run between 200 MHz to 480 MHz. This allows a wide range of output frequencies up to125 MHz.

The phase detector compares the input reference clock to the external feedback input. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by FB_SEL(0:2) and VCO_SEL select inputs (see *Table 1*). The VCO frequency is then divided to provide the required output frequencies. These dividers are set by SELA(0,1), SELB(0,1), SELC(0,1) select inputs (see *Table 2*). For situations in which the VCO needs to run at relatively low frequencies and hence might not be stable, assert VCO_SEL LOW to divide the VCO frequency by 2. This will maintain the desired output relationships, but will provide an enhanced PLL lock range.

The Z9973 is also capable of providing inverted output clocks. When INV_CLK is asserted HIGH, QC2 and QC3 output clocks are inverted. These clocks could be used as feedback outputs to the Z9973 or a second PLL device to generate early or late clocks for a specific design. This inversion does not affect the output to output skew.

Table 2. Frequency Select Inputs

VCO_SEL	SELA1	SELA0	QA	SELB1	SELB0	QB	SELC1	SELC0	QC
0	0	0	VCO/8	0	0	VCO/8	0	0	VCO/4
0	0	1	VCO/12	0	1	VCO/12	0	1	VCO/8
0	1	0	VCO/16	1	0	VCO/16	1	0	VCO/12
0	1	1	VCO/24	1	1	VCO/20	1	1	VCO/16
1	0	0	VCO/4	0	0	VCO/4	0	0	VCO/2
1	0	1	VCO/6	0	1	VCO/6	0	1	VCO/4
1	1	0	VCO/8	1	0	VCO/8	1	0	VCO/6
1	1	1	VCO/12	1	1	VCO/10	1	1	VCO/8

Zero Delay Buffer

When used as a zero delay buffer, the Z9973 will likely be in a nested clock tree application. For these applications the Z9973 offers a low-voltage PECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The Z9973 can then lock onto the LVPECL reference and translate with near-zero delay to low-skew outputs.

By using one of the outputs as a feedback to the PLL, the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing near-zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between inputs and outputs. Because the static phase offset is a function of the reference clock, the Tpd of the Z9973 is a function of the configuration used.

Glitch-Free Output Frequency Transitions

Customarily, when output buffers have their internal counters changed “on the fly,” their output clock periods will:

1. contain short or “runt” clock periods. These are clock cycles in which the cycle(s) are shorter in period than either the old or new frequency to which it is being transitioned.
2. contain stretched clock periods. These are clock cycles in which the cycle(s) are longer in period than either the old or new frequency to which it is being transitioned.

This device specifically includes logic to guarantee that runt and stretched clock pulses do not occur if the device logic levels of any or all of the following pins changed “on the fly” while it is operating: SELA, SELB, SELC, and VCO_SEL.

SYNC Output

In situations where output frequency relationships are not integer multiples of each other, the SYNC output provides a signal for system synchronization. The Z9973 monitors the relationship between the QA and the QC output clocks. It provides a low-going pulse, one period in duration, one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse depend on the higher of the QA and QC output frequencies. The following timing diagram illustrates various waveforms for the SYNC output (see *Figure 1*). **Note**. The SYNC output is defined for all possible combinations of the QA and QC outputs even though under some relationships the lower frequency clock could be used as a synchronizing signal.

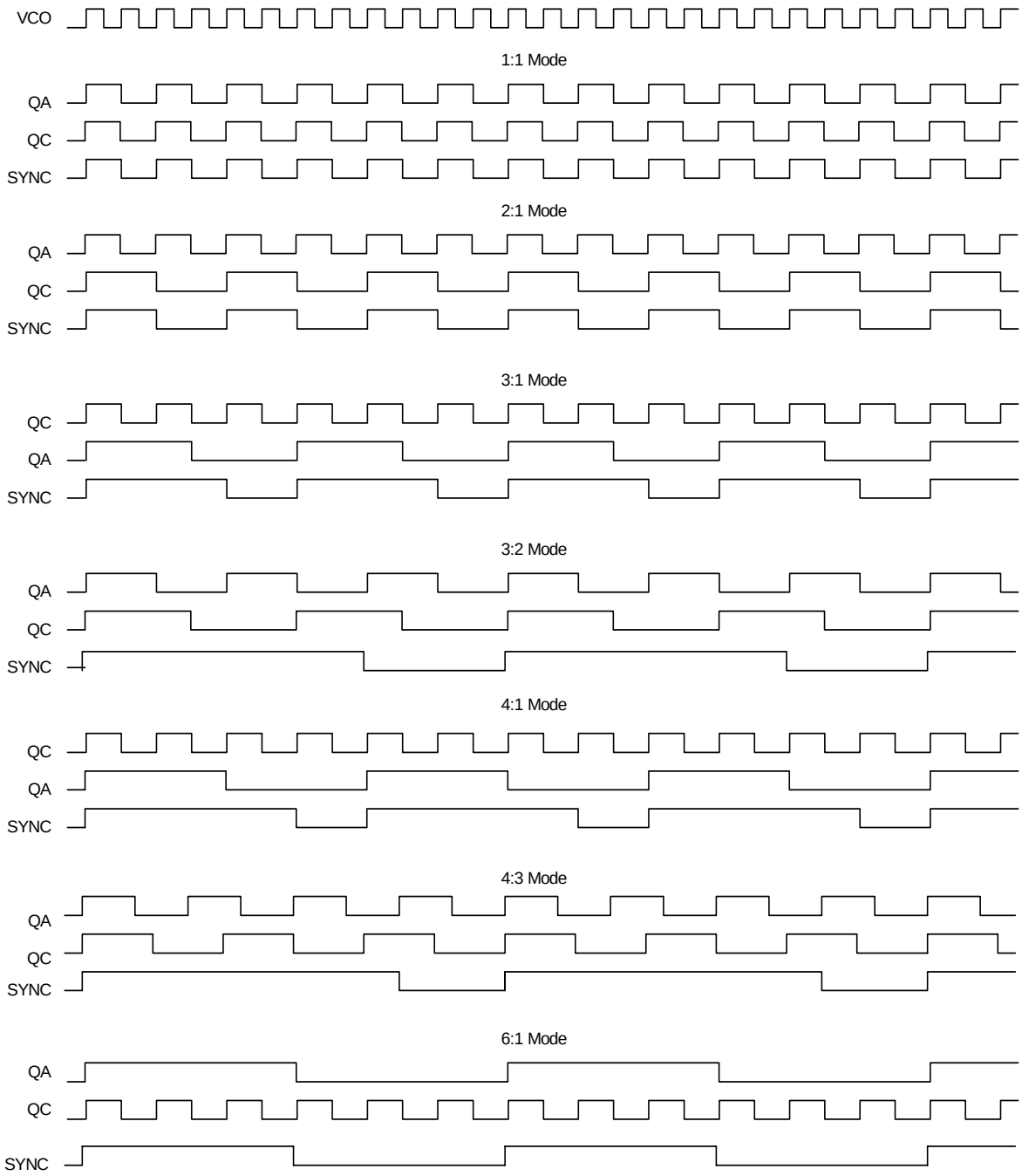


Figure 1. Sync Output Waveforms

Power Management

The individual output enable/freeze control of the Z9973 allows the user to implement unique power management schemes into the design. The outputs are stopped in the logic “0” state when the freeze control bits are activated. The serial input register contains one programmable freeze enable bit for 12 of the 14 output clocks. The QC0 and FB_OUT outputs cannot be frozen with the serial port, which avoids any potential lock-up situation should an error occur in loading the serial data. An output is frozen when a logic “0” is programmed and enabled when a logic “1” is written. The enabling and freezing of individual outputs is done in such a manner as to eliminate the possibility of partial “runt” clocks.

The serial input register is programmed through the SDATA input by writing a logic “0” start bit followed by 12 NRZ freeze enable bits (see *Figure 2*). The period of each SDATA bit equals the period of the free-running SCLK signal. The SDATA is sampled on the rising edge of SCLK.

D0-D3 are the control bits for QA0-QA3, respectively
D4-D7 are the control bits for QB0-QB3, respectively
D8-D10 are the control bits for QC1-QC3, respectively
D11 is the control bit for SYNC

Figure 2. SDATA Input Register

Maximum Ratings[3]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: .....–65°C to + 150°C

Operating Temperature: .....–40°C to +85°C

Maximum ESD protection .....2 kV

Maximum Power Supply: 5.5V

Maximum Input Current:.....±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range:

$V_{SS} < (V_{IN} \text{ or } V_{OUT}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters (V_{DD} = 2.9V to 3.6V, V_{DDC} = 3.3V ±10%, T_A = –40°C to +85°C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Voltage		V_{SS}		0.8	V
V_{IH}	Input HIGH Voltage		2.0		V_{DD}	V
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		300		1000	mV
V_{CMR}	Common Mode Range PECL_CLK[9]		V_{DD} – 2.0		V_{DD} – 0.6	V
I_{IL}	Input Low Current[10]				–120	µA
I_{IH}	Input High Current[10]				120	µA
V_{OL}	Output Low Voltage[11]	I_{OL} = 20 mA			0.5	V
V_{OH}	Output High Voltage[11]	I_{OH} = –20 mA	2.4			V
I_{DDQ}	Quiescent Supply Current			10	15	mA
I_{DDA}	PLL Supply Current	V_{DD} only		15	20	mA
I_{DD}	Dynamic Supply Current	QA and QB @ 60 MHz, QC @ 120 MHz, C_L = 30 pF		225		mA
		QA and QB @ 25 MHz, QC @ 50 MHz, C_L = 30 pF		125		
C_{IN}	Input Pin Capacitance			4		pF

AC Parameters (V_{DD} = 2.9V to 3.6V, V_{DDC} = 3.3V ±10%, T_A = –40°C to +85°C) [4]

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
Tr / Tf	TCLK Input Rise / Fall				3.0	ns
Fref	Reference Input Frequency		Note 5		Note 5	MHz
FrefDC	Reference Input Duty Cycle		25		75	%
Fvco	PLL VCO Lock Range		200		480	MHz
Tlock	Maximum PLL Lock Time				10	ms
Tr / Tf	Output Clocks Rise/Fall Time[6]	0.8V to 2.0V	0.15		1.2	ns

Notes:

3. The voltage on any input or I/O pic cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
4. Parameters are guaranteed by design and characterization. Not 100% tested in production.
5. Maximum and minimum input reference is limited by VC0 lock range.
6. Outputs loaded with 30 pF each.

AC Parameters (V_{DD} = 2.9V to 3.6V, V_{DDC} = 3.3V ±10%, T_A = –40°C to +85°C) (Continued)[4]

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
Fout	Maximum Output Frequency	Q (÷2)			125	MHz
		Q (÷4)			120	
		Q (÷6)			80	
		Q (÷8)			60	
FoutDC	Output Duty Cycle[6]		TCYCLE /2 – 750		TCYCLE /2 + 750	ps
tpZL, tpZH	Output Enable Time[6](all outputs)		2		10	ns
tpLZ, tpHZ	Output Disable Time[6](all outputs)		2		8	ns
TCCJ	Cycle to Cycle Jitter (peak to peak)[6]			± 100		ps
TSKEW	Any Output to Any Output Skew[6,7]			250	350	ps
	Propagation Delay[7,8]		–225	–25	175	ps
Tpd		QFB = (÷8)	–70	130	330	
			–130	70	270	

Ordering Information

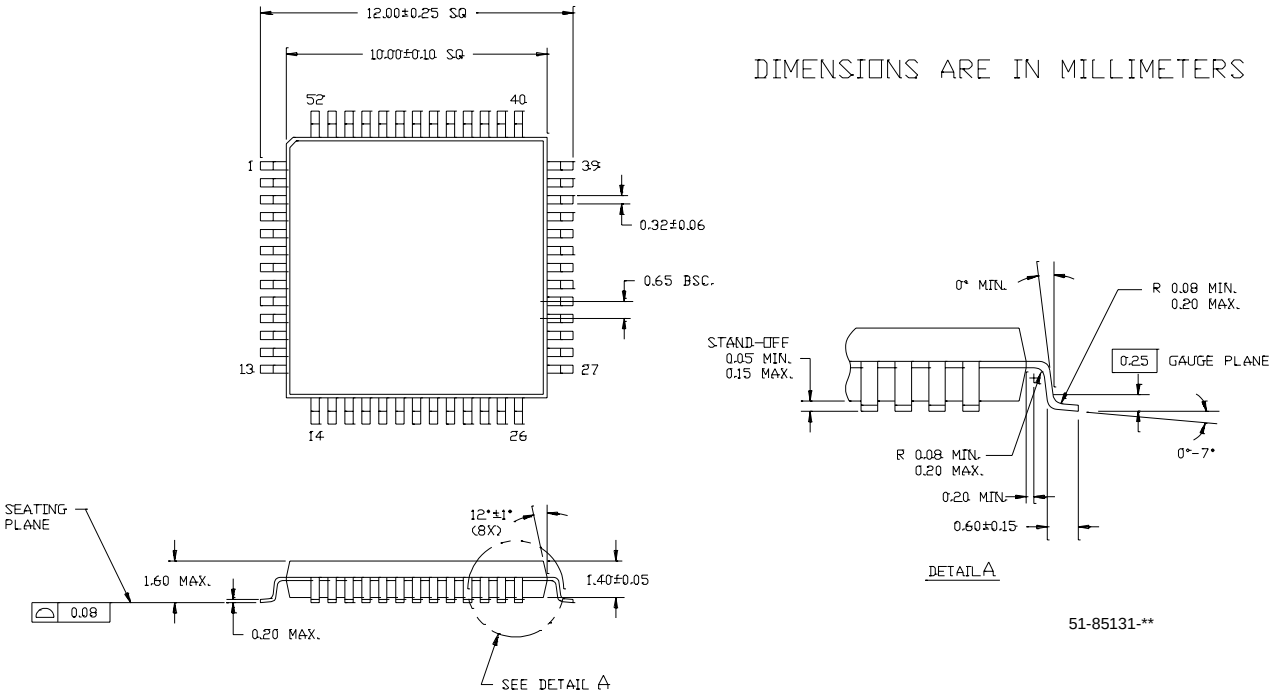
Part Number	Package Type	Production Flow
IMIZ9973BA	52-pin TQFP	Industrial, –40°C to +85°C
IMIZ9973BAT	52-pin TQFP–Tape and Reel	Industrial, –40°C to +85°C

Notes:

7. 50Ω transmission line terminated into VDD/2.
8. Tpd is specified for a 50-MHz input reference. Tpd does not include jitter.
9. The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the VCMR range and the input lies within the VPP specification.
10. Inputs have pull-up/pull-down resistors that effect input current.
11. Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines.

Package Drawing and Dimensions

52-lead Thin Plastic Quad Flat Pack (10 × 10 × 1.4 mm) A52



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Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107125	06/06/01	IKA	Convert from IMI to Cypress
*A	108067	07/03/01	NDP	Changed Commercial to Industrial
*B	111799	02/06/02	BRK	Convert from Word Doc to Adobe Framemaker Cypress Format Changed the Timing Diagram and the operating voltage condition
*C	116452	07/30/02	HWT	Corrected the Ordering Information to match the DevMaster.
*D	122774	12/21/02	RBI	Add power up requirements to maximum ratings information.