Fast, Complete 12-Bit A/D Converters

AD ADC84/AD ADC85/AD5240

FEATURES

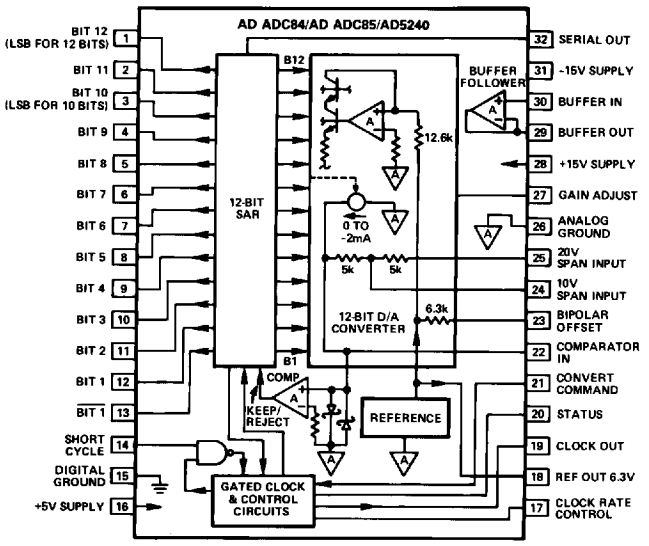
Performance

Complete 12-Bit A/D Converter with Reference and Clock
Fast Successive Approximation Conversion: 10μs or 5μs
Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C
Max Nonlinearity: <±0.012%
Low Power: 880mW Typical
Low Chip Count – High Reliability
Industry Standard Pin Out
"Z" Models for ±12V Operation Available
MIL-STD-883B Processing Available

Versatility

Negative-True Parallel or Serial Logic Outputs
Short Cycle Capability
Precision +6.3V Reference for External Applications

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC84/AD ADC85/AD5240 series devices are high-speed, low-cost 10- and 12-bit successive approximation analog-to-digital converters that include internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC84/AD ADC85/AD5240 series include a maximum linearity error at +25°C of ±0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 880mW, and conversion time of less than 10μs for the 12-bit versions. Of considerable significance in severe and aerospace applications is the guaranteed performance from -55°C to +125°C of the AD ADC85S which is also available with environmental screening. Monotonic operation of the feedback D/A converter guarantees no missing codes over temperature ranges of 0 to +70°C, -25°C to +85°C, and -55°C to +125°C.

The design of the AD ADC84/AD ADC85/AD5240 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +6.3V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is negative-true and available in either serial or parallel form.

The AD ADC84/AD ADC85/AD5240 series devices are available in two different performance grades. The devices are specified for either 10-bit accuracy (±0.048% FSR max) or 12-bit accuracy (±0.012% FSR max) with 8.4μs, 10μs (AD ADC84/AD ADC85) and 4.1μs, 5μs (AD5240) max conversion times respectively.

The AD ADC84 and AD ADC85C specified for operation over the 0 to +70°C temperature range. The AD ADC85 and AD ADC85S are specified for the -25°C to +85°C, -55°C to +125°C ranges respectively.

PRODUCT HIGHLIGHTS

1. The AD ADC84/AD ADC85/AD5240 series devices are complete 12-bit A/D converters. No external components are required to perform a conversion.
2. The AD ADC84/AD ADC85/AD5240 directly replaces other devices of this type with significant increases in performance.
3. The fast conversion rates of the AD ADC84/AD ADC85 (10μs) and AD5240 (5μs) make them an excellent choice for applications requiring high system throughput rates.
4. The internal buried zener reference is laser trimmed to 6.3V ±0.1% and ±10ppm/°C typical T.C. The reference is available externally and can provide up to 1mA.
5. The integrated package construction provides high quality and reliability with small size and weight.
6. The monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
7. The AD ADC85S/883B and AD5240SD/883B come processed to MIL-STD-883, Class B requirements (see ADI Military Products Databook).

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD ADC 84/AD ADC85/AD5240—SPECIFICATIONS (typical@ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD ADC84	AD ADC85C	AD ADC85	AD ADC85S	AD5240KD/ AD5240SD	UNITS
RESOLUTION	10/12	10/12	10/12	10/12	12	Bits
ANALOG INPUTS						
Voltage Ranges						
Bipolar	±2.5, ±5, ±10	*	*	*	*	Volts
Unipolar	0 to +5, 0 to +10	*	*	*	*	Volts
Impedance (Direct Input)						
0V to +5V, ±2.5V	2.5(±20%)	*	*	*	*	kΩ
0V to +10V, ±5V	5(±20%)	*	*	*	*	kΩ
±10V	10(±20%)	*	*	*	*	kΩ
Buffer Amplifier[1]						
Impedance (min)	100	*	*	*	*	MΩ
Bias Current	50	*	*	*	*	nA
Settling Time						
To 0.01% for 20V Step	2	*	*	*	*	μs
DIGITAL INPUTS[2]						
Convert Command	Positive Pulse 100ns min Trailing Edge Initiates Conversion	*	*	*	*	
Logic Loading	1	*	*	*	*	TTL Load
TRANSFER CHARACTERISTICS ERROR						
Gain Error[3]	±0.1(±0.25% max)	*	*	*	±0.2	%
Offset Error[3]	Adjustable to Zero	*	*	*	*	
Unipolar	±0.05(±0.2% max)	*	*	*	±0.1	% of FSR[4]
Bipolar[5]	±0.1(±0.25% max)	*	*	*	±0.2	% of FSR
Linearity Error (max)[6]	±0.048/±0.012	*	*	*	±0.012	% of FSR
Inherent Quantization Error	±0.5	*	*	*	*	LSB
Differential Linearity Error	±0.5	*	*	*	*	LSB
No Missing Codes Temperature Range	0 to +70	0 to +70	−25 to +85	−55 to +125	0 to +70/−55 to +125	°C
Power Supply Sensitivity						
±15V	±0.004	*	*	*	*	% of FSR/%V
+5V	±0.001	*	*	*	*	% of FSR/%V
DRIFT						
Specification Temperature Range	0 to +70	*	−25 to +85	−55 to +125	0 to +70/−55 to +125	°C
Gain (max)	±30	±40/±25	±20/±15	±25	±30/±25	ppm/°C
Offset						
Unipolar	±3	*	*	±5 max	*	ppm/°C
Bipolar (max)[5]	±15	±20/±12	±10/±7	±10	±15/±7	ppm/°C
Linearity (max)	±3	*	±3/±2	*	±2	ppm/°C
Monotonicity	GUARANTEED	*	*	*	GUARANTEED	
CONVERSION SPEED (MAX)	8.4/10	*	*	*	5	μs
DIGITAL OUTPUT						
(all codes complementary)						
Parallel						
Output Codes[7]						
Unipolar	CSB	*	*	*	*	
Bipolar	COB, CTC	*	*	*	*	
Output Drive	2	*	*	*	*	TTL Loads
Serial Data Codes (NRZ)	CSB, COB	*	*	*	*	
Output Drive	2	*	*	*	*	TTL Loads
Status	Logic "1" during Conversion	*	*	*	*	
Status Output Drive	2	*	*	*	*	TTL Loads
Internal Clock						
Clock Output Drive	2	*	*	*	*	TTL Loads
Frequency	1.9/1.22	*	*	*	2.6	MHz
INTERNAL REFERENCE VOLTAGE	6.3/±15mV max	*	*	*	*	Volts
Max. External Current (with no degradation of specifications)	1.0	*	*	*	*	mA
Tempco of Drift, (max)	±20/max	±10 typ	±5 typ	±5 typ	±10	ppm/°C
POWER REQUIREMENTS						
Rated Voltages	+5, ±15	*	*	*	*	Volts
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*	*	Volts
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	*	*	*	*	Volts
Supply Drain +15V	25 max	*	*	*	15 max	mA
−15V	35 max	*	*	*	35 max	mA
+5V	140 max	*	*	*	100 max	mA
Total Power Dissipation	1500 max	*	*	*	1100 max	mW
TEMPERATURE RANGE						
Specification	0 to +70	*	−25 to +85	−55 to +125	0 to +70/−55 to +125	°C
Operating (Derated Specs)	−25 to +85	*	−55 to +125	−55 to +125	−55 to +125	°C
Storage	−55 to +125	*	*	*	−65 to +150	°C
PACKAGE OPTION[9]						
DH-32F	Ceramic	Ceramic	Ceramic	Ceramic	Ceramic	

NOTES

[1] Buffer Settling time adds to conversion speed when buffer is connected to input.

[2] DTL/TTL compatible Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital output, Logic "0" = 0.4V max, Logic "1" = 2.4V min.

[3] Adjustable to zero.

[4] FSR means Full Scale Range.

[5] Guaranteed at V_{IN} = 0 volts.

[6] Error shown is the same as ±1/2LSB max error in % of FSR.

[7] See Table I.

[8] For ±12V operation add "Z" to model number. Input range limited to a maximum of ±5V.

[9] For package outline information see Package Information section.

*Specifications same as AD ADC84.

Specifications subject to change without notice.

Typical Performance Curves – AD ADC84/AD ADC85/AD5240

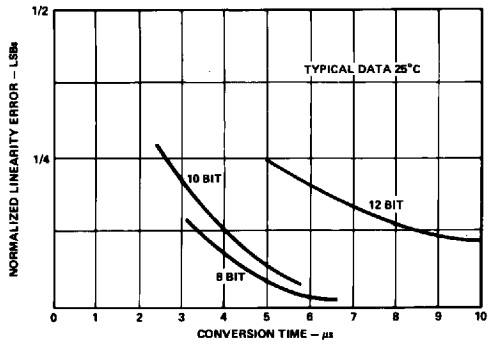


Figure 1a. Linearity Error vs. Conversion Speed (AD ADC84/AD ADC85)

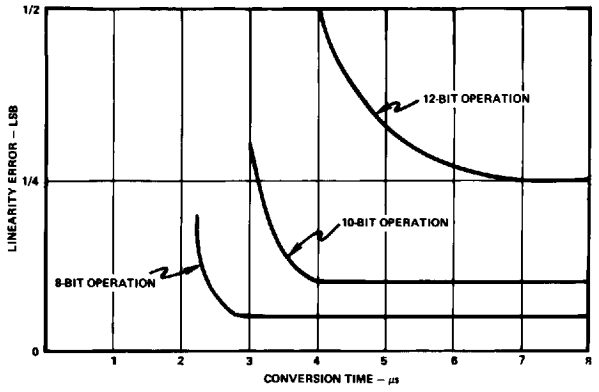


Figure 1b. Linearity Error vs. Conversion Speed (AD5240)

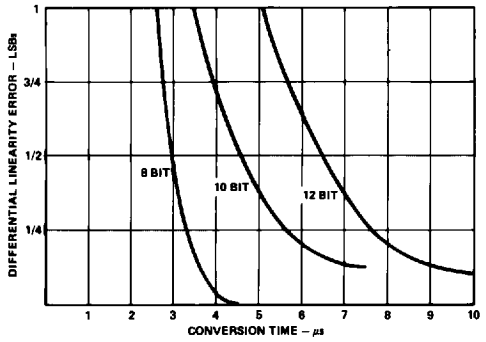


Figure 2a. Change in Differential Linearity vs. Conversion Speed (AD ADC84/AD ADC85)

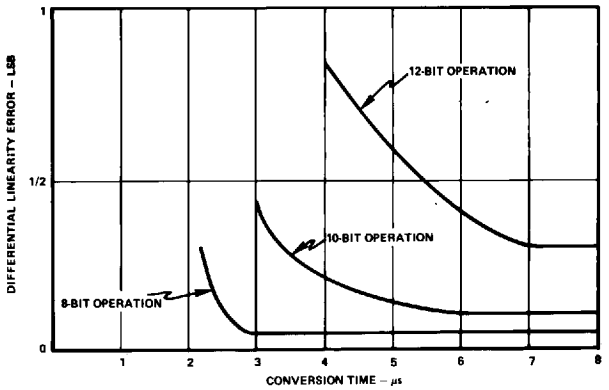


Figure 2b. Change in Differential Linearity vs. Conversion Speed (AD5240)

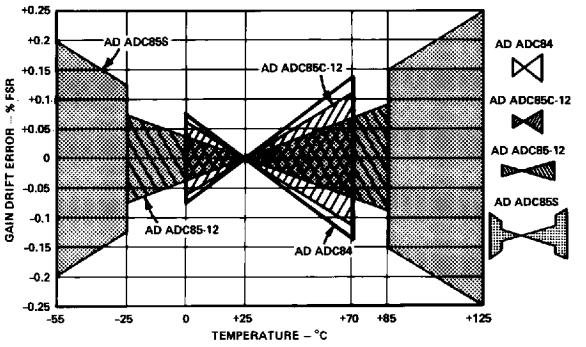


Figure 3a. Gain Drift Error (% FSR) vs. Temperature (AD ADC84/AD ADC85)

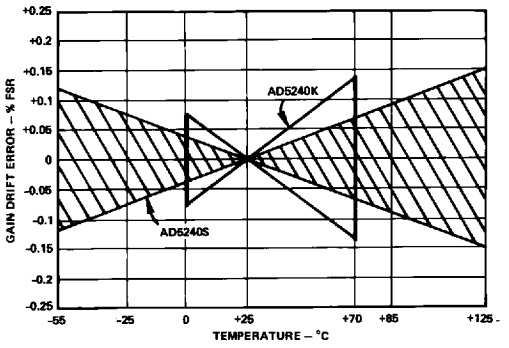


Figure 3b. Gain Drift Error (% FSR) vs. Temperature (AD5240)

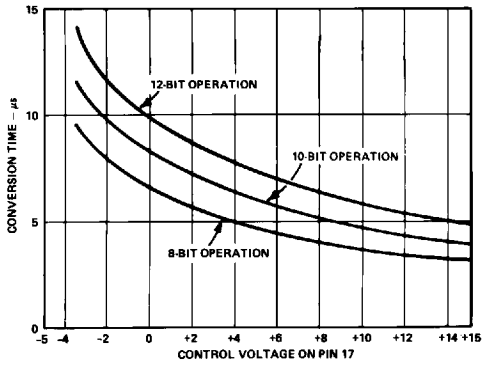


Figure 4a. Conversion Speed vs. Control Voltage (AD ADC84/AD ADC85)

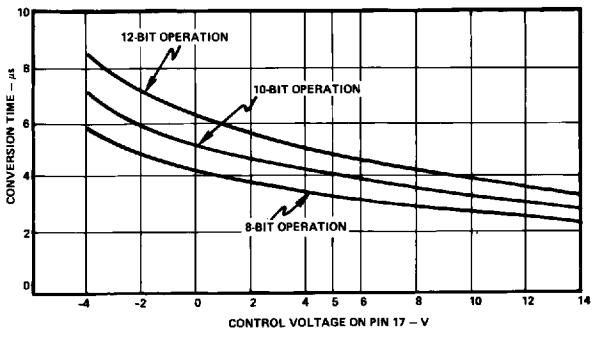


Figure 4b. Conversion Speed vs. Control Voltage (AD5240)

ORDERING GUIDE

Model[1]	Linearity	Temperature Range	Gain T. C. – ppm/°C	Conversion Time
AD ADC84-10	±0.048%	0 to +70°C	±30	10μs
AD ADC84-12	±0.012%	0 to +70°C	±30	10μs
AD ADC85C-10	±0.048%	0 to +70°C	±40	10μs
AD ADC85C-12	±0.012%	0 to +70°C	±25	10μs
AD ADC85-10	±0.048%	-25°C to +85°C	±20	10μs
AD ADC85-12	±0.012%	-25°C to +85°C	±15	10μs
AD ADC85S-10	±0.048%	-55°C to +125°C	±25	10μs
AD ADC85S-12	±0.012%	-55°C to +125°C	±25	10μs
AD5240KD	±0.012%	0 to +70°C	±30	5μs
AD ADC85S-12/883B	±0.012%	-55°C to +125°C	±25	10μs
AD5240SD/883B	±0.012%	-55°C to +125°C	±25	5μs

[1] For complete model number suffixes must be added for "Z" option (±12V operation), linearity. The following guide shows the proper suffix order.
AD ADC (*)(**)-(***)

*Model Number
**"Z" Version Designator
***Linearity

Typical Part Numbers
AD ADC84-12
AD ADC85SZ-12
AD5240ZKD

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 22 for all ranges. As shown in Figure 5 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

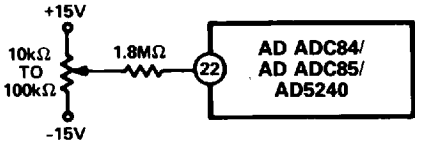


Figure 5. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 5.

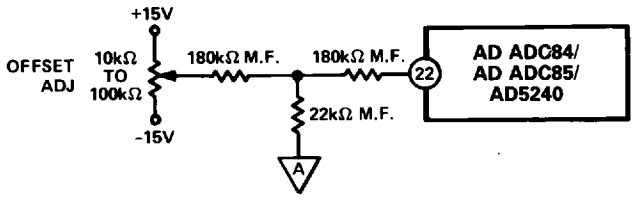


Figure 6. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 22 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 27 as shown in Figure 7.

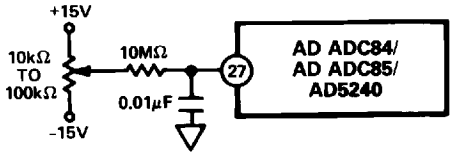


Figure 7. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 8.

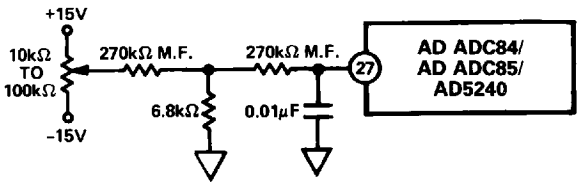


Figure 8. Low Tempco Gain Adjustment Circuit

THEORY OF OPERATION

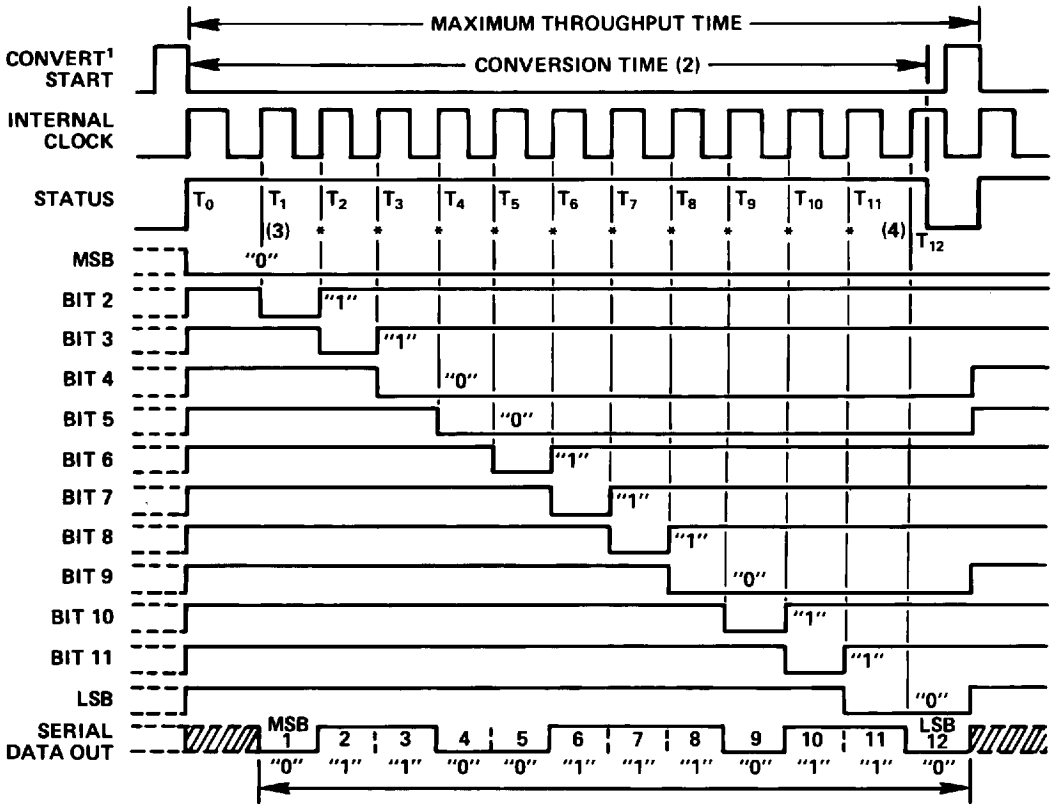
On receipt of a CONVERT START command, the AD ADC84/AD ADC85/AD5240 converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 9. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 – B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking into a receiving shift register on these edges (see Figure 9).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES

1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 10μs FOR 12 BITS AND 8.4μs FOR 10 BITS (AD ADC84/AD ADC85) OR 5μs FOR 12 BITS AND 4.1μs FOR 10 BITS (AD5240).
3. MSB DECISION.
4. LSB DECISION 20ns PRIOR TO THE STATUS GOING LOW.

*BIT DECISIONS.

Figure 9. Timing Diagram (Binary Code 0 1 1 0 0 1 1 1 0 1 1 0)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 9. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 9. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 9 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 9). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I.

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	AD ADC84/ AD ADC85 (AD5240) Conversion Time (μs)	Status Flag Reset
16	15	12	0.024	10 (5)	t_{12} +40ns
2	16	10	0.100	8.5 (4.1)	t_{10} +40ns
4	28	8	0.390	6.8 (3.3)	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC84/AD ADC85/AD5240 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 10 for circuit detail.

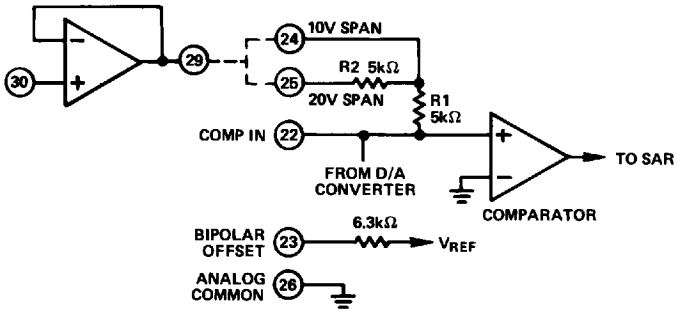


Figure 10. Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
±10V	COB or CTC	22	Input Signal	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24

Table II. Input Scaling Connections

INPUT VOLTAGE RANGE AND LSB VALUES

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available to pin 13.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definition

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 11 and 12, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

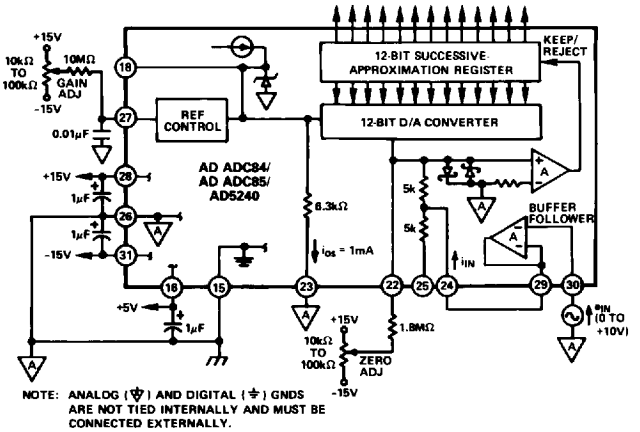


Figure 11. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower

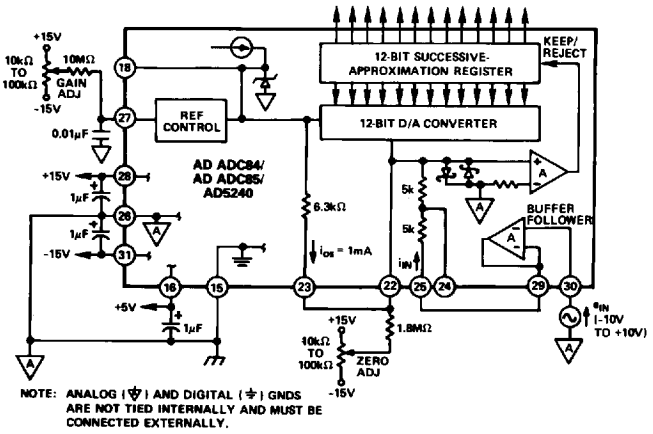


Figure 12. Analog and Power Connections for Bipolar −10V to +10V Input Range with Buffer Follower

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 011111111111.

Other Ranges: Representative digital coding for 0 to +10V and -10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, -2.5V to +2.5V and -5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC84/AD ADC85/AD5240. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC84/AD ADC85/AD5240's supply terminals should be capacitively decoupled as close to the device as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the CLOCK RATE is desired for faster conversion speeds, the CLOCK RATE CONTROL may be connected to an external multi-turn trim potentiomer with a TCR of ±100ppm/°C or less as shown in Figures 13 and 14. If the potentiometer is connected to -15V, conversion time can be increased as shown in Figures 4a and 4b. If these adjustments are used, delete the connections shown in Table I for pin 17. See Figures 1a and 1b for nonlinearity error vs. conversion speed and Figures 4a and 4b for the effect of the control voltage on clock speed.

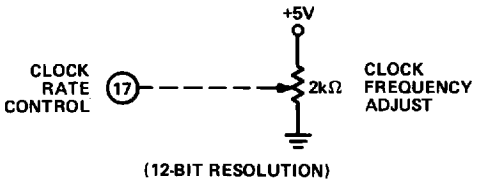


Figure 13. 12-Bit Clock Rate Control Optional Fine Adjust

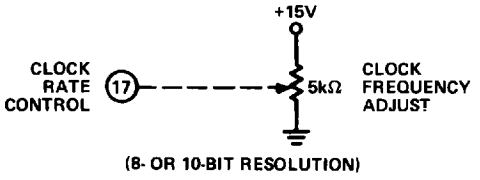


Figure 14. 8-Bit Clock Rate Control Optional Fine Adjust

MICROPROCESSOR INTERFACING

The fast conversion times of the AD ADC84/AD ADC85 and AD5240 suggest several different methods of interface to microprocessors. In systems where the ADC is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least-significant 8 bits occupy one byte and the four MSB's reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSB's in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

Figure 15 shows a typical connection of an 8085-type bus, using a left-justified data format for unipolar inputs. Status polling is optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD ADC84/AD ADC85/AD5240 should be reversed,

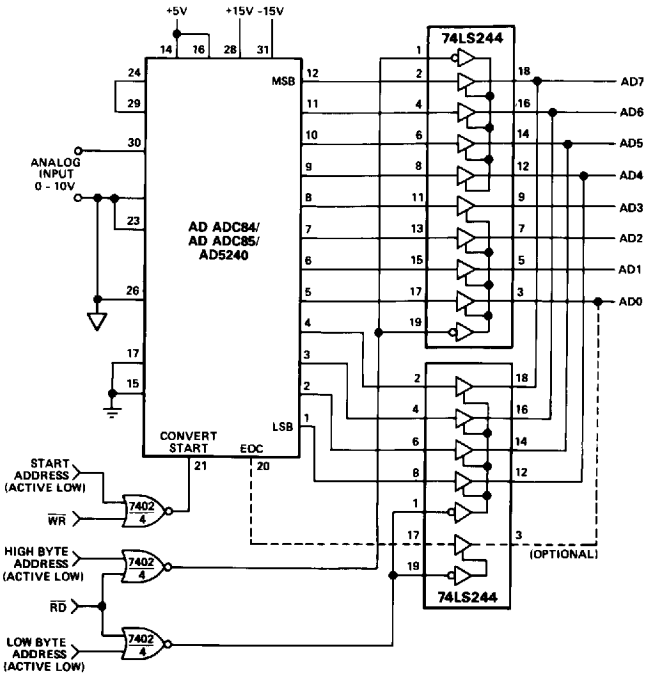


Figure 15. AD ADC84/AD ADC85/AD5240 – 8085A Interface Connections

as well as the connections to the data bus high and low byte address signals.

When dealing with bipolar inputs (±5V, ±10V ranges), using the MSB directly yields a complementary offset binary-coded output. If complementary two's complement coding is desired, it can be produced by substituting $\overline{\text{MSB}}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

OUTLINE DIMENSIONS

Dimensions shown in inches (mm)

DH-32E Package