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Two's Complement, Dual
12-Bit DACs, Internal REF

Preliminary Technical Data

AD5399

FEATURES

- Monotonic DNL $< \pm 1$ LSB
- Improved Accuracy at Zero Scale
- Fast $1\mu\text{s}$ Settling Time
- Power ON Reset
- 3-Wire Serial Data Input
- 28MHz Data Load Rate
- Internal Reference Voltage
- +4.5V to +5.5V Single Supply Operation

APPLICATIONS

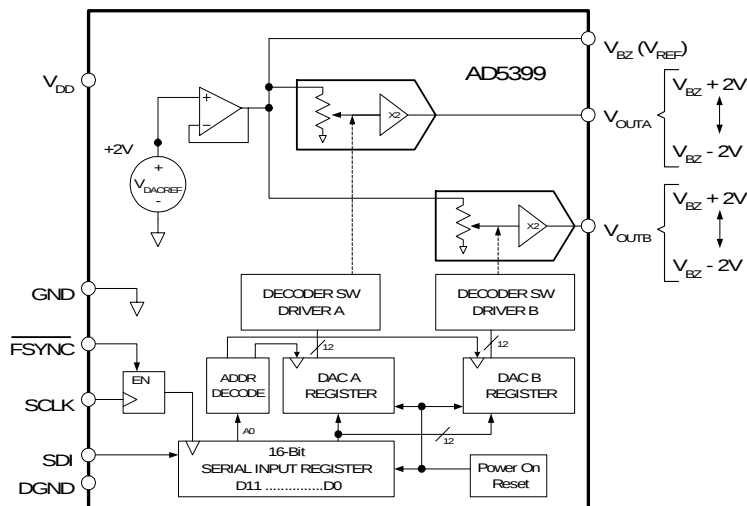
- Digital Control of Gain & Offset

GENERAL DESCRIPTION

The AD5399 is a serial-input, dual 12-bit digital-to-analog converter that accepts two's complement digital coding. An internal voltage reference generates a stable 2V DACREF. The buffered DACREF output generates the system bipolar ground reference at pin V_{BZ} . The bipolar DAC output swing programs over a $4V_{pp}$ range. The device is specified for operation from +5 volts $\pm 10\%$.

Data is loaded MSB first on the positive clock edge (SCLK) when the frame synch (FSYNC) input is active low. The serial clock input word is 16-bits with the MSB position containing an address bit. The last 12 data bits clocked into the register will be transferred to the internal DAC register when the strobe input is returned to logic high.

FUNCTIONAL BLOCK DIAGRAM



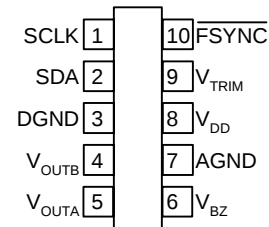
The output transfer equation is:

$$V_{OUT} = [(D-2048) / 4096 * V_{DACREF}] + V_{BZ}$$

Where D is the 12-bit decimal data, and V_{OUT} , V_{DACREF} , V_{BZ} are with respect to ground.

The AD5399 is available in the compact 1.1mm thin $\mu\text{SOIC-10}$ package. All parts are guaranteed to operate over the industrial temperature range of 0°C to $+70^\circ\text{C}$.

PIN CONFIGURATION



ORDERING GUIDE

Model	RES (bits)	Temp Range	Package Description	Package Option	Top Brand
AD5399KRM-REEL7	12	$0/+70^\circ\text{C}$	$\mu\text{SOIC-10}$	RM-10	DHB
AD5399SRM-REEL7	12	$-40/+125^\circ\text{C}$	$\mu\text{SOIC-10}$	RM-10	

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AD5399 - SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($V_{DD} = +5V \pm 10\%$, $0^\circ C < T_A < +70^\circ C$ unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Units
DC CHARACTERISTICS						
Resolution	N		12			Bits
Differential Nonlinearity Error	DNL		-1	± 0.5	+1	LSB
Integral Nonlinearity Error	INL		-0.25	± 0.02	+0.25	%FS
Integral Nonlinearity Error	INL	Within 256 codes of V_{BZ}	-0.02	± 0.01	+0.02	%FS
Positive-Full-Scale Error	V_{+FSE}	Code = 7FF _H	-0.25	-0.05	+0.25	%FS
Bipolar-Zero-Scale Error	V_{BZSE}	Code = 000 _H	-0.1	± 0.01	+0.1	V
Negative-Full-Scale Error	V_{-FSE}	Code = 800 _H	-0.25	-0.05	+0.25	%FS
ANALOG OUTPUTS						
Nominal Positive Full-Scale	$V_{OUTA/B}$	Code = 7FF _H		4		Volts
Positive Full-Scale Tempco ²	$TCV_{OUTA/B}$	Code = 7FF _H		± 50		ppm/°C
Nominal V_{BZ} Output Voltage	V_{BZ}			2		Volts
Bipolar-Zero Output Resistance ²	R_{BZ}			1		Ohm
Nominal Peak-Peak Output Swing	$ V_{+FS} + V_{-FS} $	Code 7FF _H to Code 800 _H		4		Volts
DIGITAL INPUTS						
Input Logic High	V_{IH}	$V_{DD} = +5V$	2.4			V
Input Logic Low	V_{IL}	$V_{DD} = +5V$			0.8	V
Input Current	I_{IL}	$V_{IN} = 0V$ or $+5V$, $V_{DD} = +5V$			± 1	μA
Input Capacitance ²	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD} Range		4.5		5.5	V
Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or $V_{IL} = 0V$		2.5		mA
Supply Current in Shutdown	I_{DD_SHDN}	$V_{IH} = V_{DD}$ or $V_{IL} = 0V$, B14=0		40		μA
Power Dissipation ³	P_{DISS}	$V_{IH} = V_{DD}$ or $V_{IL} = 0V$, $V_{DD} = +5.5V$		12.5		mW
Power Supply Sensitivity	PSS	$\Delta V_{DD} = +5V \pm 10\%$		0.0002	0.01	%/%
DYNAMIC CHARACTERISTICS²						
Settling Time	t_S	0.1% error band		0.8		μs
INTERFACE TIMING CHARACTERISTICS^{2,4}						
SCLK Cycle Frequency	t_{CYC}				28	MHz
SCLK Clock Cycle time	t_1	Clock level low or high	35			ns
Input Clock Pulse Width	t_2, t_3		20			ns
Data Setup Time	t_4		5			ns
Data Hold Time	t_5		5			ns
FSYNC to SCLK active edge Setup Time	t_6		10			ns
SCLK to FSYNC Hold Time	t_7		0			ns
Minimum FSYNC High Time	t_8		35			ns

NOTES:

- Typicals represent average readings at $+25^\circ C$ and $V_{DD} = +5V$.
- Guaranteed by design and not subject to production test.
- P_{DISS} is calculated from $(I_{DD} \times V_{DD})$. CMOS logic level inputs result in minimum power dissipation.
- See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F = 2ns$ (10% to 90% of $+3V$) and timed from a voltage level of 1.5V. Switching characteristics are measured using $V_{DD} = +5V$. Input logic should have a $1V/\mu sec$ minimum slew rate.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V _{DD} to GND	-0.3,+6V
V _{OUTA} , V _{OUTB} , V _{BZ} to GND	0V, V _{DD}
Digital Input Voltages to GND	0V, V _{DD} +0.3V
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature (T _J MAX)	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Package Power Dissipation.....(T _J MAX - T _A) / θ _{JA}	
Thermal Resistance θ _{JA} , μSOIC-10	206°C/W

AD5399 Two's Complement Coding

Binary	Hexadecimal	Scale
0111 1111 1111	7 F F	+FS
0111 1111 1110	7 F F	+FS-1LSB
0000 0000 0001	0 0 1	BZS+1LSB
0000 0000 0000	0 0 0	BZS
1111 1111 1111	F F F	BZS-1LSB
1000 0000 0001	8 0 1	-FS+1LSB
1000 0000 0000	8 0 0	-FS

TABLE 2: AD5399 PIN Descriptions

Pin	Name	Description
1	SCLK	Serial Clock Input, positive edge triggered
2	SDA	Serial Data Input, MSB first format
3	DGND	Digital Ground
4	V _{OUTB}	DAC B Voltage Output (A0 = logic "1")
5	V _{OUTA}	DAC A Voltage Output (A0 = logic "0")
6	V _{BZ}	Virtual Bipolar Zero (Active Output)
7	AGND	Analog Ground
8	V _{DD}	Positive power supply, specified for operation at +5V.
9	V _{TRIM}	Connect to V _{DD}
10	FSYNC	Frame Sync Input, Active Low. When FSYNC returns HIGH data in the serial input register is transferred into the DAC register.

TABLE 1: AD5399 Serial-Data Word Format

ADDR		DATA									
B16	B15	B14	B13	B12	B11	<>	B4	B3	B2	B1	
A0	X	SD	0	D11	D10	<>	D3	D2	D1	D0	LSB
MSB											

SD: Shutdown is active high B14="1". Both DACs and the DACREF becomes open circuit.

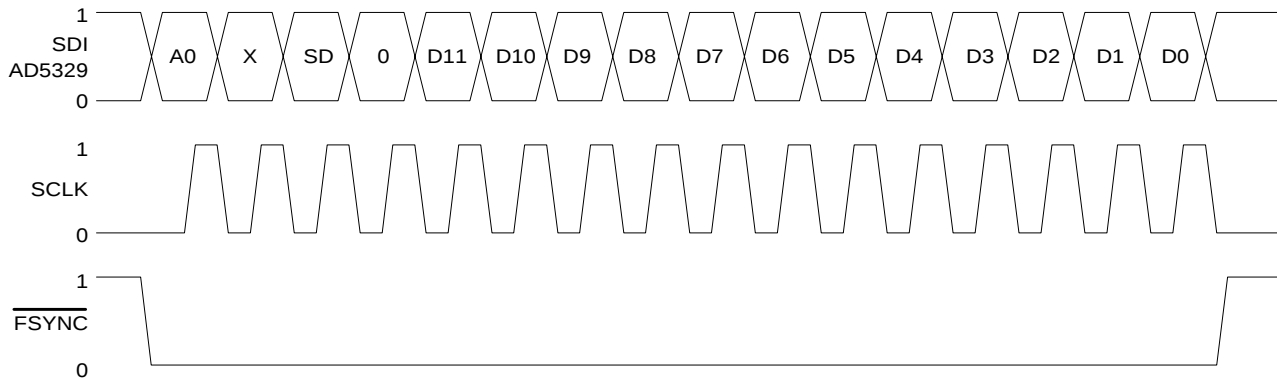


Figure 1A. Timing Diagram

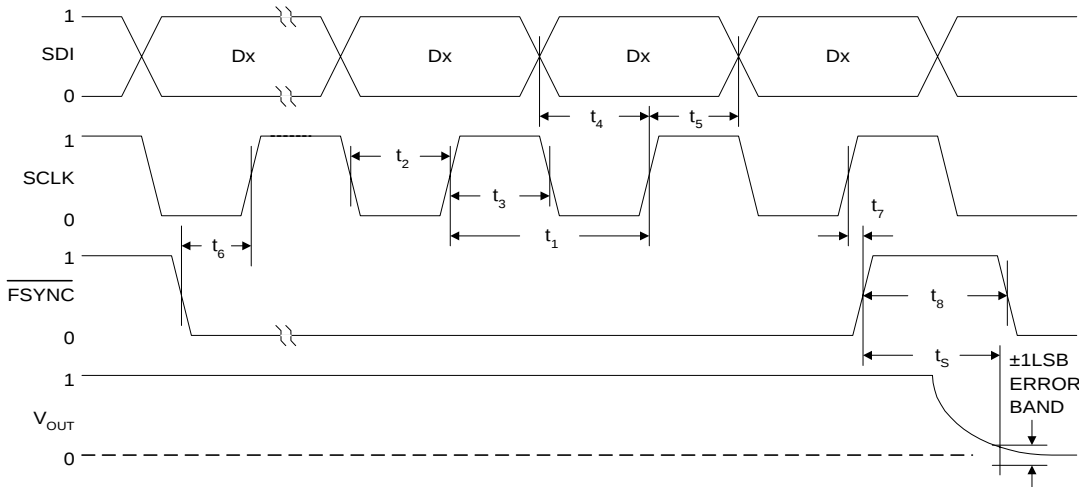
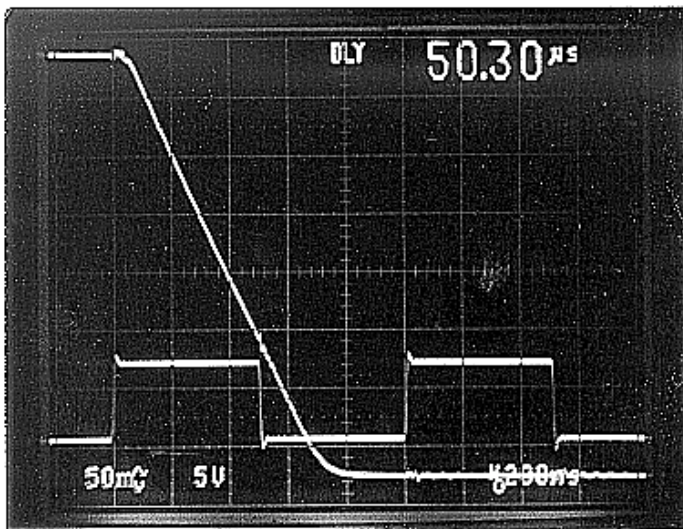
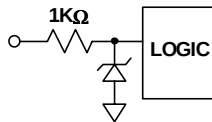


Figure 1B. Detail Timing Diagram

AD5399

All digital inputs are ESD protected with a series input resistor and parallel Zener as shown in figure 7. Applies to digital input pins SCLK, SDA, FSYNC



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