Quad, Parallel Input, Voltage Output, 12-/10-Bit Digital-to-Analog Converter

AD5582/AD5583

FEATURES

- 12-Bit Linearity and Monotonic AD5582
- 10-Bit Linearity and Monotonic AD5583
- Wide Operating Range: Single +5 V to +15 V or Dual ±5 V Supply
- Unipolar or Bipolar Operation
- Double Buffered Registers Enable Independent or Simultaneous Multichannel Update
- 4 Independent Rail-to-Rail Reference Inputs
- Parallel Interface
- Data Readback Capability
- 5 μs Settling Time
- Buffered Output
- Built-In Matching Resistor Simplifies Negative Reference
- Compact Footprint: TSSOP-48
- Extended Temperature Range: −40°C to +125°C

APPLICATIONS

- Process Control Equipment
- Closed-Loop Servo Control
- Data Acquisition Systems
- Digitally Controlled Calibration
- Motor Control
- Optical Network Control Loops

GENERAL DESCRIPTION

The AD5582/AD5583 family of quad, 12-/10-bit, voltage output digital-to-analog converters is designed to operate from a single +5 V to +15 V or dual ±5 V supply. Built using an advance BiCMOS process, this high performance DAC is cost effective and compact. It offers the user ease of use in single-or dual-supply systems.

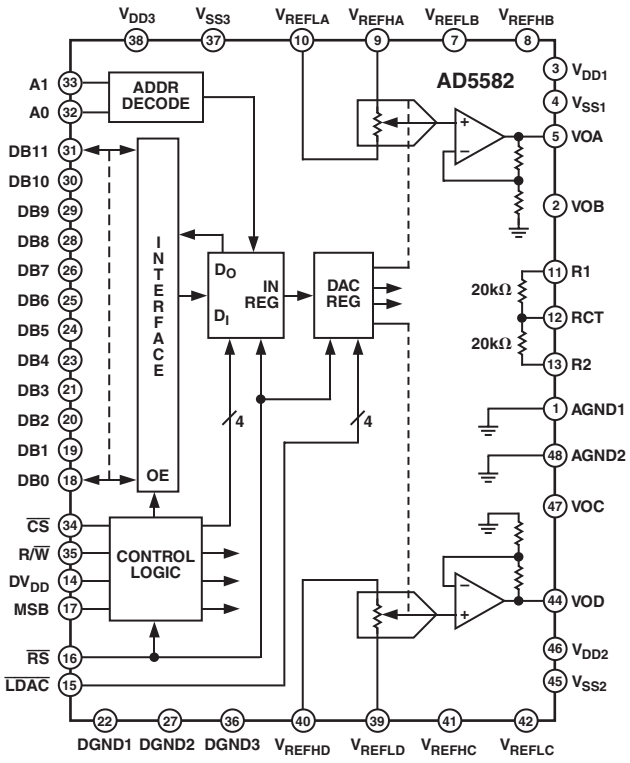
The applied external reference V_{REF} determines the full-scale output voltage. Valid V_{REF} values include $V_{SS} < V_{REF} < V_{DD}$ resulting in a wide selection of full-scale outputs. For multiplying and wide dynamic applications, ac reference inputs can be as high as $|V_{DD} - V_{SS}|$. Two built-in precision trimmed resistors are available and can be configured easily to provide four-quadrant multiplications.

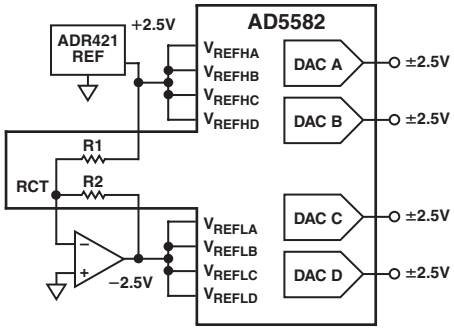
A doubled-buffered parallel interface offers 25 Mbps data load rates. A common level sensitive load DAC strobe ($\overline{LDAC}$) input allows simultaneous update of all DAC outputs from previously loaded input registers. An external asynchronous reset ($\overline{RS}$) forces all registers to the zero code state when MSB = 0 or to midscale when MSB = 1.

Both parts are offered in the same pinout to allow users to select the amount of resolution appropriate for their application without PCB layout changes.

REV. 0

FUNCTIONAL BLOCK DIAGRAM





DIGITAL CIRCUITRY OMITTED FOR CLARITY

Figure 1. Using Built-In Matching Resistors to Generate a Negative Voltage Reference

AD5582 is well suited for DAC8412 replacement in medium voltage applications in new designs.

The AD5582/AD5583 are specified over the extended industrial (–40°C to +125°C) temperature range and offered in a thin and compact 1.1 mm TSSOP-48 package.

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AD5582/AD5583–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5 V, V_{SS} = –5 V, DV_{DD} = +5 V ± 10%, V_{REFH} = +2.5 V, V_{REFL} = –2.5 V, –40°C < T_A < +125°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ[1]	Max	Unit
STATIC PERFORMANCE						
Resolution[2]	N	AD5582		12		Bits
		AD5583		10		Bits
Relative Accuracy[3]	INL		–1		+1	LSB
Differential Nonlinearity[3]	DNL	Monotonic	–1			LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H for AD5582 and AD5583	–2		+2	LSB
Gain Error	V_{GE}	Data = FFF_H for AD5582 and $3FF_H$ for AD5583	–2		+2	LSB
Gain Error	V_{GE}	V_{DD} = 2.7 V–4.5 V	–4		+4	LSB
Full-Scale Tempco[4]	TCV_{FS}			1.5		ppm/°C
REFERENCE INPUT						
V_{REFH} Input Range	V_{REFH}		V_{REFL} + 0.5		V_{DD}	V
V_{REFL} Input Range[5]	V_{REFL}		V_{SS}		V_{REFH} – 0.5	V
Input Resistance	R_{REF}	Data = 555_H (Minimum R_{REF}) for AD5582 and 155_H for AD5583	12	20		kΩ[1]
Input Capacitance[4]	C_{REF}			80		pF
REF Input Current	I_{REF}	Data = 555_H for AD5582			500	µA
REF Multiplying Bandwidth	BW_{REF}	Code = Full Scale			1.3	MHz
R1–R2 Matching	R1/R2	AD5582			±0.025	%
		AD5583			±0.100	%
ANALOG OUTPUT						
Output Current[6]	I_{OUT}	Data = 800_H for AD5582 and 200_H for AD5583, $\Delta V_{OUT} \le 4$ mV			±2	mA
Capacitive Load[4]	C_L	No Oscillation		2000		pF
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}	DV_{DD} = 5 V ± 10%			0.8	V
		DV_{DD} = 3 V ± 10%			0.4	V
Logic Input High Voltage	V_{IH}	DV_{DD} = 5 V ± 10%	2.4			V
		DV_{DD} = 3 V ± 10%	2.1			V
Input Leakage Current	I_{IL}			0.01	1	µA
Input Capacitance[4]	C_{IL}			5		pF
Output Voltage High	V_{OH}	I_{OH} = –0.8 mA	2.4			V
Output Voltage Low	V_{OL}	I_{OL} = 1.2 mA, T_A = 85°C			0.4	V
		I_{OL} = 0.6 mA, DV_{DD} = 3 V				
		I_{OL} = 1.0 mA, T_A = 125°C,			0.4	V
		I_{OL} = 0.5 mA, DV_{DD} = 3 V				
AC CHARACTERISTICS						
Output Slew Rate	SR	Data = Zero Scale to Full Scale to Zero Scale		2		V/µs
Settling Time[7]	t_S	To ±0.1% of Full Scale		5		µs
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$ for AD5582 and $1FF_H$ to 200_H to $1FF_H$ for AD5583		100		nVs
Digital Feedthrough	V_{OUT}/t_{CS}	Data = Midscale, $\overline{CS}$ Toggles at f = 16 MHz		5		nVs
Analog Crosstalk	V_{OUT}/V_{REF}	V_{REF} = 1.5 V dc + 1 V p-p, Data = 000_H, f = 100 kHz		–80		dB
Output Noise	e_N	f = 1 kHz		33		nV/√Hz

Parameter	Symbol	Condition	Min	Typ[1]	Max	Unit
SUPPLY CHARACTERISTICS						
Single-Supply Voltage Range	V_{DD}	V_{SS} = 0 V	3		18	V
Dual-Supply Voltage Range	V_{DD}/V_{SS}	V_{DD} = +2.7 V to +6.5 V, V_{SS} = –6.5 V to –2.7 V	–9		+9	V
Digital Logic Supply	DV_{DD}		2.7		8	V
Positive Supply Current[6]	I_{DD}	V_{IL} = 0 V, No Load		1.7	3	mA
Negative Supply Current	I_{SS}	V_{IL} = 0 V, No Load		1.5	3	mA
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load		16	30	mW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = ±5%		30		ppm/V

NOTES
[1]Typical specifications represent average readings measured at 25°C.
[2]DAC Output Equation: $V_{OUT} = V_{REFL} + [(V_{REFH} - V_{REFL}) \times D/2\text{^}N]$, where D = data loaded in corresponding DAC Register A, B, C, D, and N equals the number of bits; AD5582 = 12 bits, AD5583 = 10 bits. One LSB step voltage = $(V_{REFH} - V_{REFL})/4096$ V and $(V_{REFH} - V_{REFL})/1024$ V for AD5582 and AD5583, respectively.
[3]The first two codes (000_H, 001_H) of the AD5583 and the first four codes (000_H, 001_H, 002_H, 003_H) of the AD5582 are excluded from the linearity error measurement in single-supply operation.
[4]These parameters are guaranteed by design and not subject to production testing.
[5]Dual-supply operation, $V_{REFL} = V_{SS}$, exclude the lowest eight codes for the AD5582 and two codes for the AD5583 for INL and DNL errors.
[6]Short circuit output and supply currents are 24 mA and 25 mA, respectively.
[7]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground in single-supply operation.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_{DD} = +15 V, V_{SS} = 0 V, DV_{DD} = +5 V ± 10%, V_{REFH} = +10 V, V_{REFL} = 0 V, –40°C < T_A < +125°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ[1]	Max	Unit
STATIC PERFORMANCE						
Resolution[2]	N	AD5582		12		Bits
		AD5583		10		Bits
Relative Accuracy[3]	INL		–1		+1	LSB
Differential Nonlinearity[3]	DNL	Monotonic	–1			LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H for AD5582 and AD5583	–2		+2	LSB
Gain Error	V_{GE}	Data = FFF_H for AD5582 and $3FF_H$ for AD5583	–2		+2	LSB
Full-Scale Tempco[4]	TCV_{FS}			1.5		ppm/°C
REFERENCE INPUT						
V_{REFH} Input Range	V_{REFH}		V_{REFL} + 0.5		V_{DD}	V
V_{REFL} Input Range[5]	V_{REFL}		V_{SS}		V_{REFH} – 0.5	V
Input Resistance	R_{REF}	Data = 555_H (Minimum R_{REF}) for AD5582 and 155_H for AD5583	12	20		kΩ[1]
Input Capacitance[4]	C_{REF}			80		pF
REF Input Current	I_{REF}	Data = 555_H for AD5582			1000	µA
REF Multiplying Bandwidth	BW_{REF}	Code = Full Scale			1.3	MHz
R1–R2 Matching	R1/R2	AD5582			±0.025	%
		AD5583			±0.100	%
ANALOG OUTPUT						
Output Current[6]	I_{OUT}	Data = 800_H for AD5582 and 200_H for AD5583, $\Delta V_{OUT} \le 4$ mV			2	mA
Capacitive Load[4]	C_L	No Oscillation		2000		pF
LOGIC INPUTS/OUTPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
		DV_{DD} = 3 V ± 10%			0.4	V
Logic Input High Voltage	V_{IH}		2.4			V
		DV_{DD} = 3 V ± 10%	2.1			V
Input Leakage Current	I_{IL}					µA
Input Capacitance[4]	C_{IL}					pF
Output Voltage High	V_{OH}	I_{OH} = –0.8 mA	2.4			V
Output Voltage Low	V_{OL}	I_{OL} = 1.2 mA, T_A = 85°C			0.4	V
		I_{OL} = 0.6 mA, DV_{DD} = 3 V				
	V_{OL}	I_{OL} = 1.0 mA, T_A = 125°C			0.4	V
		I_{OL} = 0.5 mA, DV_{DD} = 3 V				

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Condition	Min	Typ[1]	Max	Unit
AC CHARACTERISTICS						
Output Slew Rate	SR	Data = Zero Scale to Full Scale to Zero Scale		2		V/µs
Settling Time[7]	t_S	To ±0.1% of Full Scale		14		µs
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$ for AD5582 and $1FF_H$ to 200_H to $1FF_H$ for AD5583		100		nVs
Digital Feedthrough	V_{OUT}/t_{CS}	Data = Midscale, $\overline{CS}$ Toggles at f = 16 MHz		5		nVs
Analog Crosstalk	V_{OUT}/V_{REF}	V_{REF} = 1.5 V dc + 1 V p-p, Data = 000_H, f = 100 kHz		–80		dB
Output Noise	e_N	f = 1 kHz		33		nV/√Hz
SUPPLY CHARACTERISTICS						
Single-Supply Voltage Range	V_{DD}	V_{SS} = 0 V	3		16.5	V
Dual-Supply Voltage Range	V_{DD}/V_{SS}	V_{DD} = +2.7 V to +6.5 V, V_{SS} = –6.5 V to –2.7 V	–6.5		+6.5	V
Digital Logic Supply	DV_{DD}		2.7		6.5	V
Positive Supply Current[6]	I_{DD}	V_{IL} = 0 V, No Load		2.3	3.5	mA
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load		34.5	52.5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		30		ppm/V

NOTES

[1]Typical specifications represent average readings measured at 25°C.

[2]DAC Output Equation: $V_{OUT} = V_{REFL} + [(V_{REFH} - V_{REFL}) \times D/2\text{^}N]$, where D = data in decimal loaded in corresponding DAC Register A, B, C, D, and N equals the number of bits; AD5582 = 12 bits, AD5583 = 10 bits. One LSB step voltage = $(V_{REFH} - V_{REFL})/4096$ V and = $(V_{REFH} - V_{REFL})/1024$ V for AD5582 and AD5583, respectively.

[3]The first two codes (000_H, 001_H) of the AD5583 and the first four codes (000_H, 001_H, 002_H, 003_H) of the AD5582 are excluded from the linearity error measurement in single-supply operation.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]Dual-supply operation, $V_{REFL} = V_{SS}$, exclude the lowest eight codes for the AD5582 and two codes for the AD5583 for INL and DNL errors.

[6]Short circuit output and supply currents are 24 mA and 25 mA, respectively.

[7]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground in single-supply operation.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = 15 V or 5 V, V_{SS} = 0 V, DV_{DD} = 5 V ± 10%, V_{REFH} = 10 V, V_{REFL} = 0 V, –40°C < T_A < +125°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INTERFACE TIMING*						
Clock Frequency	f_{CLK}				25	MHz
Chip Select Write Pulsewidth	t_{WCS}		20			ns
Chip Select Read Pulsewidth	t_{RCS}		130			ns
Write Setup	t_{WS}		0			ns
Write Hold	t_{WH}		0			ns
Address Setup	t_{AS}		0			ns
Address Hold	t_{AH}		0			ns
Load Setup	t_{LS}		0			ns
Load Hold	t_{LH}		0			ns
Write Data Setup	t_{WDS}		0			ns
Write Data Hold	t_{WDH}		0			ns
Load Data Pulsewidth	t_{LDW}		20			ns
Reset Pulsewidth	t_{RESET}		20			ns
Read Data Hold	t_{RDH}		0			ns
Read Data Setup	t_{RDS}		0			ns
Data to Hi-Z	t_{DZ}	C_L = 10 pF			100	ns
Chip Select to Data	t_{CSD}	C_L = 10 pF			100	ns
Chip Select Repetitive Pulsewidth	t_{CSP}		10			ns
Load Setup in Double Buffer Mode	t_{LDS}		20			ns
Load Data Hold	t_{LDH}		0			ns

*All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = 15 V or 5 V, V_{SS} = 0 V, DV_{DD} = 3 V ± 10%, V_{REFH} = 10 V, V_{REFL} = 0 V, –40°C < T_A < +125°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INTERFACE TIMING*						
Clock Frequency	f_{CLK}				14	MHz
Chip Select Write Pulsewidth	t_{WCS}		35			ns
Chip Select Read Pulsewidth	t_{RCS}		130			ns
Write Setup	t_{WS}		0			ns
Write Hold	t_{WH}		0			ns
Address Setup	t_{AS}		0			ns
Address Hold	t_{AH}		0			ns
Load Setup	t_{LS}		0			ns
Load Hold	t_{LH}		0			ns
Write Data Setup	t_{WDS}		0			ns
Write Data Hold	t_{WDH}		0			ns
Load Data Pulsewidth	t_{LDW}		35			ns
Reset Pulsewidth	t_{RESET}		35			ns
Read Data Hold	t_{RDH}		0			ns
Read Data Setup	t_{RDS}		0			ns
Data to Hi-Z	t_{DZ}	C_L = 10 pF	80		100	ns
Chip Select to Data	t_{CSD}	C_L = 10 pF	80		100	ns
Chip Select Repetitive Pulsewidth	t_{CSP}		20			ns
Load Setup in Double Buffer Mode	t_{LDS}		35			ns
Load Data Hold	t_{LDH}		0			ns

*All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to V_{SS} . . . . . –0.3 V to +18 V
V_{DD} to GND . . . . . –0.3 V to +18 V
V_{SS} to GND . . . . . +0.3 V to –9 V
V_{DD} to V_{REF+} . . . . . –0.3 V to (V_{DD} – V_{SS})
V_{REF-} to V_{SS} . . . . . –0.3 V to (V_{DD} – V_{SS})
V_{REFH} to V_{REFL} . . . . . –0.3 V to (V_{DD} – V_{SS})
DV_{DD} to GND . . . . . 8 V
Logic Inputs to GND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
V_{OUT} to GND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND . . . . . 24 mA
Thermal Resistance Junction to Ambient, θ_{JA} . . . . . 115°C/W
Thermal Resistance Junction to Case, θ_{JC} . . . . . 42°C/W
Maximum Junction Temperature (T_J Max) . . . . . 150°C
Package Power Dissipation = (T_J Max – T_A)/θ_{JA}
Operating Temperature Range . . . . . –40°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature
RV-48 (Soldering, 60 secs) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE*

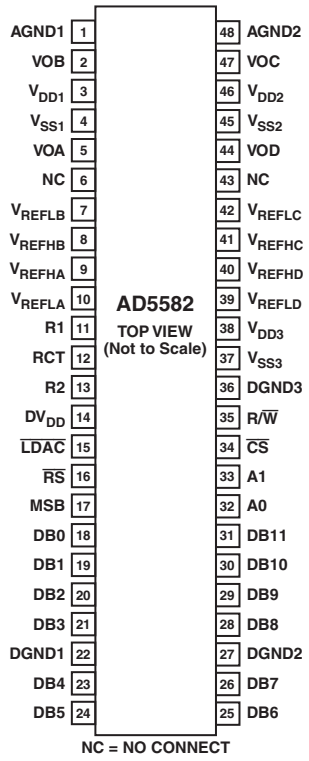
Model	Resolution (Bits)	Temperature Range	Package Description	Package Option	Container Quantity	Top Marking
AD5582YRV-REEL	12	–40°C to +125°C	TSSOP-48	RV-48	2500	AD5582Y
AD5583YRV-REEL	10	–40°C to +125°C	TSSOP-48	RV-48	2500	AD5583Y
AD5582YRV	12	–40°C to +125°C	TSSOP-48	RV-48	39	AD5582Y
AD5583YRV	10	–40°C to +125°C	TSSOP-48	RV-48	39	AD5583Y

*The AD5582 contains 4116 transistors. The die size measures 108 mil × 144 mil.
First row marking is shown in the table above. Second row marking contains date code in YYWW format. Third row marking contains the lot number.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5582/AD5583 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD5582 PIN CONFIGURATION

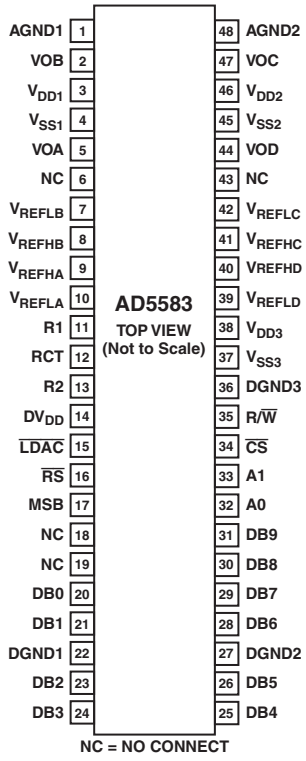


AD5582 PIN FUNCTION DESCRIPTIONS*

Pin No.	Mnemonic	Description
1	AGND1	Analog Ground for DAC A and B
2	VOB	DAC B Output
3	V_{DD1}	Positive Power Supply for DAC A and B
4	V_{SS1}	Negative Power Supply for DAC A and B
5	VOA	DAC A Output
6	NC	No Connect
7	V_{REFLB}	DAC B Voltage Reference Low Terminal
8	V_{REFHB}	DAC B Voltage Reference High Terminal
9	V_{REFHA}	DAC A Voltage Reference High Terminal
10	V_{REFLA}	DAC A Voltage Reference Low Terminal
11	R1	R1 Terminal (for Negative Reference)
12	RCT	Center Tap Terminal (for Negative Reference)
13	R2	R2 Terminal (for Negative Reference)
14	DV_{DD}	Power Supply for Digital Circuits
15	$\overline{LDAC}$	DAC Register Load, Active Low Level Sensitive
16	$\overline{RS}$	Reset Strobe
17	MSB	MSB = 0, Reset to 000_H, MSB = 1, Reset to 800_H
18	DB0	Data Bit 0
19	DB1	Data Bit 1
20	DB2	Data Bit 2
21	DB3	Data Bit 3
22	DGND1	Digital Ground 1
23	DB4	Data Bit 4
24	DB5	Data Bit 5
25	DB6	Data Bit 6
26	DB7	Data Bit 7
27	DGND2	Digital Ground 2
28	DB8	Data Bit 8
29	DB9	Data Bit 9
30	DB10	Data Bit 10
31	DB11	Data Bit 11
32	A0	Address Input 0
33	A1	Address Input 1
34	$\overline{CS}$	Chip Select, Active Low
35	R/$\overline{W}$	Read/Write Mode Select
36	DGND3	Digital Ground 3
37	V_{SS3}	Negative Power Supply for Analog Switches
38	V_{DD3}	Positive Power Supply for Analog Switches
39	V_{REFLD}	DAC D Voltage Reference Low Terminal
40	V_{REFHD}	DAC D Voltage Reference High Terminal
41	V_{REFHC}	DAC C Voltage Reference High Terminal
42	V_{REFLC}	DAC C Voltage Reference Low Terminal
43	NC	No Connect
44	VOD	DAC D Output
45	V_{SS2}	Negative Power Supply for DAC C and D
46	V_{DD2}	Positive Power Supply for DAC C and D
47	VOC	DAC C Output
48	AGND2	Analog Ground for DAC C and D

*AD5582 optimizes internal layout design to reduce die area so that all supply voltage pins are required to be connected externally. See Figure 5.

AD5583 PIN CONFIGURATION



AD5583 PIN FUNCTION DESCRIPTIONS*

Pin No.	Mnemonic	Description
1	AGND1	Analog Ground for DAC A and B
2	VOB	DAC B Output
3	V_{DD1}	Positive Power Supply for DAC A and B
4	V_{SS1}	Negative Power Supply for DAC A and B
5	VOA	DAC A Output
6	NC	No Connect
7	V_{REFLB}	DAC B Voltage Reference Low Terminal
8	V_{REFHB}	DAC B Voltage Reference High Terminal
9	V_{REFHA}	DAC A Voltage Reference High Terminal
10	V_{REFLA}	DAC A Voltage Reference Low Terminal
11	R1	R1 Terminal (for Negative Reference)
12	RCT	Center Tap Terminal (for Negative Reference)
13	R2	R2 Terminal (for Negative Reference)
14	DV_{DD}	Power Supply for Digital Circuits
15	$\overline{LDAC}$	DAC Register Load, Active Low Level Sensitive
16	$\overline{RS}$	Reset Strobe
17	MSB	MSB = 0, Reset to 000_H, MSB = 1, Reset to 200_H
18	NS	No Connection
19	NS	No Connection
20	DB0	Data Bit 0
21	DB1	Data Bit 1
22	DGND1	Digital Ground 1
23	DB2	Data Bit 2
24	DB3	Data Bit 3
25	DB4	Data Bit 4
26	DB5	Data Bit 5
27	DGND2	Digital Ground 2
28	DB6	Data Bit 6
29	DB7	Data Bit 7
30	DB8	Data Bit 8
31	DB9	Data Bit 9
32	A0	Address Input 0
33	A1	Address Input 1
34	$\overline{CS}$	Chip Select, Active Low
35	R/$\overline{W}$	Read/Write Mode Select
36	DGND3	Digital Ground 3
37	V_{SS3}	Negative Power Supply for Analog Switches
38	V_{DD3}	Positive Power Supply for Analog Switches
39	V_{REFLD}	DAC D Voltage Reference Low Terminal
40	V_{REFHD}	DAC D Voltage Reference High Terminal
41	V_{REFHC}	DAC C Voltage Reference High Terminal
42	V_{REFLC}	DAC C Voltage Reference Low Terminal
43	NC	No Connect
44	VOD	DAC D Output
45	V_{SS2}	Negative Power Supply for DAC C and D
46	V_{DD2}	Positive Power Supply for DAC C and D
47	VOC	DAC C Output
48	AGND2	Analog Ground for DAC C and D

*AD5583 optimizes internal layout design to reduce die area so that all supply voltage pins are required to be connected externally. See Figure 5.

TIMING DIAGRAMS

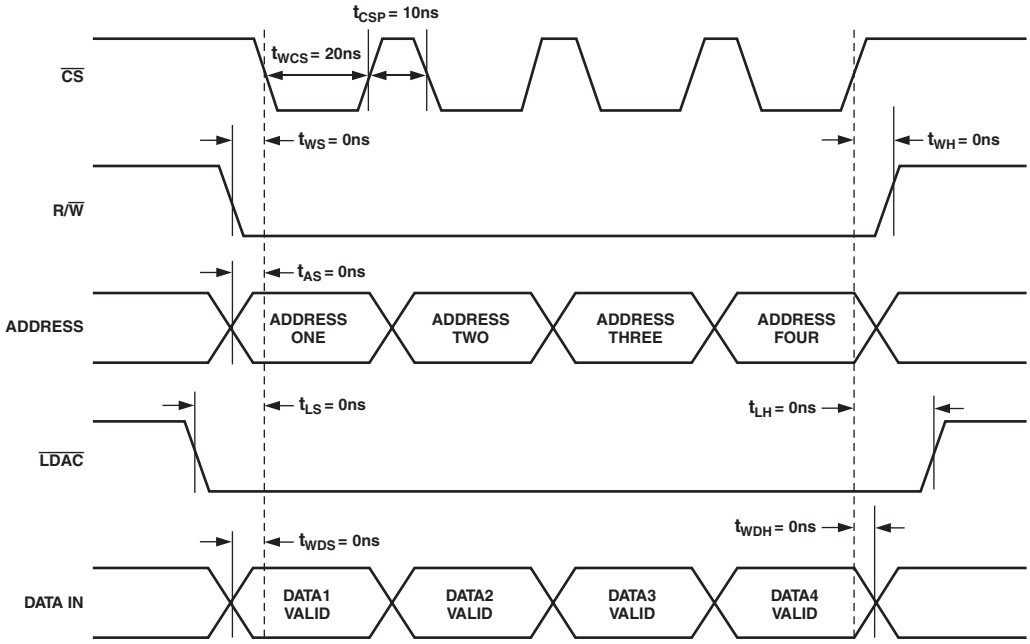


Figure 2a. Single Buffer Mode, Output Updated Individually, DV_{DD} = 5 V

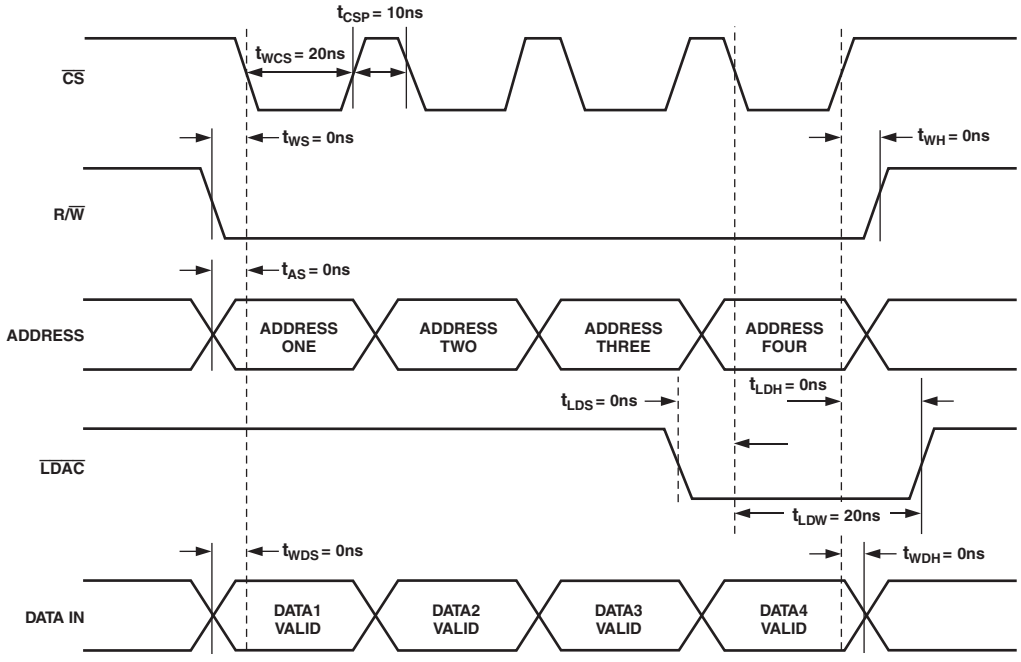


Figure 2b. Double Buffer Mode, Output Updated Simultaneously, DV_{DD} = 5 V

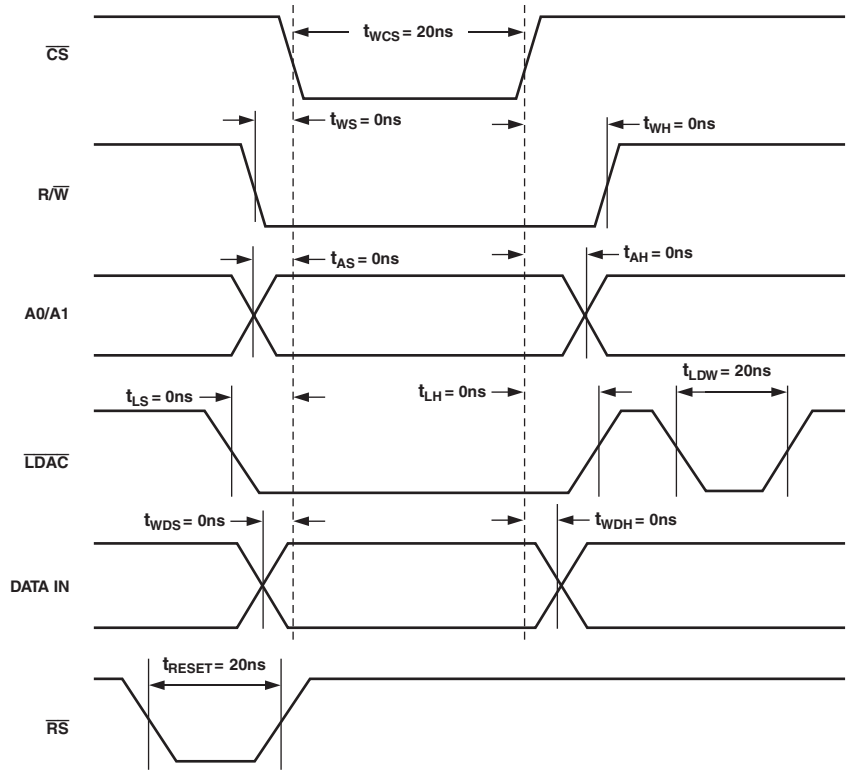


Figure 2c. Data Write (Input and Output Registers) Timing

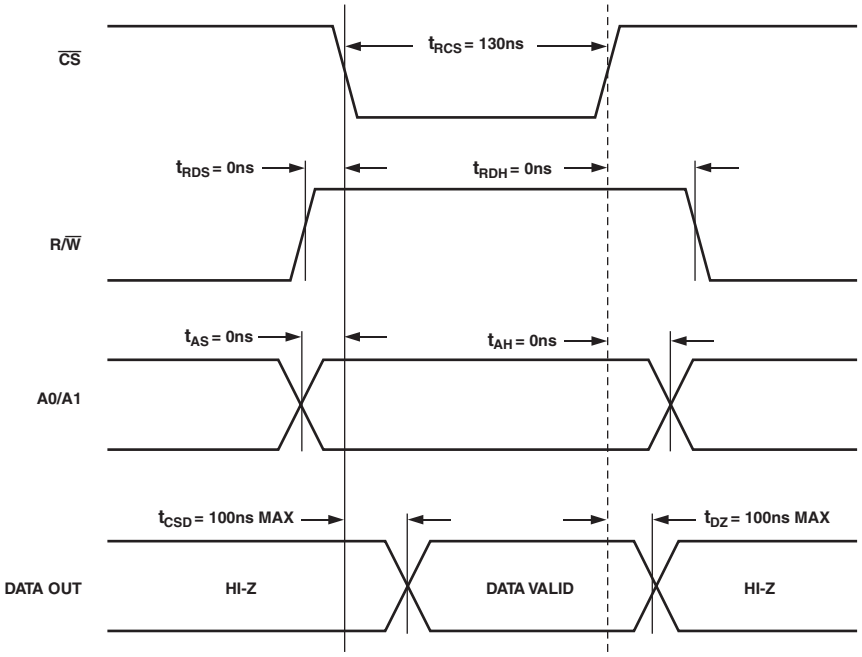
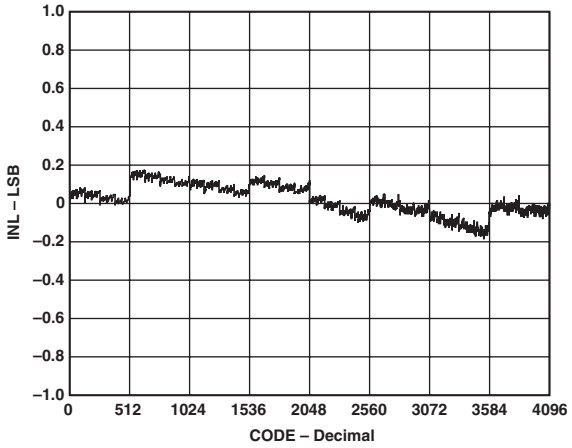
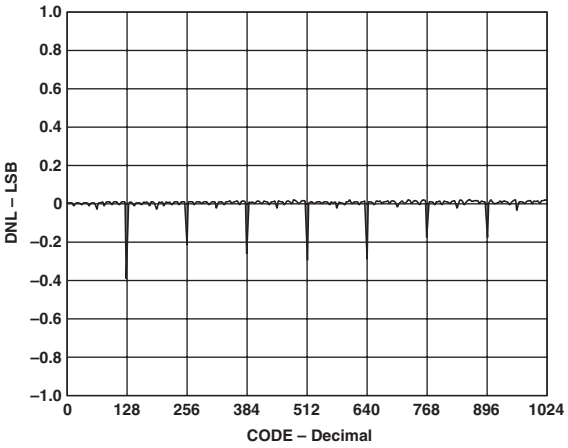


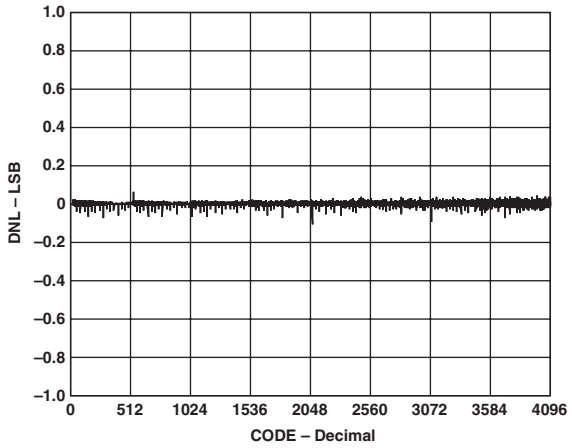
Figure 2d. Data Output (Read Timing)



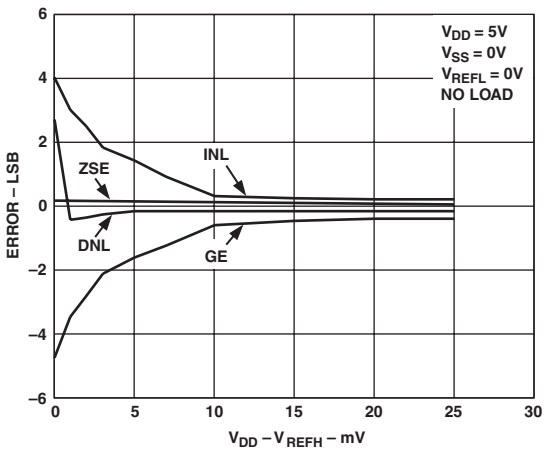
TPC 1. AD5582 Integral Nonlinearity Error



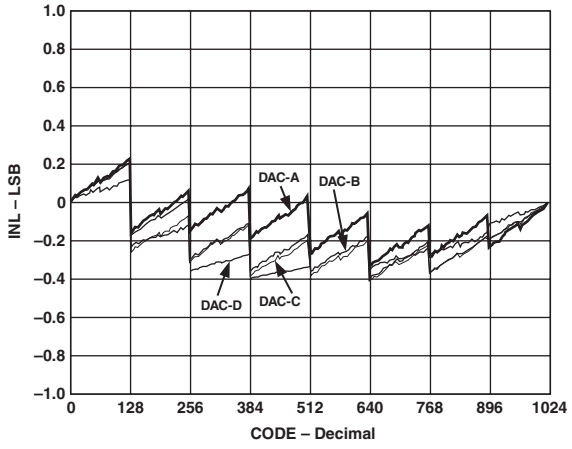
TPC 4. AD5583 Differential Nonlinearity Error



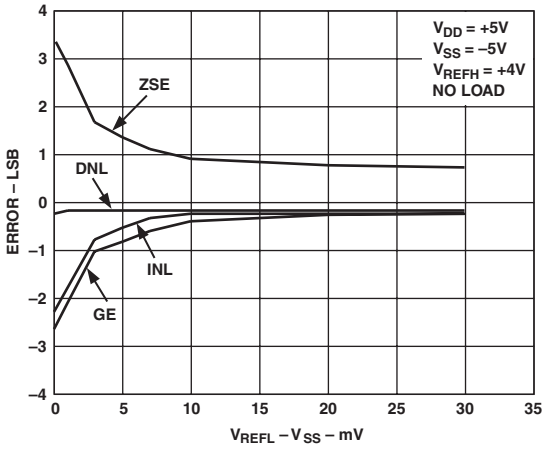
TPC 2. AD5582 Differential Nonlinearity Error



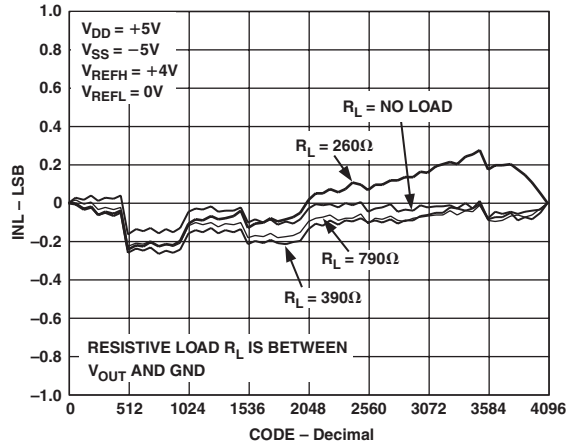
TPC 5. AD5582 INL, DNL, ZSE, and GE at Positive Rail-to-Rail Operation



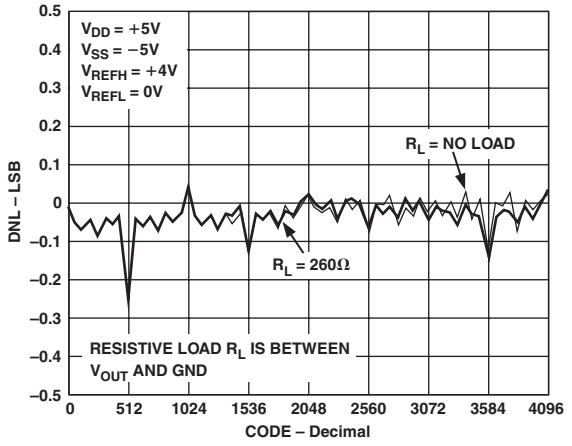
TPC 3. AD5583 Integral Nonlinearity Error



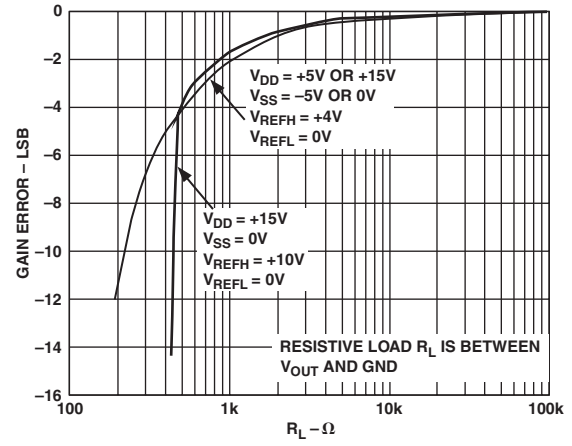
TPC 6. AD5582 INL, DNL, GE, and ZSE at Negative Rail-to-Rail Operation



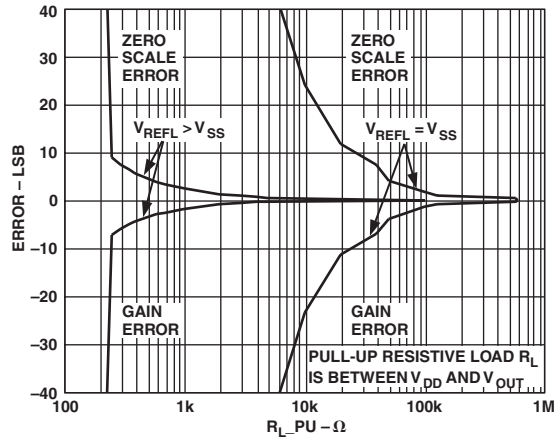
TPC 7. AD5582 INL at Various Resistive Loads



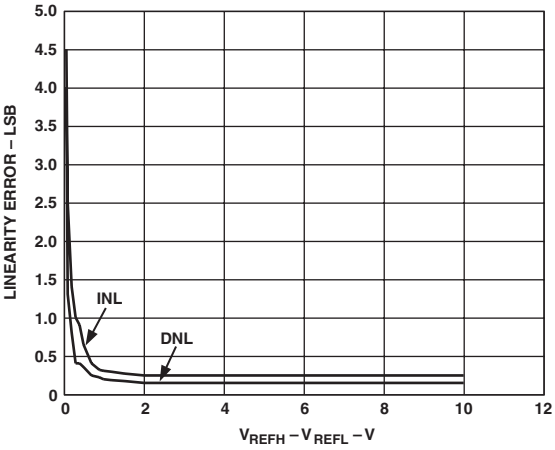
TPC 8. AD5582 DNL at Various Resistive Loads



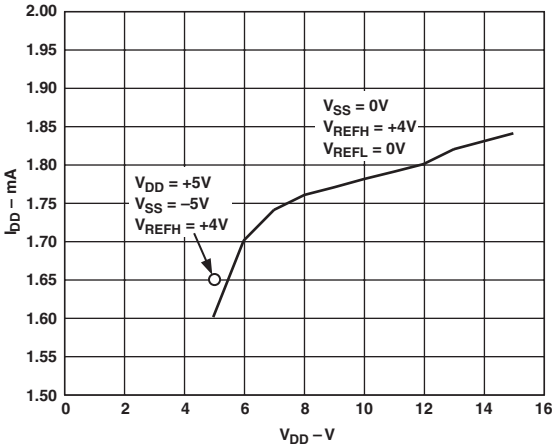
TPC 9. AD5582 Gain Error vs. Resistive Load



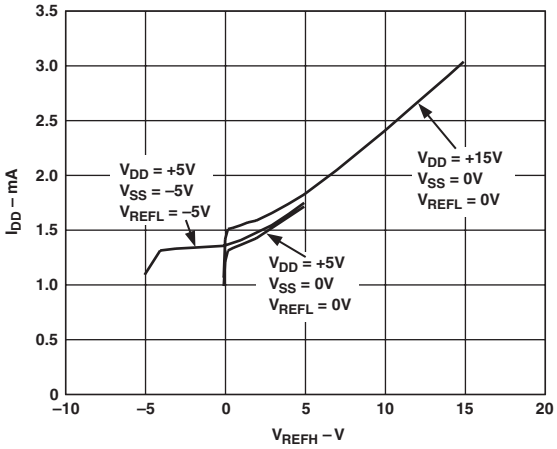
TPC 10. AD5582 Gain and Zero-Scale Error vs. Pull-Up Resistive Loads



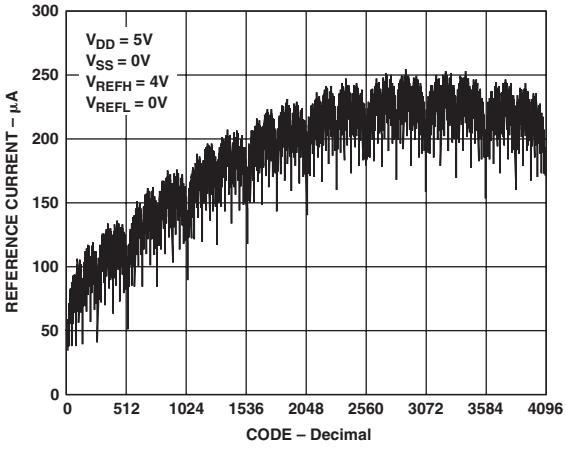
TPC 11. AD5582 Linearity Errors vs. Differential Reference Ranges



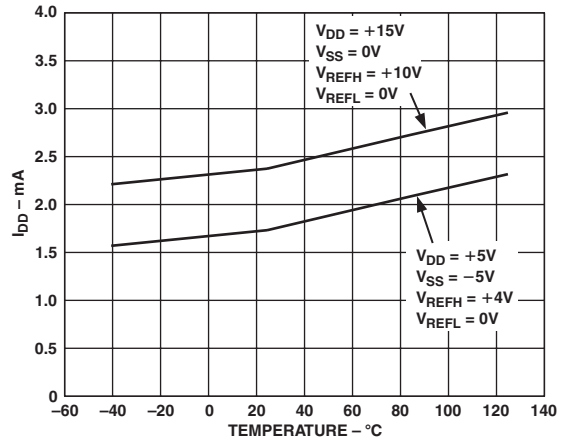
TPC 12. AD5582 Supply Current vs. Supply Voltage



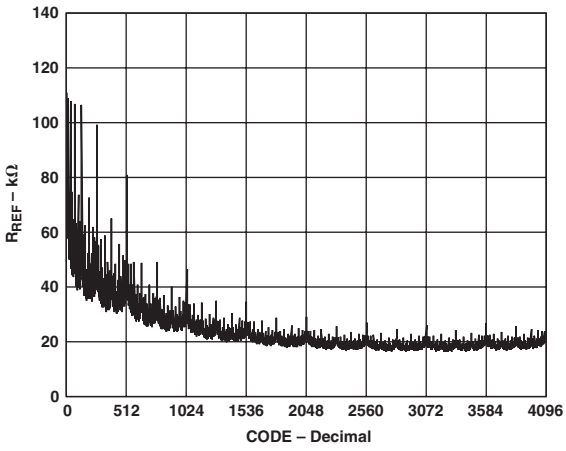
TPC 13. AD5582 Supply Current vs. Reference Voltage



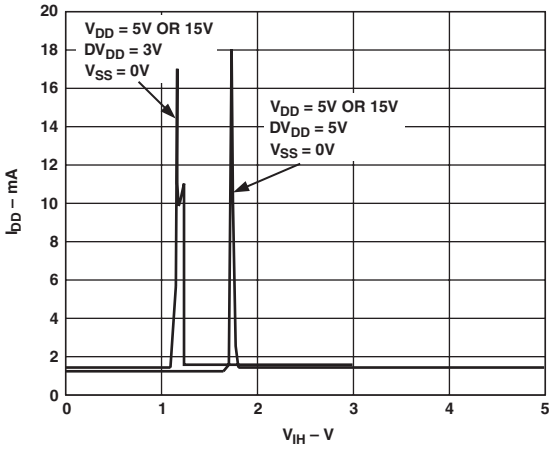
TPC 16. AD5582 Reference Current



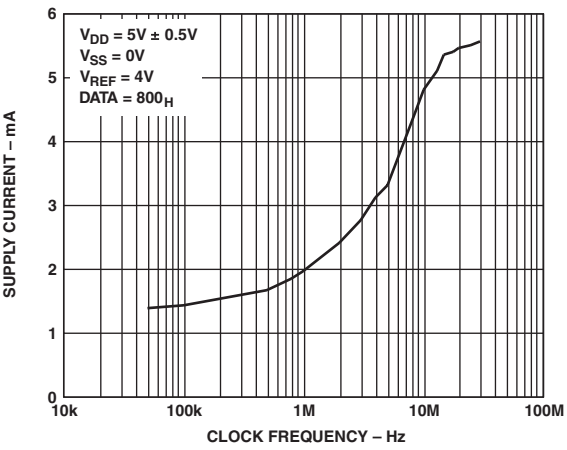
TPC 14. AD5582 Supply Current vs. Temperature



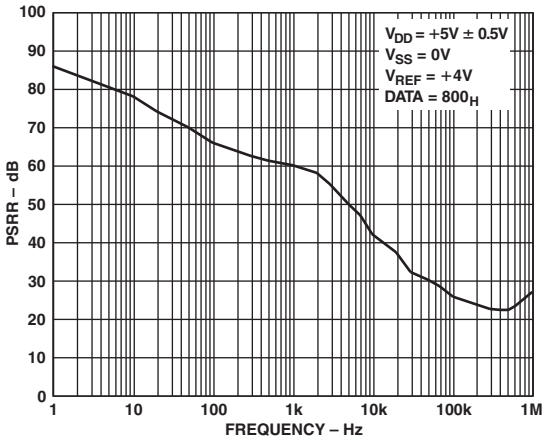
TPC 17. AD5582 Referenced Input Resistance



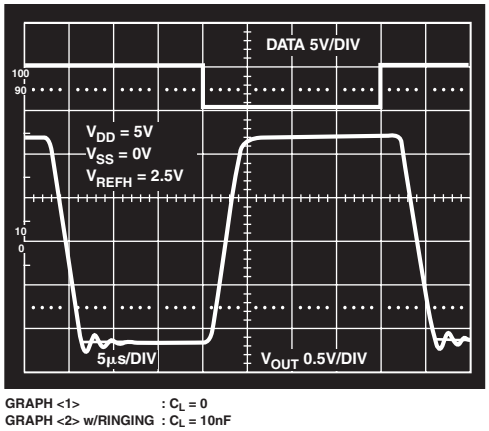
TPC 15. AD5582 Supply Current vs. Logic Input Voltage



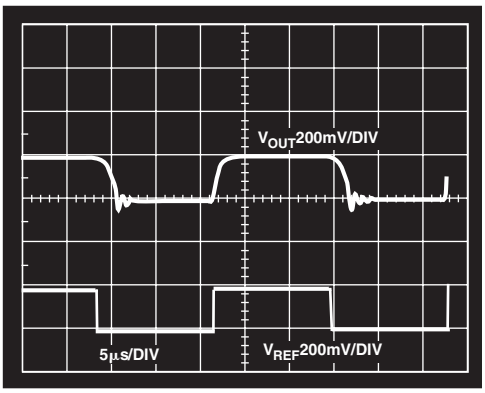
TPC 18. AD5582 Supply Current vs. Clock Frequency



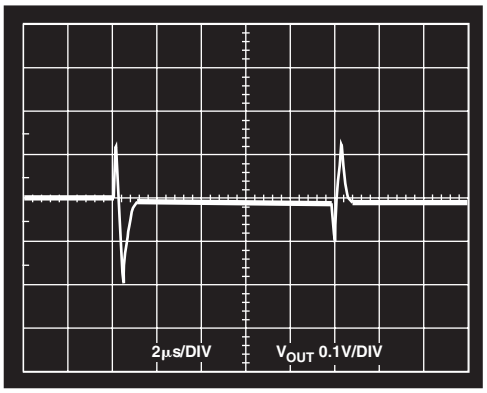
TPC 19. AD5582 PSRR vs. Frequency



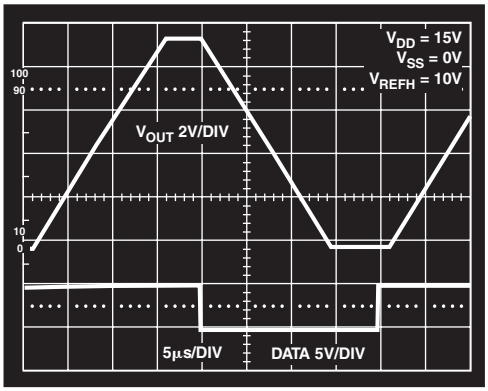
TPC 22. Large Signal Settling When Loaded (See Test Circuit 1)



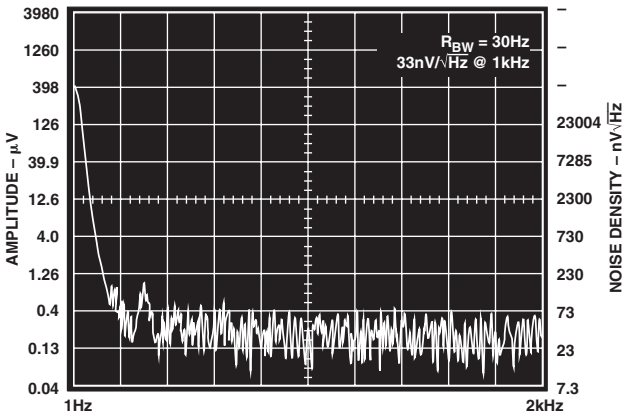
TPC 20. Small Signal Response Operating at Near Rail, C_L = 2 nF (See Test Circuit 1)



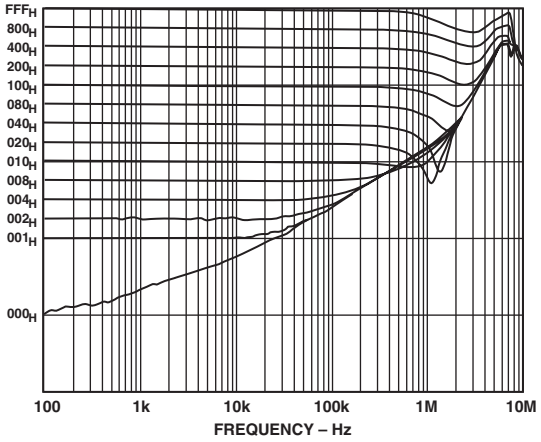
TPC 23. Midscale Transition Glitch



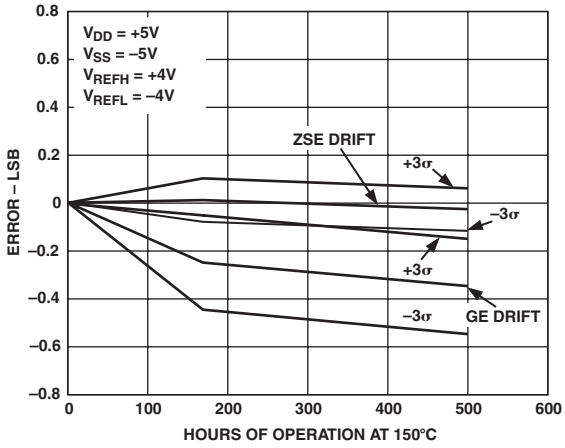
TPC 21. Large Signal Settling



TPC 24. AD5582 Output Noise Density

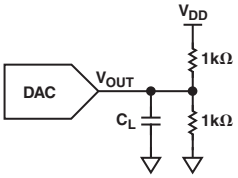


TPC 25. AD5582 Multiplying Bandwidth



TPC 26. AD5582 Long-Term Drift

Test Circuit



Test Circuit 1

THEORY OF OPERATION

The AD5582/AD5583 are quad, voltage output, 12-/10-bit parallel input DACs in compact TSSOP-48 packages.

Each DAC is a voltage switch, high impedance (R = 20 kΩ), R-2R ladder configuration with segmentation to optimize die area and precision. Figure 3 shows a simplified R-2R structure without showing the detailed segmentation. The 2R resistances are switched between V_{REFH} and V_{REFL}, and the output is obtained from the rightmost ladder node. As the code is sequenced through all possible states, the voltage of this node changes in steps of (2/3 V_{REFH} – V_{REFL})/(2^N – 1) starting from the lowest V_{REFL} and going to the highest V_{REFH} – DUTLSB. Buffering it with an amplifier with a gain of 1.5 brings the output to:

$$V_{OUT} = \frac{D}{2^N - 1}\left(V_{REFH} - V_{REFL}\right) + \left(V_{REFL}\right) \quad (1)$$

where D is the decimal equivalent of the data bits and N is the numbers of bits.

If V_{REFL} is equal to V_{REFH} as V_{REF}, V_{OUT} is simplified to:

$$V_{OUT} = \left(\frac{D}{2047} - 1\right)V_{REF} \quad \text{(For AD5582) (2)}$$

$$V_{OUT} = \left(\frac{D}{511} - 1\right)V_{REF} \quad \text{(For AD5583) (3)}$$

The advantage of this scheme is that it allows the DAC to interpolate between two voltages for differential references or single-ended references.

These DACs feature double buffers, which allow both synchronous and asynchronous channels to update with additional data readback capability. These parts can be reset to zero scale or midscale controlled by the $\overline{RS}$ and MSB pins. When $\overline{RS}$ is activated, MSB of 0 resets the DACs to zero scale and MSB of 1 resets the DACs to midscale. The ability to operate from wide supply voltages, +5 V to +15 V or ±5 V, with multiplying bipolar references is another key feature of these DACs.

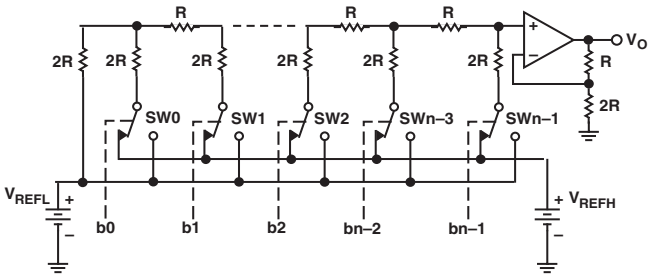


Figure 3. Simplified R-2R Architecture (Segmentation Not Shown)

Power Supplies

There are three separate power supplies needed for the operation of the DACs. For dual supply, V_{SS} can be set between –6.5 V to –2.7 V and V_{DD} can be set between +2.7 V to +6.5 V. For single supply, V_{SS} should be set at 0 V while V_{DD} is set between 3 V to 16.5 V. However, setting the single supply of V_{DD} below 4.5 V can impact the overall accuracy of the device.

Since these DACs can be operated at high voltages, the digital signal levels are therefore controlled separately by the provision of DV_{DD}. DV_{DD} can be set as low as 2.7 V but no more than 6.5 V. This allows the DAC to be operable from low level digital signals generated from a wide range of microcontrollers, FPGA, and signal processors.

Reference Input

All four channels of DACs allow independent and differential reference voltages. The flexibility of independent references allows users to apply a unique reference voltage to each channel. Similarly, bipolar references can be applied across the differential references. To maintain optimum accuracy, the difference between V_{REFH} and V_{REFL} should be greater than 1 V. See TPC 11.

The voltages applied to these reference inputs set the output voltage limits of all four channels of the DACs, and V_{REFH} must always be higher than V_{REFL}. V_{REFH} can be set at any voltage from V_{REFL} + 0.5 V to V_{DD}, while V_{REFL} can be set at any voltage from V_{SS} to V_{REFH} – 0.5 V. In addition, a symmetrical negative reference can be generated easily by an external op amp in an inverting mode with a pair of built-in precision resistors, R1 and R2. These resistors are matched within ±0.025% for AD5582 and 0.1% for AD5583, which is equivalent to less than one LSB mismatch. Figure 3 shows a simple configuration.

Common reference or references can be applied to all four channels, but each reference pin should be decoupled with a 0.1 μF ceramic capacitor mounted close to the pin.

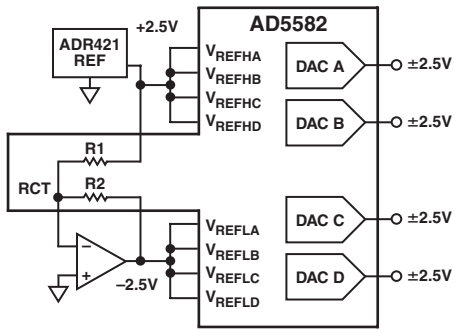


Figure 4. Using On-Board Matching Resistors to Generate a Negative Voltage REF

Digital I/O

Digital I/O consists of a 12-/10-bit bidirectional data bus, two register select inputs, A0 and A1, an R/$\overline{W}$ input, a Reset ($\overline{RS}$), a Chip Select ($\overline{CS}$), and a Load DAC ($\overline{LDAC}$) input. Control of the DACs and the bus direction is determined by these inputs as shown in Table I. All digital pins are TTL/CMOS compatible and all internal registers are level triggered.

The register selects inputs A0 and A1. Decoding of the registers is enabled by the $\overline{CS}$ input. When $\overline{CS}$ is high, no decoding is taking place and neither the writing nor the reading of the input registers is enabled. The loading of the second bank of registers is controlled by the asynchronous $\overline{LDAC}$ input. By taking $\overline{LDAC}$ low while $\overline{CS}$ is enabled, the individual channel is updated as Single Buffer Mode, Figure 2a. If $\overline{CS}$ is enabled sequentially to load data into all input registers, then a subsequent $\overline{LDAC}$ pulse will allow all channels to be updated simultaneously as Double Buffer Mode, Figure 2b.

R/$\overline{W}$ controls the writing to and reading from the input register.

Reset

The $\overline{RS}$ function can be used either at power-up or at any time during operation. The $\overline{RS}$ function has priority over any other digital inputs. This pin is active low and sets the DAC output registers to either zero scale or midscale, determined by the state of MSB. The reset to midscale is useful when the DAC is configured for bipolar references and the output will be reset to 0 V.

Output Amplifiers

Unlike many voltage output DACs, the AD5582/AD5583 feature buffered voltage outputs. Each output is capable of both sourcing and sinking ±2 mA, eliminating the need for external buffers when driving capacitive loads as large as 500 pF without oscillation. These amplifiers also have short circuit protection.

Glitch

AD5582/AD5583 are designed specifically to minimize glitch performance. For example, the worst-case glitch of AD5582 occurs at the transitions between midscale (1000 0000 0000B) to midscale minus 1 (0111 1111 1111B), or vice versa. The glitch energy is measured as 100 mV × 1 μs or equivalent to 100 nVs. Such glitch occurs in a shorter duration than the settling time and therefore most applications will be immune to such an effect without a deglitcher.

Layout and Power Supply Bypassing

It is a good practice to employ compact, minimum-lead length PCB layout design. The leads to the input should be as short as possible to minimize IR drop and stray inductance.

It is also essential to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 μF to 0.1 μF disc or chip ceramics capacitors. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance. AD5582/AD5583 optimize internal layout design to reduce die area so that all analog supply pins are required to be connected externally. See Figure 5.

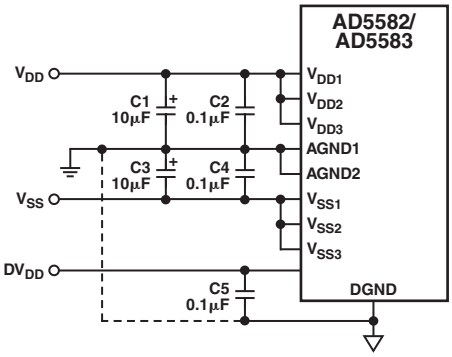


Figure 5. Power Supply Configurations

APPLICATIONS

Programmable Current Source

Figure 6 shows a versatile V-I conversion circuit using an improved Howland Current Pump. In addition to the precision current conversion it provides, this circuit enables a bidirectional current flow and high voltage compliance. The voltage compliance is mainly limited by the op amp supply voltages. This circuit can be used in 4 to 20 mA current transmitters with up to 500 Ω of load.

Table I. AD5582/AD5583 Logic Table

A1	A0	R/$\overline{W}$	$\overline{CS}$	$\overline{LDAC}$	$\overline{RS}$	INPUT REGISTER	DAC REGISTER	OPERATION MODE	SELECTED DAC
0	0	0	0	0	1	Write	Transparent	Transparent	A
0	1	0	0	0	1	Write	Transparent	Transparent	B
1	0	0	0	0	1	Write	Transparent	Transparent	C
1	1	0	0	0	1	Write	Transparent	Transparent	D
0	0	0	0	1	1	Write	Hold	Write Input	A
0	1	0	0	1	1	Write	Hold	Write Input	B
1	0	0	0	1	1	Write	Hold	Write Input	C
1	1	0	0	1	1	Write	Hold	Write Input	D
0	0	1	0	1	1	Read	Hold	Readback to D0 to DN	A
0	1	1	0	1	1	Read	Hold	Readback to D0 to DN	B
1	0	1	0	1	1	Read	Hold	Readback to D0 to DN	C
1	1	1	0	1	1	Read	Hold	Readback to D0 to DN	D
X	X	X	1	0	1	Hold	Update All Registers	Update All Registers	All
X	X	X	1	1	1	Hold	Hold	Hold	All
X	X	X	X	X	0	All registers reset to midscale or zero scale.			All
X	X	X	1	X	↑	All registers latched to midscale or zero scale.			All

MSB = 0 resets to zero scale, MSB = 1 resets to midscale. X: Don't Care. Input and output registers are transparent when asserted.

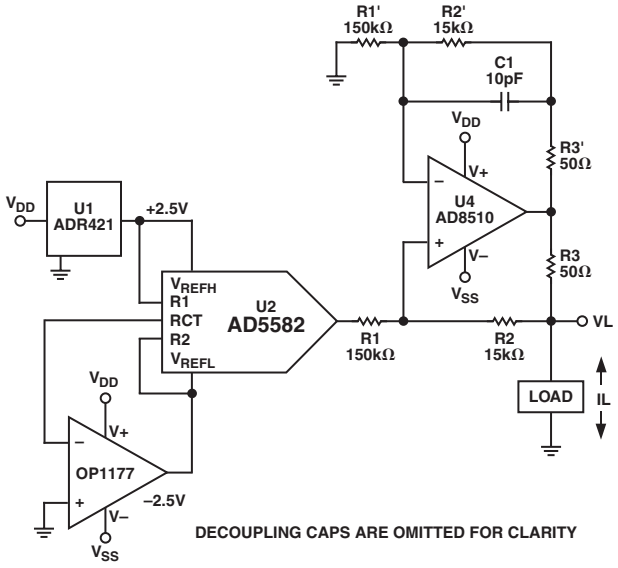


Figure 6. Programmable Current Source with Bidirectional Current Control and High Voltage Compliance Capabilities

Figure 6 shows that if the resistor network is matched, the load current is:

$$I_L = \frac{(R2 + R3)/R1}{R3} V_{IN} \quad (4)$$

*R*3 in theory can be made small to achieve the current needed within the U4 output current driving capability. In this circuit, the AD8510 can deliver ±20 mA in both directions and the voltage compliance approaches +15 V.

This circuit is versatile; however, users must pay attention to the compensation. Without C1, it can be shown that the output impedance becomes:

$$Z_O = \frac{R1'R3(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \quad (5)$$

If the resistors are perfectly matched, Z_O is infinite, which is highly desirable. On the other hand, if they are not matched, Z_O can either be positive or negative. The latter, because of the pole in the right S-plane, can cause oscillation. As a result, C1 in the range of a few pF is needed to prevent the oscillation. For critical applications, C1 should be found empirically without overcompensating.

Boosted Programmable Voltage Source

The AD5582/AD5583 cannot deliver much current without adding external op amp and power transistors. Figure 7 shows programmable power supply with 200 mA capability.

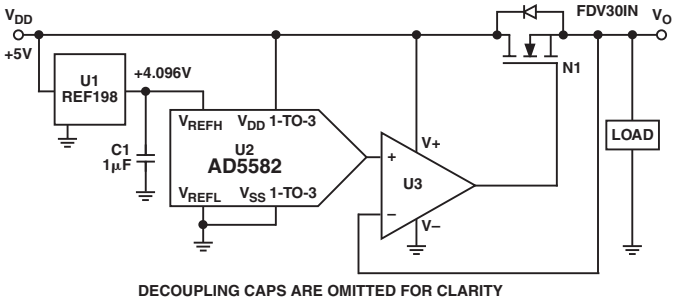


Figure 7. Boosted Programmable Voltage Source

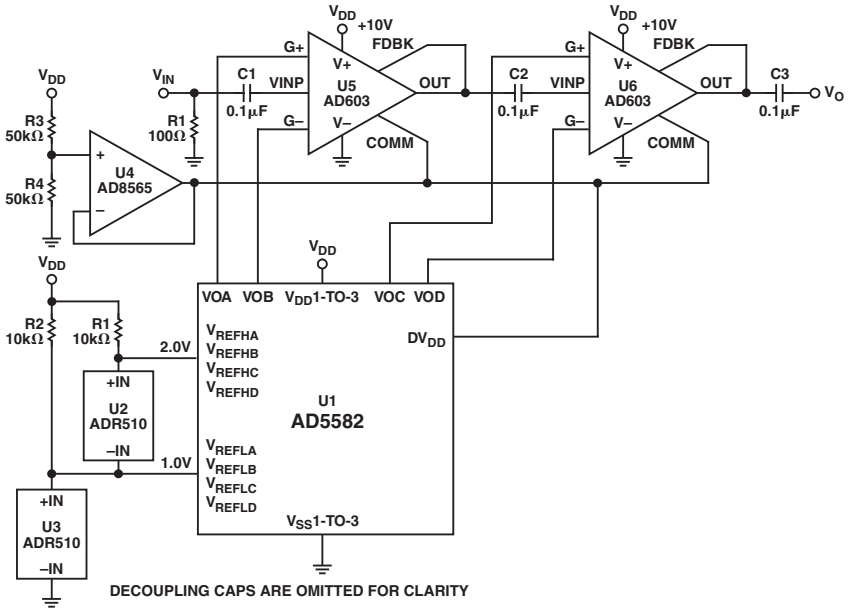


Figure 8. Programmable PGA

In this circuit, the inverting input of the op amp forces the V_O to be equal to the DAC output. The load current is then delivered by the supply via the N-Ch FET N1. U3 needs to be a rail-to-rail input type. With a V_{DD} of 5 V, this circuit can source a maximum of 200 mA at 4.096 V full scale, 100 mA at midscale, and 50 mA near zero-scale outputs. Higher current can be achieved with N1 in a larger package mounted on heat sink.

Programmable PGA

The AD603 is a low noise, voltage controlled amplifier for use in RF and IF AGC (automatic gain control) systems. It provides accurate, pin selectable gains of –11 dB to +31 dB with a bandwidth of 90 MHz, or 9 dB to 51 dB with a bandwidth of 9 MHz. Any intermediate gain range may be arranged using one external resistor between Pin 5 and Pin 7. The input referred noise spectral density is only 1.3 nV/$\sqrt{\text{Hz}}$ and power consumption is 125 mW at the recommended ±5 V supplies.

The decibel gain is linear in dB, accurately calibrated, and stable over temperature and supply. The gain is controlled at a high impedance (50 MΩ), low bias (200 nA) differential input; the scaling is 25 mV/dB, requiring a gain control voltage of only 1 V to span the central 40 dB of the gain range. An overrange and underrange of 1 dB is provided whatever the selected range. The gain control response time is less than 1 ms for a 40 dB change.

The differential gain control interface allows the use of either differential or single-ended positive or negative control voltages, where the common-mode range is –1.2 V to +2.0 V. The AD5582/AD5583 is ideally suited to provide the differential input range of 1 V within the common-mode range of 0 V to 2 V. To accomplish this, place V_{REFH} at 2.0 V and V_{REFL} at 1.0 V, then all 4096 V levels of the AD5582 will fall within the gain control range of the AD603. Please refer to the AD603 data sheet for further information regarding gain control, layout, and general operation.

18-Bit Bipolar DAC

The multichannel, high accuracy, and differential reference capabilities of the AD5582 make it well suited for an enhanced resolution configuration. Three of the four channels of the AD5582 can be cascaded to form one high resolution DAC, as shown in Figure 9, that has a potential of much higher bit resolution than a single channel.

As DAC A and B are moving together to form the coarse adjustment, their outputs are used as the differential references for DAC C. DAC C provides 12-bit fine adjustment but its full adjustment range C is bounded by these differential references programmed by DAC A and B. As a result, the differential references range dictates the final resolution of this circuit. To keep INL and DNL within 1 LSB error at 12-bit resolution (see TPC 11), DAC C differential references are set to 156.25 mV. With V_{REFH}/V_{REFL} of ±5.000 V, the codes of DAC A and B must always be maintained at 64 steps apart when DAC A and B are moving together. The equation that yields 18-bit resolution becomes:

$$V_O = \frac{D_C}{4096}\left\{\left[\begin{array}{l} V_{REF}\left(\frac{D_A}{2048}-1\right) \\ -V_{REF}\left(\frac{D_B}{2048}-1\right)\end{array}\right]\right\} + V_{REF}\left(\frac{D_B}{2048}-1\right) \quad (6)$$

where D_A, D_B, and D_C are the decimal equivalent of the data bits of DAC A, B, and C, respectively. The benefit of achieving such high resolution comes with an expense of programming complexity, as shown in Table II. Notice D is the decimal equivalent of the 18-bit data bit, which must be translated to the equivalent D_A, D_B, and D_C settings. It can be shown that D is equal to:

$$D = \frac{D_C\left(D_A - D_B\right)}{64} + 64D_B - 2^{18} \quad (7)$$

and the condition of

$$D_A = D_B + 64 \quad (8)$$

must always be applied.

Table II. 18-Bit DAC Programming Example

D	D_A	D_B	D_C	V_O
0	64	0	0	–5.00000
2048	64	0	2048	–4.92188
61440	1024	960	0	–2.65625
63488	1024	960	2048	–2.57813
126976	2048	1984	0	–0.15625
129024	2048	1984	2048	–0.07813
257984	4095	4031	0	4.84375
260032	4095	4031	2048	4.920654

Finally, an 18-bit bipolar DAC is formed with DAC A/DAC B controlling the coarse 6-bit and DAC C providing the fine 12-bit adjustment within each coarse step. Notice that this DAC provides 2^{18} numbers of steps of adjustment; the precision remains at 12-bits accurate because of the limitation of the DAC C differential references. As a result, this circuit is suitable for those applications that require 18 bits of adjustment while absolute accuracy is not required.

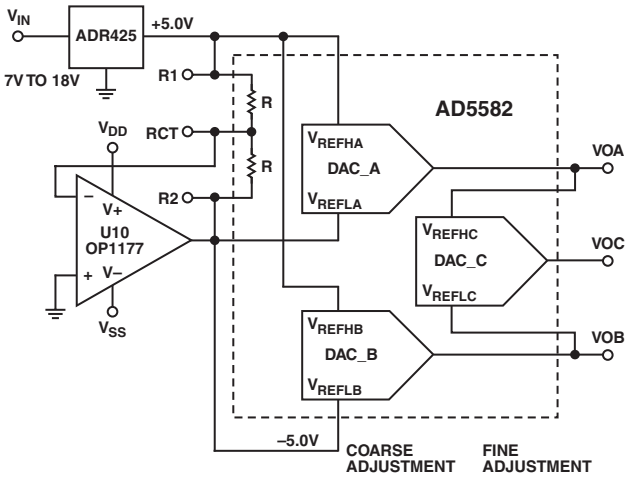
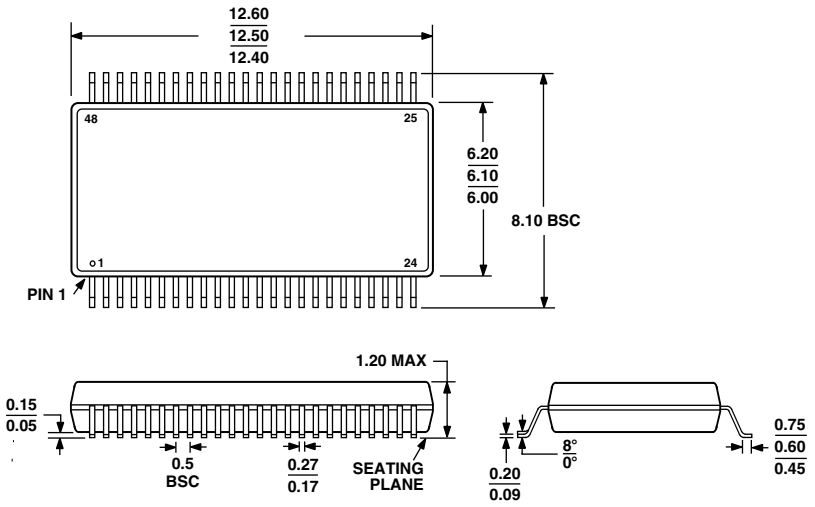


Figure 9. 18-Bit Bipolar DAC

OUTLINE DIMENSIONS

48-Lead Thin Shrink Small Outline Package (TSSOP)
(RV-48)

Dimensions shown in millimeters



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