



# QUAD, Parallel-Input, Voltage Output, 12-/10-Bit Digital-to-Analog Converter

## AD5582/AD5583

### FEATURES

- 12-Bit Linearity and Monotonic  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Single  $+5\text{V}$  to  $+12\text{V}$  or dual  $\pm 5\text{V}$  supply
- Unipolar or Bipolar Operation
- Double Buffered Registers Enable Simultaneous Multi-Channels Update
- 4 Separate Rail-to-Rail Reference Inputs
- Parallel Interface
- Data Readback Capability
- $5\mu\text{s}$  Settling Time

### APPLICATIONS

- Process Control Equipment
- Closed Loop Servo Control
- Data Acquisition Systems
- Digitally Controlled Calibration
- Motor Control
- Optical Network Control Loops

### GENERAL DESCRIPTION

The AD5582/AD5583 family of quad, 12-/10-bit, voltage-output digital-to-analog converter is designed to operate from a single  $+5$  to  $+15$  volt or a dual  $\pm 5\text{V}$  supply. Built using a CBCMOS process, this monolithic DAC offers the user low cost, and ease-of-use in single or dual-supply systems.

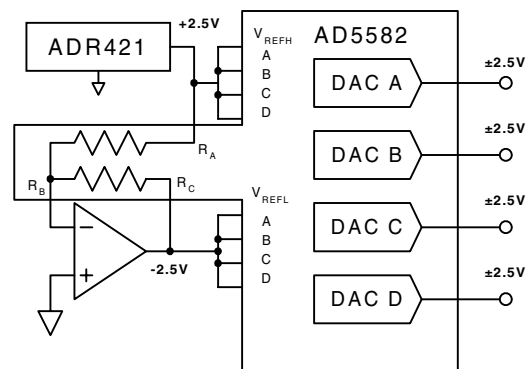
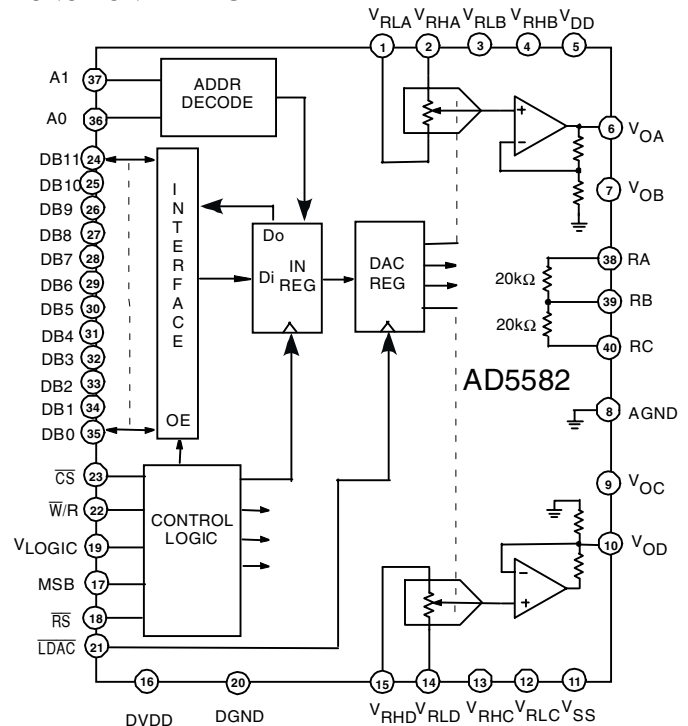
The applied external reference  $V_{REF}$  determines the full-scale output voltage. Valid  $V_{REF}$  values include  $V_{SS} < V_{REF} < V_{DD}$  resulting in a wide selection of full scale outputs. For multiplying applications AC inputs can be as large as  $|V_{DD} - V_{SS}|$ . Two on-board precision trimmed resistors are available for 4-Quadrant configurations.

A doubled-buffered parallel interface offers 25Mbps data load rates. A common level-sensitive load-DAC strobe ( $\overline{\text{LDAC}}$ ) input allows simultaneous update of all DAC outputs from previously loaded Input Registers. An external asynchronous reset ( $\overline{\text{RS}}$ ) forces all registers to the zero code state when  $\text{MSB}=0$  or to midscale when  $\text{MSB}=1$ .

Both parts are offered in the same pin-out to allow users to select the amount of resolution appropriate for their application without circuit card redesign.

The AD5582/AD5583 are specified over the extended industrial ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) temperature range. Packages available include thin 1.1 mm TSSOP-48 package.

### FUNCTIONAL DIAGRAM



DIGITAL CIRCUITRY OMITTED FOR CLARITY

Figure 1 Using Onboard Offset resistors to generate a negative voltage REF

# PRELIMINARY TECHNICAL DATA

## AD5582/AD5583

**ELECTRICAL CHARACTERISTICS** at  $V_{DD} = +5V$ ,  $V_{SS} = -5V$ ,  $V_L = +5V \pm 10\%$ ,  $V_{REFH} = +2.5V$ ,  $V_{REFL} = -2.5V$ ,  $-40^\circ C < T_A < +125^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
<b>STATIC PERFORMANCE</b>						
Resolution <sup>1</sup>	N	AD5582		12		Bits
Resolution <sup>1</sup>	N	AD5583		10		Bits
Relative Accuracy <sup>2</sup>	INL		-1		+1	LSB
Differential Nonlinearity <sup>2</sup>	DNL	Monotonic	-1			LSB
Zero-Scale Error	V <sub>ZSE</sub>	Data = 000H			2	LSB
Full-Scale Voltage Error	V <sub>FSE</sub>	Data = FFFH			2	LSB
Full-Scale Tempco <sup>3</sup>	TCV <sub>FS</sub>			10		ppm/°C
<b>REFERENCE INPUT</b>						
V <sub>REFH</sub> Input Range <sup>4</sup>	V <sub>REFH</sub>		V <sub>SS</sub>		V <sub>DD</sub>	V
V <sub>REFL</sub> Input Range <sup>4</sup>	V <sub>REFL</sub>		V <sub>SS</sub>		V <sub>DD</sub>	V
Input Resistance <sup>8</sup>	R <sub>REF</sub>	Data = 555H	10			KΩ <sup>5</sup>
Input Capacitance <sup>3</sup>	C <sub>REF</sub>			80		pF
REF Input Current	I <sub>REF</sub>				500	μA
REF Multiplying Bandwidth	BW <sub>REF</sub>					Hz
<b>ANALOG OUTPUT</b>						
Output Current	I <sub>OUT</sub>	Data = 800H, ΔV <sub>OUT</sub> = 4LSB			±2	mA
Capacitive Load <sup>3</sup>	C <sub>L</sub>	No Oscillation		500		pF
<b>LOGIC INPUTS</b>						
Logic Input Low Voltage	V <sub>IL</sub>	V <sub>L</sub> = 5V ± 10%			0.8	V
Logic Input High Voltage	V <sub>IH</sub>	V <sub>L</sub> = 5V ± 10%	2.4			V
Input Leakage Current	I <sub>IL</sub>					μA
Input Capacitance <sup>3</sup>	C <sub>IL</sub>					pF
Output Voltage High	V <sub>OH</sub>	I <sub>OH</sub> = -0.8mA	2.4			V
Output Voltage Low	V <sub>OL</sub>	I <sub>OL</sub> = 1.6mA			0.4	V
<b>AC CHARACTERISTICS</b>						
Output Slew Rate	SR	Data = 000H to FFFH to 000H		2		V/μs
Settling Time <sup>7</sup>	t <sub>S</sub>	To ±0.1% of Full Scale		5		μs
Shutdown Recovery	t <sub>SDR</sub>					μs
DAC Glitch	Q	Code 7FF <sub>H</sub> to 800 <sub>H</sub> to 7FF <sub>H</sub>		100		nVs
Digital Feed Through	V <sub>OUT</sub> /t <sub>CS</sub>	Data=800 <sub>H</sub> , CS toggles at f=16MHz		5		nVs
Analog Crosstalk	V <sub>OUT</sub> /V <sub>REF</sub>	V <sub>REF</sub> = 1.5V <sub>DC</sub> +1V <sub>p-p</sub> , Data = 000H, f=100KHz		-80		dB
Output Noise	e <sub>N</sub>			40		nV√Hz
<b>SUPPLY CHARACTERISTICS</b>						
Positive Supply Current	I <sub>DD</sub>	V <sub>IL</sub> = 0V, No Load			3	mA
Negative Supply Current	I <sub>SS</sub>	V <sub>IL</sub> = 0V, No Load			3	mA
Power Dissipation	P <sub>DISS</sub>	V <sub>IL</sub> = 0V, No Load			30	mW
Power Supply Sensitivity	PSS	ΔV <sub>DD</sub> = ±5%		30		ppm/V

**NOTES:**

- DAC Output Equation:  $V_{OUT} = V_{REFL} + [(V_{REFH} - V_{REFL}) * \text{Code} / 2^N]$ , where Code = data loaded in corresponding DAC register A, B, C, D and N equals the DAC resolution AD5582 = 12, AD5583 = 10 bits. One LSB = V<sub>REF</sub>/4096V for the 12-bit AD5582.
- The first two codes (000H, 001H) are excluded from the linearity error measurement in single supply operation.
- These parameters are guaranteed by design and not subject to production testing.
- When V<sub>REF</sub> is connected to either the V<sub>DD</sub> or the V<sub>SS</sub> power supply the corresponding V<sub>OUT</sub> voltage will program between ground and the supply voltage minus the offset voltage of the output buffer, which is the same as the V<sub>ZSE</sub> error specification. See additional discussion in the operation section of the data sheet.
- Typical specifications represent average readings measured at 25°C.
- The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground in single supply operation.

# PRELIMINARY TECHNICAL DATA

## AD5582/AD5583

**ELECTRICAL CHARACTERISTICS** at  $V_{DD} = +15V$ ,  $V_{SS} = 0V$ ,  $V_L = +5V \pm 10\%$ ,  $V_{REFH} = +10V$ ,  $V_{REFL} = 0V$ ,  $-40^\circ C < T_A < +125^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
<b>STATIC PERFORMANCE</b>						
Resolution <sup>1</sup>	N	AD5582		12		Bits
Resolution <sup>1</sup>	N	AD5583		10		Bits
Relative Accuracy <sup>2</sup>	INL		-1		+1	LSB
Differential Nonlinearity <sup>2</sup>	DNL	Monotonic	-1			LSB
Zero-Scale Error	V <sub>ZSE</sub>	Data = 000 <sub>H</sub>			2	LSB
Full-Scale Voltage Error	V <sub>FSE</sub>	Data = FFF <sub>H</sub>			2	LSB
Full-Scale Tempco <sup>3</sup>	TCV <sub>FS</sub>			10		ppm/°C
<b>REFERENCE INPUT</b>						
V <sub>REFH</sub> Input Range <sup>4</sup>	V <sub>REFH</sub>		V <sub>SS</sub>		V <sub>DD</sub>	V
V <sub>REFL</sub> Input Range <sup>4</sup>	V <sub>REFL</sub>		0		V <sub>DD</sub>	V
Input Resistance <sup>8</sup>	R <sub>REF</sub>	Data = 555 <sub>H</sub>	10			KΩ <sup>5</sup>
Input Capacitance <sup>3</sup>	C <sub>REF</sub>			80		pF
REF Input Current	I <sub>REF</sub>				500	μA
REF Multiplying Bandwidth	BW <sub>REF</sub>					Hz
<b>ANALOG OUTPUT</b>						
Output Current	I <sub>OUT</sub>	Data = 800 <sub>H</sub> , ΔV <sub>OUT</sub> = 4LSB			+5	mA
Capacitive Load <sup>3</sup>	C <sub>L</sub>	No Oscillation		500		pF
<b>LOGIC INPUTS/OUTPUTS</b>						
Logic Input Low Voltage	V <sub>IL</sub>				0.8	V
Logic Input High Voltage	V <sub>IH</sub>		2.4			V
Input Leakage Current	I <sub>IL</sub>					μA
Input Capacitance <sup>3</sup>	C <sub>IL</sub>					pF
Output Voltage High	V <sub>OH</sub>	I <sub>OH</sub> = -0.8mA	2.4			V
Output Voltage Low	V <sub>OL</sub>	I <sub>OL</sub> = 1.6mA			0.4	V
<b>AC CHARACTERISTICS</b>						
Output Slew Rate	SR	Data = 000 <sub>H</sub> to FFF <sub>H</sub> to 000 <sub>H</sub>		2		V/μs
Settling Time <sup>7</sup>	t <sub>S</sub>	To ±0.1% of Full Scale		5		μs
Shutdown Recovery	t <sub>SDR</sub>					μs
DAC Glitch	Q	Code 7FF <sub>H</sub> to 800 <sub>H</sub> to 7FF <sub>H</sub>		100		nVs
Digital Feed Through	V <sub>OUT</sub> /t <sub>CS</sub>	Data=800 <sub>H</sub> , CS toggles at f=16MHz		5		nVs
Analog Crosstalk	V <sub>OUT</sub> /V <sub>REF</sub>	V <sub>REFH</sub> = 2.5V <sub>DC</sub> +1V <sub>p-p</sub> , Data = 000 <sub>H</sub> , f=100KHz		-80		dB
Output Noise	e <sub>N</sub>			40		nV√Hz
<b>SUPPLY CHARACTERISTICS</b>						
Positive Supply Current	I <sub>DD</sub>	V <sub>IL</sub> = 0V, No Load			3	mA
Power Dissipation	P <sub>DISS</sub>	V <sub>IL</sub> = 0V, No Load			45	mW
Power Supply Sensitivity	PSS	ΔV <sub>DD</sub> = ±5%		30		ppm/V

### NOTES:

- DAC Output Equation:  $V_{OUT} = V_{REFL} + [(V_{REFH} - V_{REFL}) * \text{Code} / 2^N]$ , where Code = data loaded in corresponding DAC register A, B, C, D and N equals the DAC resolution AD5582 = 12, AD5583 = 10 bits. One LSB = V<sub>REF</sub>/4096V for the 12-bit AD5582.
- The first two codes (000<sub>H</sub>, 001<sub>H</sub>) are excluded from the linearity error measurement in single supply operation.
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- When V<sub>REF</sub> is connected to either the V<sub>DD</sub> or the V<sub>SS</sub> power supply the corresponding V<sub>OUT</sub> voltage will program between ground and the supply voltage minus the offset voltage of the output buffer, which is the same as the V<sub>ZSE</sub> error specification. See additional discussion in the operation section of the data sheet.
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# PRELIMINARY TECHNICAL DATA

## AD5582/AD5583

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PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
<b>INTERFACE TIMING<sup>1,2</sup></b>						
Clock Frequency	$f_{CLK}$				25	MHz
Chip Select Write Pulsewidth	$t_{WCS}$		30			ns
Write Setup	$t_{WS}$	$t_{WCS} = 50$ ns	0			ns
Write Hold	$t_{WH}$	$t_{WCS} = 50$ ns	0			ns
Address Setup	$t_{AS}$		0			ns
Address Hold	$t_{AH}$		0			ns
Load Setup	$t_{LS}$		70			ns
Load Hold	$t_{LH}$		30			ns
Write Data Setup	$t_{WDS}$	$t_{WCS} = 50$ ns	0			ns
Write Data Hold	$t_{WDH}$	$t_{WCS} = 50$ ns	0			ns
Load Data Pulsewidth	$t_{LDW}$		50			ns
Reset Pulsewidth	$t_{RESET}$		50			ns
Chip Select Read Pulsewidth	$t_{RCS}$		130			ns
Read Data Hold	$t_{RDH}$	$t_{RCS} = 130$ ns	0			ns
Read Data Setup	$t_{RDS}$	$t_{RCS} = 130$ ns	0			ns
Data to Hi Z	$t_{DZ}$	$C_L = 10$ pF		100		ns
Chip Select to Data	$t_{CSD}$	$C_L = 100$ pF		100		ns
Chip Select Repetitive Pulsewidth	$t_{CSP}$		10			ns
Load Setup in Double Buffer Mode	$t_{LDS}$		20			ns

### NOTES:

- All input control signals are specified with  $t_R = t_F = 2$  ns (10% to 90% of +3V) and timed from a voltage level of 1.5V.
- Typicals represent average readings measured at 25°C.

### ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to $V_{SS}$ .....	-0.3V to +16.5V
$V_{DD}$ to GND.....	-0.3V to 5.5V
$V_{SS}$ to GND.....	+0.3V to -5.5V
$V_{DD}$ to $V_{REF+}$ .....	-0.3V to ( $V_{DD} - V_{SS}$ )
$V_{REF-}$ to $V_{SS}$ .....	-0.3V to ( $V_{DD} - V_{SS}$ )
$V_{REFH}$ to $V_{REFL}$ .....	-0.3V to ( $V_{DD} - V_{SS}$ )
Logic Inputs to GND.....	$V_{SS} - 0.3V$ , $V_{DD} + 0.3V$
$V_{OUT}$ to GND.....	$V_{SS} - 0.3V$ , $V_{DD} + 0.3V$
$I_{OUT}$ Short Circuit to GND.....	.....
Thermal Resistance $\theta_{JA}$	
TSSOP-48 Lead (RU-48).....	xxx°C/W

Maximum Junction Temperature ( $T_J$ MAX).....	150°C
Package Power Dissipation = ( $T_J$ MAX - $T_A$ )/ $\theta_{JA}$	
Operating Temperature Range.....	-40°C to +125°C
Storage Temperature Range.....	-65°C to +150°C
Lead Temperature:	
RU-48 (Vapor Phase, 60 secs).....	xxx°C
RU-44 (Infrared, 15 secs).....	xxx°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ORDERING GUIDE:

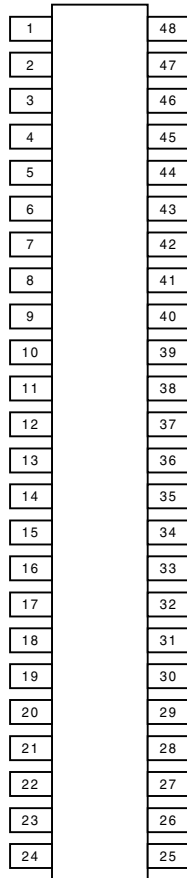
MODEL	Resolution (Bits)	TEMP RANGE	Package Description	Package Option	Container Qty
AD5582YRU-REEL7	12	-40/+125°C	TSSOP-48	RU-48	
AD5583YRU-REEL7	10	-40/+125°C	TSSOP-48	RU-48	

The AD5582 contains xxx transistors. The die size measures 108 mil X 144 mil.

# PRELIMINARY TECHNICAL DATA

## AD5582/AD5583

### PIN CONFIGURATION



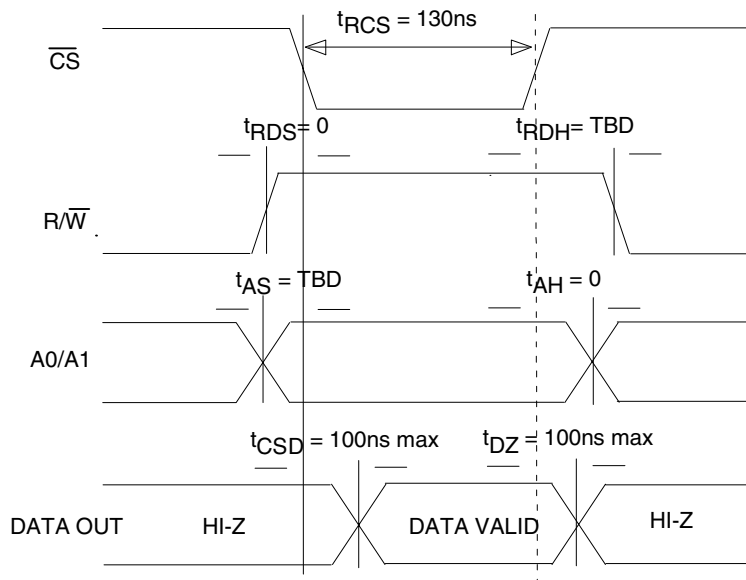
**NOTE: Pin Out not finalized!**

**Please contact Analog Devices Inc. for final version**

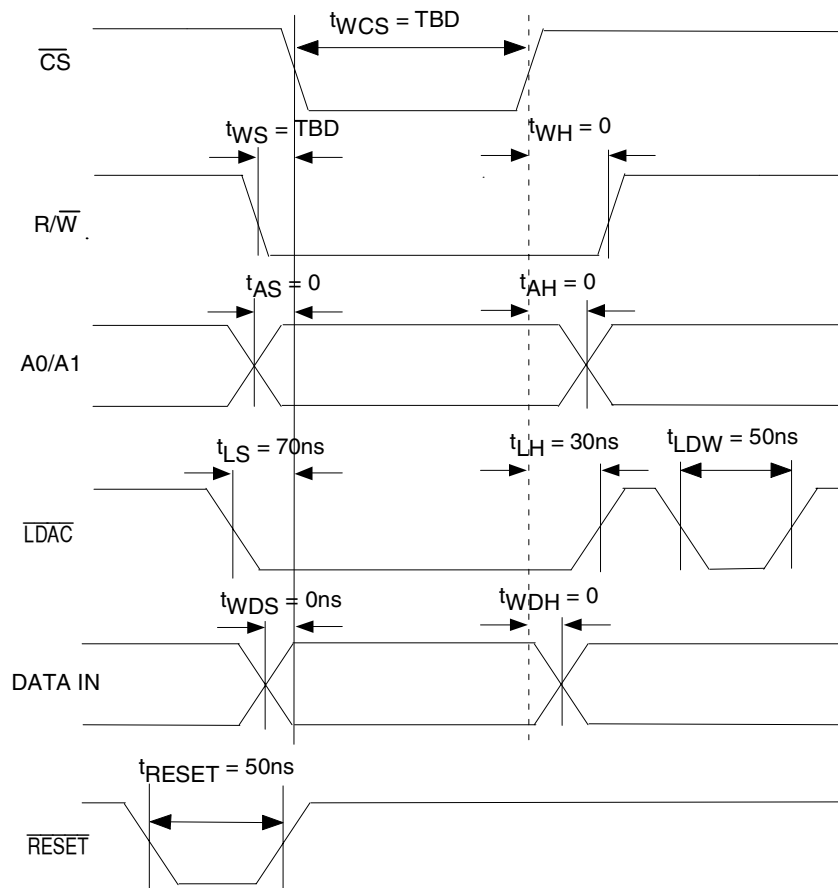
Pin#	Name	Description
	VRLA	Voltage Reference Low Input Terminal DAC A
	VRHA	Voltage Reference High Input Terminal DAC A
	VRLB	Voltage Reference Low Input Terminal DAC B
	VRHB	Voltage Reference High Input Terminal DAC B
	VDD	Positive Power Supply
	VOA	DAC A Output
	VOB	DAC B output
	RA	End Tap Offset Resistor
	RB	Center Tap Offset Resistor
	RC	End Tap Offset Resistor
	AGND	Analog Ground
	VOC	Voltage Out DAC C
	VOD	DAC D Output
	VSS	Negative Power Supply
	VRLC	Voltage Reference Low Input Terminal DAC C
	VRHC	Voltage Reference High Input Terminal DAC C
	VRLD	Voltage Reference Low Input Terminal DAC D
	VRHD	Voltage Reference High Input Terminal DAC D
	DGND	Digital Ground
	DVDD	
	LDAC	DAC Register Load, active low level sensitive
	RS	Reset strobe
	MSB	Reset Mode: MSB=0 Code = 000 <sub>H</sub> , MSB=1 Code = 800 <sub>H</sub>
	VL	Logic Supply Voltage
	W/R	Write Read Mode select
	CS	Chip Select, active low
	DB0	Data Bit 0
	DB1	Data Bit 1
	DB2	Data Bit 2
	DB3	Data Bit 3
	DB4	Data Bit 4
	DB5	Data Bit 5
	DB6	Data Bit 6
	DB7	Data Bit 7
	DB8	Data Bit 8
	DB9	Data Bit 9
	DB10	Data Bit 10
	DB11	Data Bit 11
	A0	Address Input 0
	A1	Address Input 1

# PRELIMINARY TECHNICAL DATA

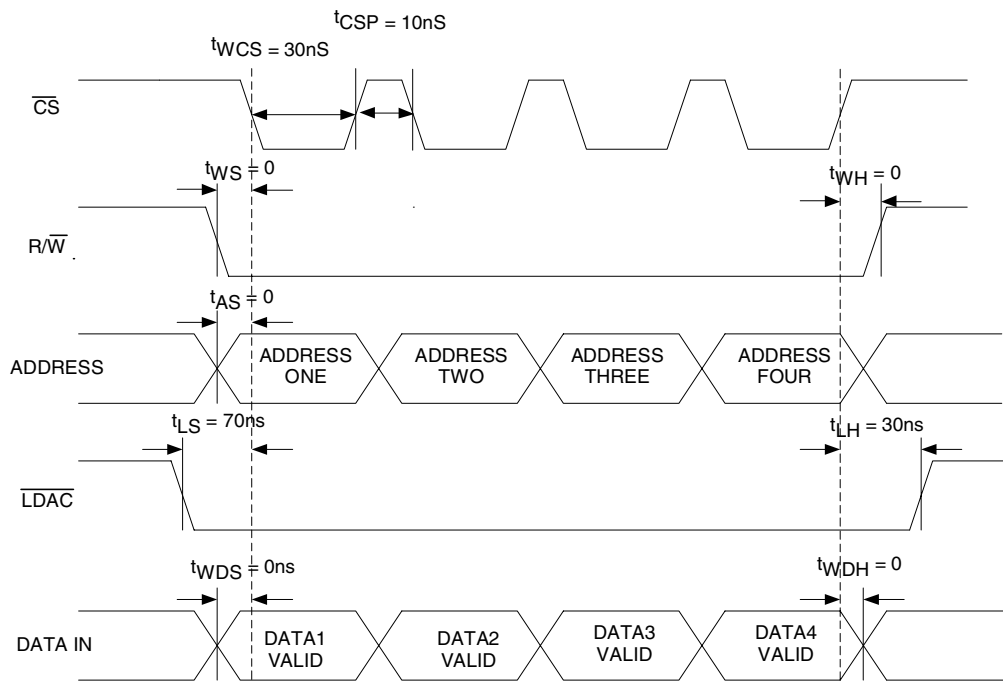
## AD5582/AD5583



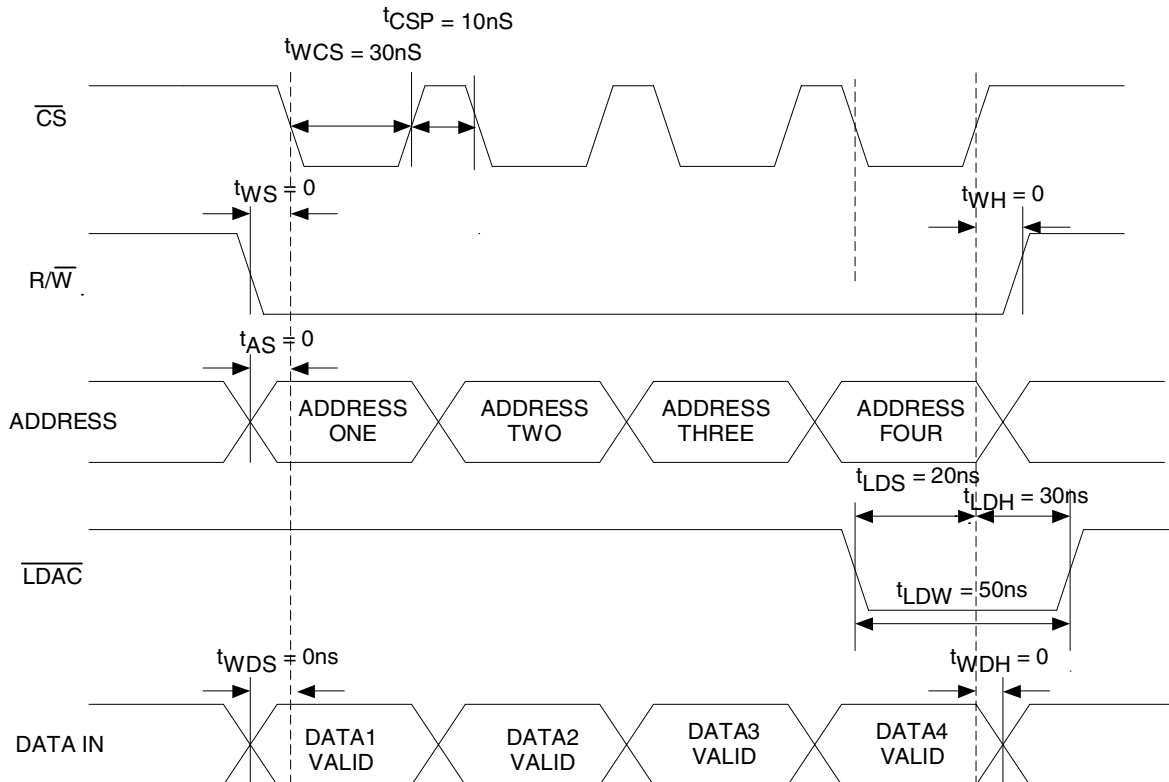
DATA OUTPUT (READ TIMING)



DATA WRITE (INPUT AND OUTPUT REGISTERS) TIMING



SINGLE BUFFER MODE  
(OUTPUT UPDATED INDIVIDUALLY)



DOUBLE BUFFER MODE  
(OUTPUT UPDATED SIMULTANEOUSLY)

**OUTLINE DIMENSIONS**  
 Dimensions shown in inches and (mm)

**48-Lead TSSOP**  
**(RU Suffix)**

