

### FEATURES

#### Very High DC Precision

- 30  $\mu\text{V}$  max Offset Voltage
- 0.3  $\mu\text{V}/^\circ\text{C}$  max Offset Voltage Drift
- 0.35  $\mu\text{V}$  p-p max Voltage Noise (0.1 Hz to 10 Hz)
- 5 Million V/V min Open Loop Gain
- 130 dB min CMRR
- 120 dB min PSRR

#### Matching Characteristics

- 30  $\mu\text{V}$  max Offset Voltage Match
- 0.3  $\mu\text{V}/^\circ\text{C}$  max Offset Voltage Drift Match
- 130 dB min CMRR Match

#### Single Version: AD707

Available in 8-Pin Plastic Mini-DIP,  
Hermetic Cerdip and TO-99 Metal Can  
Packages, Chips and /883B Parts Available.

### PRODUCT DESCRIPTION

The AD708 is a very high precision, dual monolithic operational amplifier. Each amplifier individually offers excellent dc precision with the best available max offset voltage and offset voltage drift of any dual bipolar op amp. In addition, the matching specifications are the best available in any dual op amp.

The AD708 sets a new standards for dual precision op amps by providing 5 V/ $\mu\text{V}$  min open loop gain and guaranteed max input voltage noise of 350 nV p-p (0.1 Hz to 10 Hz). All dc specifications show excellent stability over temperature, with offset voltage drift typically 0.1  $\mu\text{V}/^\circ\text{C}$  and input bias current drift of 25 pA/ $^\circ\text{C}$  max. Both CMRR (130 dB min) and PSRR (120 dB min) are an order of magnitude improved over any available single monolithic op amp except the AD707.

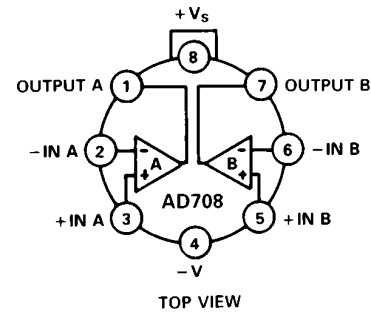
The AD708 is available in four performance grades. The AD708J is rated over the commercial temperature range of  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  and is available in a plastic mini-DIP package. The AD708A and AD708B are rated over the industrial temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  and are available in a cerdip and TO-99 package. The AD708S is rated over the military temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  and is available in cerdip and TO-99 packages. Military versions are available processed to MIL-STD-883B, Rev. C.

### REV. B

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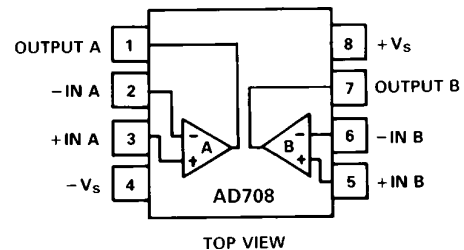
### CONNECTION DIAGRAMS

#### TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE

#### Plastic (N), and Cerdip (Q) Packages



### APPLICATION HIGHLIGHTS

1. The combination of outstanding matching and individual specifications make the AD708 ideal for constructing high gain, precision instrumentation amplifiers.
2. The low offset voltage drift and low noise of the AD708 allows the designer to amplify very small signals without sacrificing overall system performance.
3. The AD708's 10 V/ $\mu\text{V}$  typical open loop gain and 140 dB common-mode rejection make it ideal for precision applications.
4. Unmounted dice are available for hybrid circuit applications.
5. The AD708 is an improved replacement for the LT1002.

# AD708—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD708J/A			AD708B			AD708S			Units	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
INPUT OFFSET VOLTAGE <sup>1</sup>	$T_{MIN}$ to $T_{MAX}$		30	100		5	50		5	30	μV	
		Drift		50	150		15	65		15	50	μV
		Long Term Stability		0.3	1.0		0.1	0.4		0.1	0.3	μV/°C
				0.3			0.3			0.3		μV/Month
INPUT BIAS CURRENT	$T_{MIN}$ to $T_{MAX}$		1.0	2.5		0.5	1.0		0.5	1	nA	
		Average Drift		2.0	4.0		1.0	2.0		1.0	4	nA
				15	40		10	25		10	30	pA/°C
OFFSET CURRENT	$V_{CM} = 0$ V $T_{MIN}$ to $T_{MAX}$		0.5	2.0		0.1	1.0		0.1	1	nA	
		Average Drift		2.0	4.0		0.2	1.5		0.2	1.5	nA
				2	60		1	25		1	25	pA/°C
MATCHING CHARACTERISTICS <sup>2</sup>	$T_{MIN}$ to $T_{MAX}$	Offset Voltage			80			50			30	μV
		Offset Voltage Drift			150			75			50	μV
		Input Bias Current			1.0			0.4			0.3	μV/°C
		Common-Mode Rejection			4.0			1.0			1.0	nA
	$T_{MIN}$ to $T_{MAX}$			5.0			2.0				2.0	nA
		Power Supply Rejection	120	140		130	140		130	140		dB
	$T_{MIN}$ to $T_{MAX}$	Channel Separation	110			130			130			dB
			110			120			120			dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		0.23	0.6		0.23	0.6		0.23	0.35	μV p-p	
		f = 10 Hz		10.3	18		10.3	12		10.3	12	nV/√Hz
		f = 100 Hz		10.0	13.0		10.0	11.0		10.0	11	nV/√Hz
		f = 1 kHz		9.6	11.0		9.6	11.0		9.6	11	nV/√Hz
INPUT CURRENT NOISE	0.1 Hz to 10 Hz		14	35		14	35		14	35	pA p-p	
		f = 10 Hz		0.32	0.9		0.32	0.8		0.32	0.8	pA/√Hz
		f = 100 Hz		0.14	0.27		0.14	0.23		0.14	0.23	pA/√Hz
		f = 1 kHz		0.12	0.18		0.12	0.17		0.12	0.17	pA/√Hz
COMMON-MODE REJECTION RATIO	$V_{CM} = \pm 13$ V $T_{MIN}$ to $T_{MAX}$		120	140		130	140		130	140	dB	
			120	140		130	140		130	140	dB	
OPEN-LOOP GAIN	$V_O = \pm 10$ V $R_{LOAD} \geq 2$ kΩ $T_{MIN}$ to $T_{MAX}$		3	10		5	10		4	10	V/μV	
			3	10		5	10		4	7	V/μV	
POWER SUPPLY REJECTION RATIO	$V_S = \pm 3$ V to $\pm 18$ V $T_{MIN}$ to $T_{MAX}$		110	130		120	130		120	130	dB	
			110	130		120	130		120	130	dB	
FREQUENCY RESPONSE	Closed Loop Bandwidth		0.5	0.9		0.5	0.9		0.5	0.9	MHz	
		Slew Rate		0.15	0.3		0.15	0.3		0.15	0.3	V/μs
INPUT RESISTANCE	Differential			60			200			200	MΩ	
		Common Mode			200			400			400	GΩ
OUTPUT VOLTAGE	$R_{LOAD} \geq 10$ kΩ $R_{LOAD} \geq 2$ kΩ $R_{LOAD} \geq 1$ kΩ $R_{LOAD} \geq 2$ kΩ $T_{MIN}$ to $T_{MAX}$		13.5	14		13.5	14.0		13.5	14	±V	
			12.5	13.0		12.5	13.0		12.5	13	±V	
			12.0	12.5		12.0	12.5		12.0	12.5	±V	
			12.0	13.0		12.0	13.0		12.0	13	±V	
			12.0	13.0		12.0	13.0		12.0	13	±V	
OPEN-LOOP OUTPUT RESISTANCE			60			60			60	Ω		

Model	Conditions	AD708J/A			AD708B			AD708S			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY											
Quiescent Current	$V_S = \pm 15\text{ V}$ No Load	4.5	5.5		4.5	5.5		4.5	5.5		mA
Power Consumption		<b>135</b>	<b>165</b>		<b>135</b>	<b>165</b>		<b>135</b>	<b>165</b>		mW
		$V_S = \pm 3\text{ V}$	12	18		12	18		12	18	
Operating Range		$\pm 3$	$\pm 18$		$\pm 3$	$\pm 18$		$\pm 3$	$\pm 18$		V

**NOTES**

<sup>1</sup>Input offset voltage specifications are guaranteed after 5 minutes of operation at  $T_A = +25^\circ\text{C}$ .

<sup>2</sup>Matching is defined as the difference between parameters of the two amplifiers.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

- Supply Voltage . . . . .  $\pm 22\text{ V}$
- Internal Power Dissipation<sup>2</sup>
- Input Voltage<sup>3</sup> . . . . .  $\pm V_S$
- Output Short Circuit Duration . . . . . Indefinite
- Differential Input Voltage . . . . .  $+V_S$  and  $-V_S$
- Storage Temperature Range (Q, H) . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$
- Storage Temperature Range (N) . . . . .  $-65^\circ\text{C}$  to  $+125^\circ\text{C}$
- Lead Temperature Range (Soldering 60 sec) . . . . .  $+300^\circ\text{C}$

**NOTES**

<sup>1</sup>Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

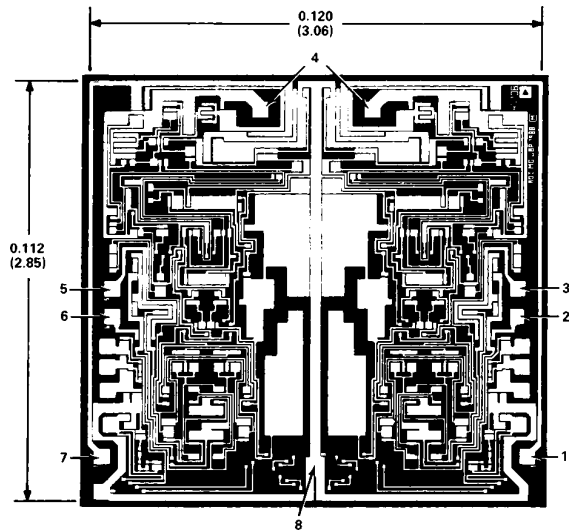
<sup>2</sup>Thermal Characteristics

- 8-Pin Plastic Package:  $\theta_{JC} = 33^\circ\text{C/Watt}$ ,  $\theta_{JA} = 100^\circ\text{C/Watt}$
- 8-Pin Cerdip package:  $\theta_{JC} = 30^\circ\text{C/Watt}$ ,  $\theta_{JA} = 110^\circ\text{C/Watt}$
- 8-Pin Metal Can Package:  $\theta_{JC} = 65^\circ\text{C/Watt}$ ,  $\theta_{JA} = 150^\circ\text{C/Watt}$ .

<sup>3</sup>For supply voltages less than  $\pm 22\text{ V}$ , the absolute maximum input voltage is equal to the supply voltage.

**METALIZATION PHOTOGRAPH**

Dimensions shown in inches and (mm).  
Contact factory for latest dimensions.



**ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option*
AD708JN	$0^\circ\text{C}$ to $+70^\circ\text{C}$	8-Pin Plastic DIP	N-8
AD708AQ	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	8-Pin Cerdip	Q-8
AD708BQ	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	8-Pin Cerdip	Q-8
AD708SQ	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	8-Pin Cerdip	Q-8
AD708AH	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	8-Pin Header	H-08A
AD708BH	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	8-Pin Header	H-08A
AD708SH	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	8-Pin Header	H-08A
AD708SH/883B	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	8-Pin Header	H-08A
AD708J Grade Chips	$0^\circ\text{C}$ to $+70^\circ\text{C}$	Die	
AD708S Grade Chips	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	Die	

\*N = Plastic DIP; Q = Cerdip; H = Hermetic Metal Can.

# AD708—Typical Characteristics ( $V_S = \pm 15\text{ V}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted)

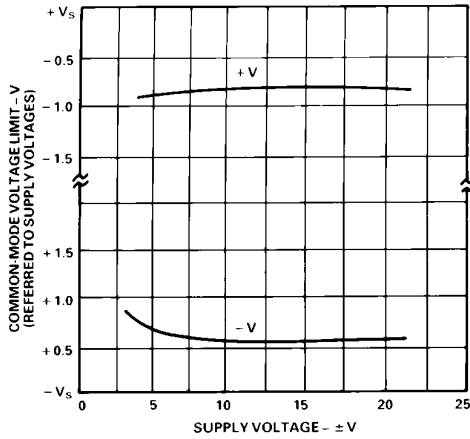


Figure 1. Input Common-Mode Range vs. Supply Voltage

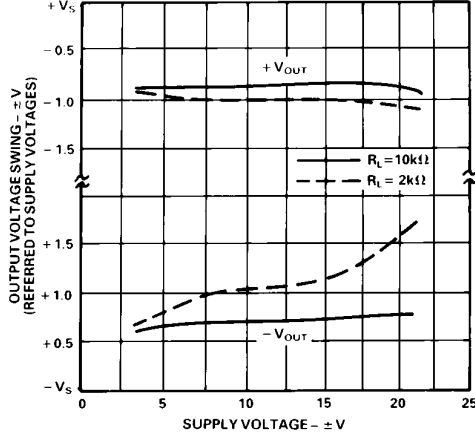


Figure 2. Output Voltage Swing vs. Supply Voltage

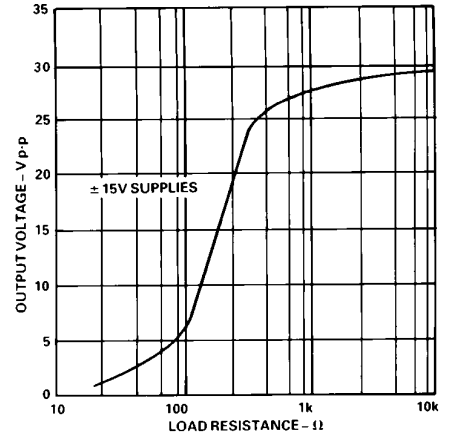


Figure 3. Output Voltage Swing vs. Load Resistance

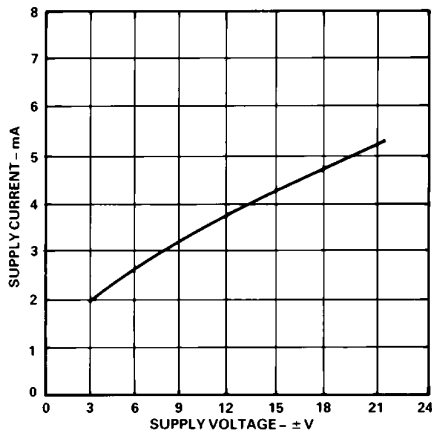


Figure 4. Supply Current vs. Supply Voltage

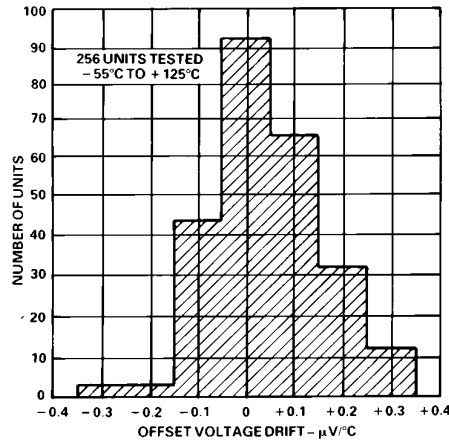


Figure 5. Typical Distribution of Offset Voltage Drift

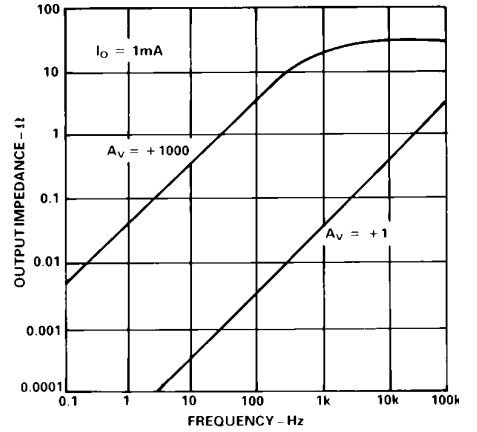


Figure 6. Output Impedance vs. Frequency

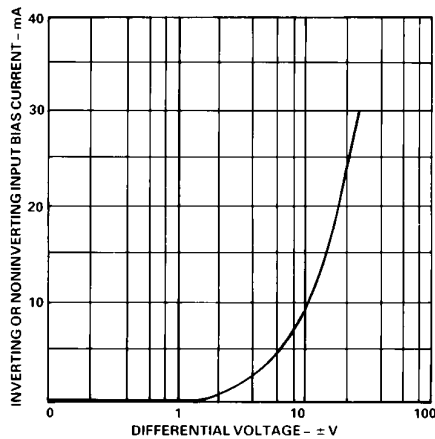


Figure 7. Input Bias Current vs. Differential Input Voltage

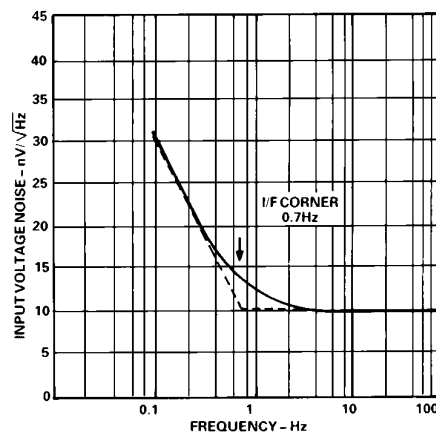


Figure 8. Input Noise Spectral Density

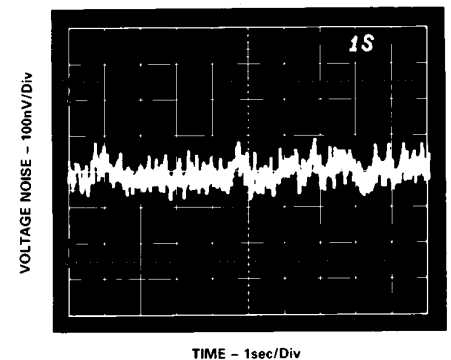


Figure 9. 0.1Hz to 10Hz Voltage Noise

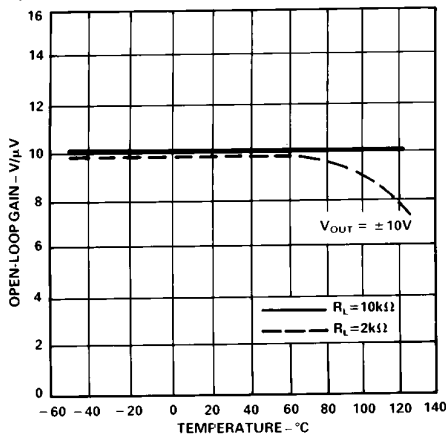


Figure 10. Open-Loop Gain vs. Temperature

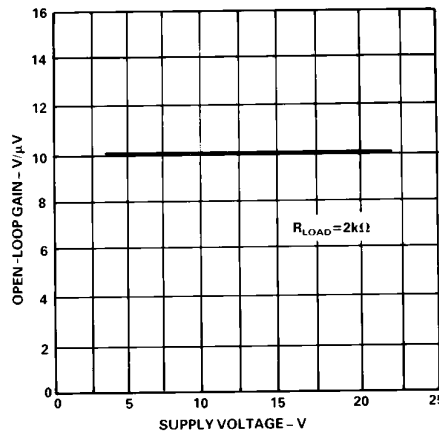


Figure 11. Open-Loop Gain vs. Supply Voltage

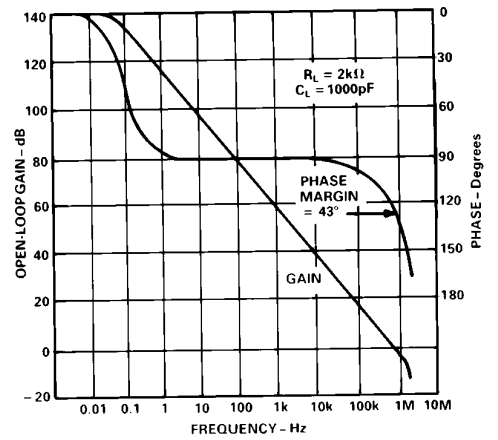


Figure 12. Open-Loop Gain and Phase vs. Frequency

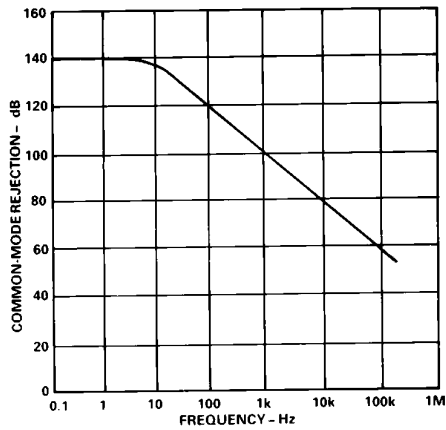


Figure 13. Common-Mode Rejection vs. Frequency

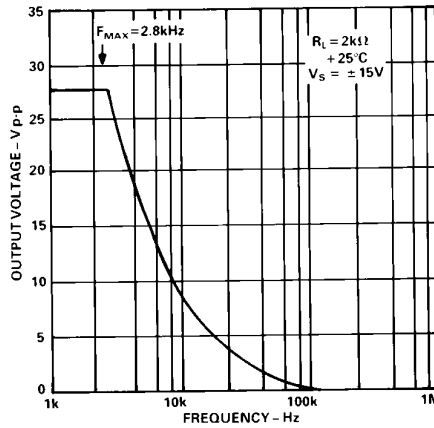


Figure 14. Large Signal Frequency Response

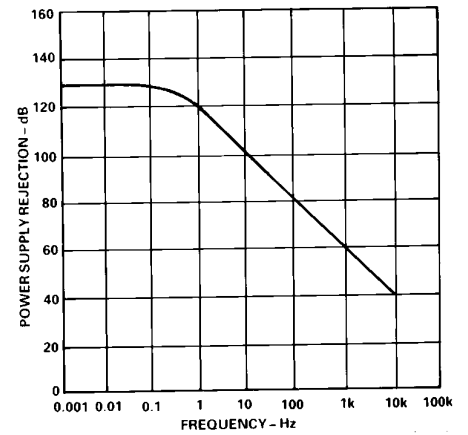


Figure 15. Power Supply Rejection vs. Frequency

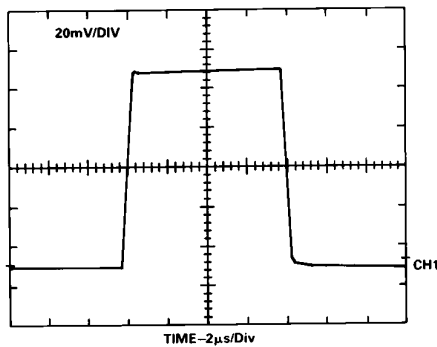


Figure 16. Small Signal Transient Response;  
 $A_V = +1$ ,  $R_L = 2k\Omega$ ,  $C_L = 50pF$

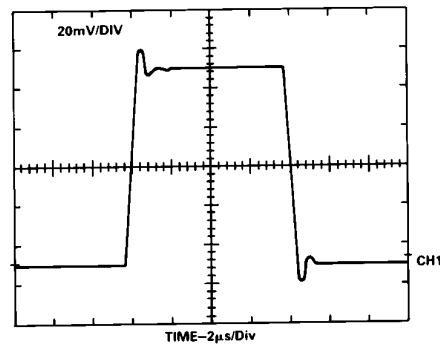


Figure 17. Small Signal Transient Response;  
 $A_V = +1$ ,  $R_L = 2k\Omega$ ,  $C_L = 1000pF$

# AD708—Matching Characteristics

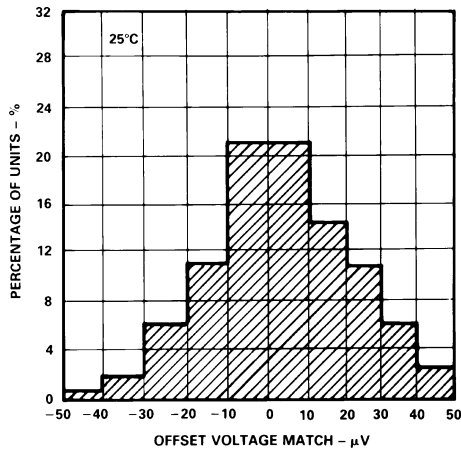


Figure 18. Typical Distribution of Offset Voltage Match

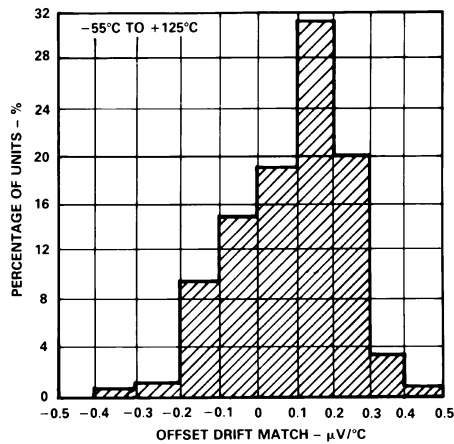


Figure 19. Typical Distribution of Offset Voltage Drift Match

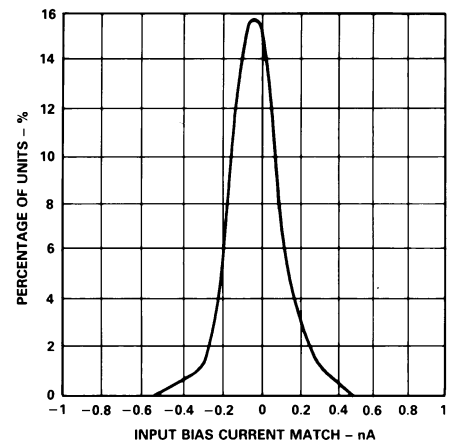


Figure 20. Typical Distribution of Input Bias Current Match

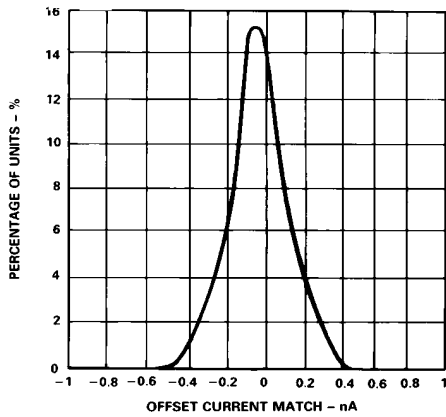


Figure 21. Typical Distribution of Input Offset Current Match

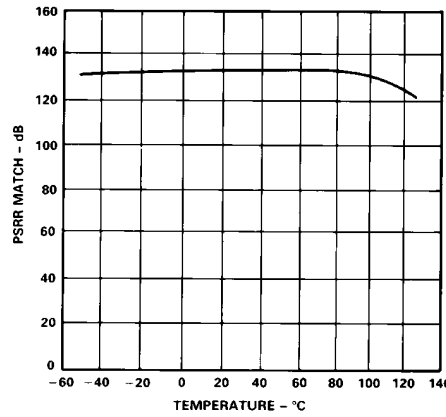


Figure 22. PSRR Match vs. Temperature

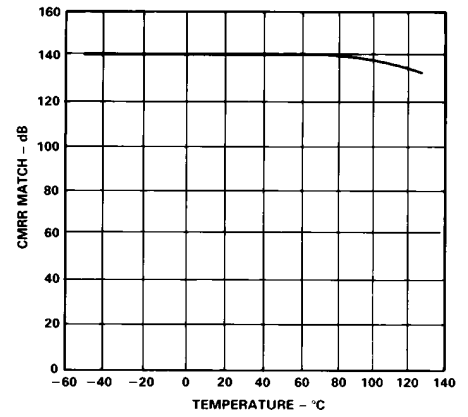


Figure 23. CMRR Match vs. Temperature

## Crosstalk from Thermal Effects of Power Dissipation

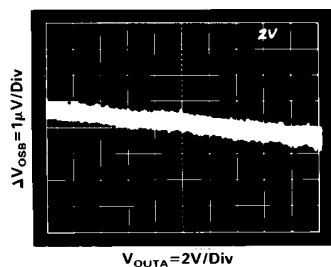
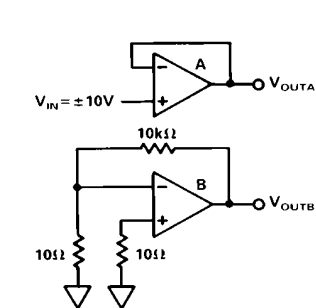


Figure 24. Crosstalk with No Load

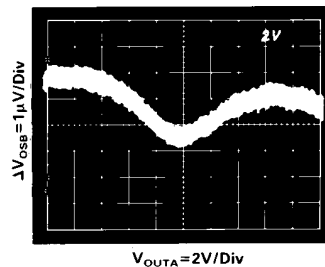
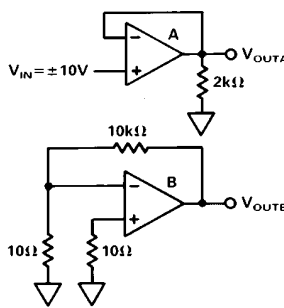


Figure 25. Crosstalk with 2 kΩ Load

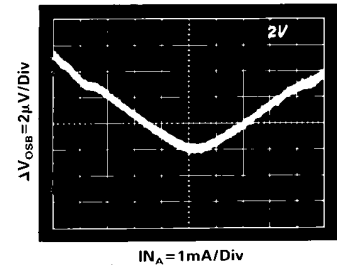
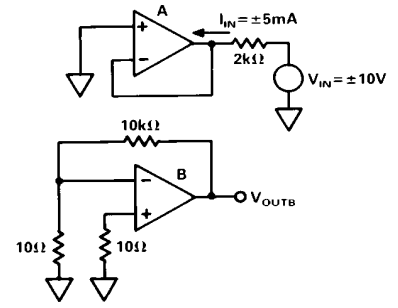


Figure 26. Crosstalk under Forced Source and Sink Conditions



# AD708

As configured, the circuit only requires a gain resistor,  $R_G$ , of suitable accuracy and a stable, accurate voltage reference. The transfer function is:

$$V_O = V_{REF} [\Delta R / (R + \Delta R)] [R_G / R]$$

and the only significant errors due to the AD708S are:

$$V_{OSout} = (V_{OSmatch})(2R_G/R) = 30 \text{ mV}$$

$$V_{OSout}(T) = (V_{OSdrift})(2R_G/R) = 0.3 \text{ mV}/^\circ\text{C}$$

To achieve high accuracy, the resistor  $R_G$  should be 0.1% or better and have a low drift coefficient.

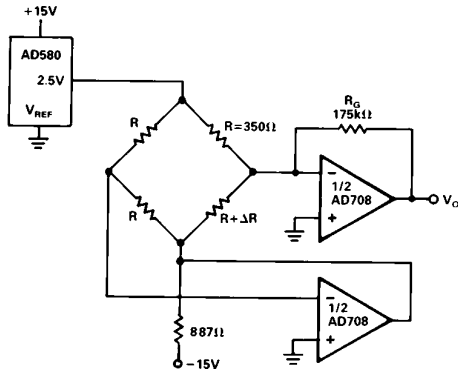


Figure 29. Bridge Signal Conditioning Circuit

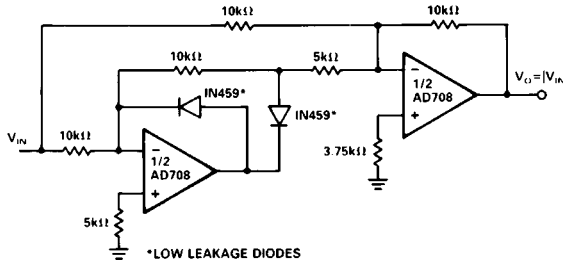


Figure 30. Precision Absolute Value Circuit

## PRECISION ABSOLUTE VALUE CIRCUIT

The AD708 is ideally suited to the precision absolute value circuit shown in Figure 30. The low offset voltage match of the AD708 enables this circuit to accurately resolve the input signal. In addition, the tight offset voltage drift match maintains the resolution of the circuit over the full military temperature range. The AD708's high dc open loop gain and exceptional gain linearity allows the circuit to perform well at both large and small signal levels.

In this circuit, the only significant dc errors are due to the offset voltage of the two amplifiers, the input offset current match of the amplifiers, and the mismatch of the resistors. Errors associated with the AD708S contribute less than 0.001% error over  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

Maximum error at  $25^\circ\text{C}$

$$\frac{30 \mu\text{V} + (10 \text{ k}\Omega)(1 \text{ nA})}{10 \text{ V}} = 40 \mu\text{V}/10 \text{ V} = 4 \text{ ppm Maximum}$$

error at  $+125^\circ\text{C}$  or  $-55^\circ\text{C}$

$$\frac{50 \mu\text{V} + (2 \text{ nA})(10 \text{ k}\Omega)}{10 \text{ V}} = 7 \text{ ppm @ } +125^\circ\text{C}$$

Figure 31 shows  $V_{OUT}$  vs.  $V_{IN}$  for this circuit with a  $\pm 3 \text{ mV}$  input signal at 0.05 Hz. Note that the circuit exhibits very low offset at the zero crossing. This circuit can also produce  $V_{OUT} = -|V_{IN}|$  by reversing the polarity of the two diodes.

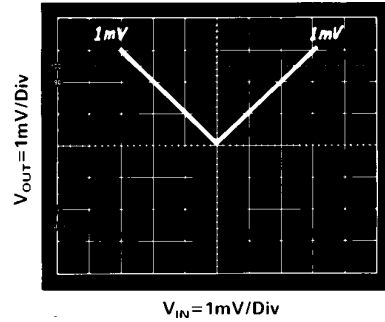


Figure 31. Absolute Value Circuit Performance (Input Signal = 0.05 Hz)

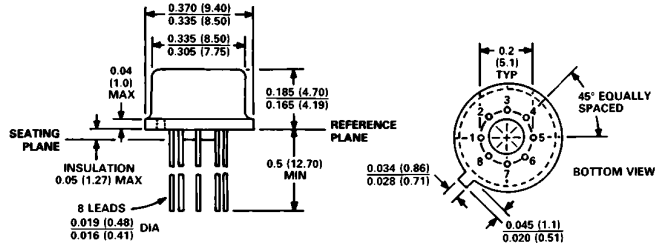
## SELECTION OF PASSIVE COMPONENTS

To take full advantage of the high precision and low drift characteristics of the AD708, high quality passive components must be used. Discrete resistors and resistor networks with temperature coefficients of less than  $10 \text{ ppm}/^\circ\text{C}$  are available from Vishay, Caddock, PRP and others.

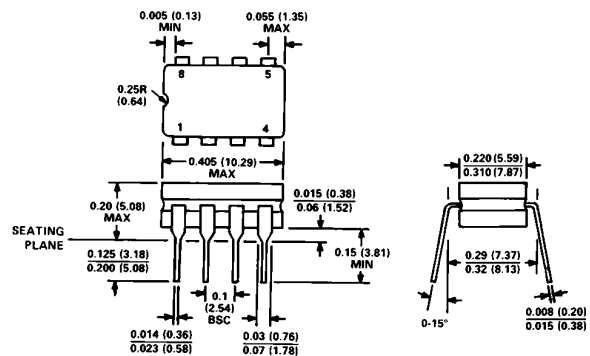
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### TO-99 (H) Package



### Cerdip (Q) Package



### Mini-DIP (N) Package

