1.6 V, Micro-Power, 8/10/12-Bit ADCs in 6 Lead SOT-23

Preliminary Technical Data — AD7466/AD7467/AD7468

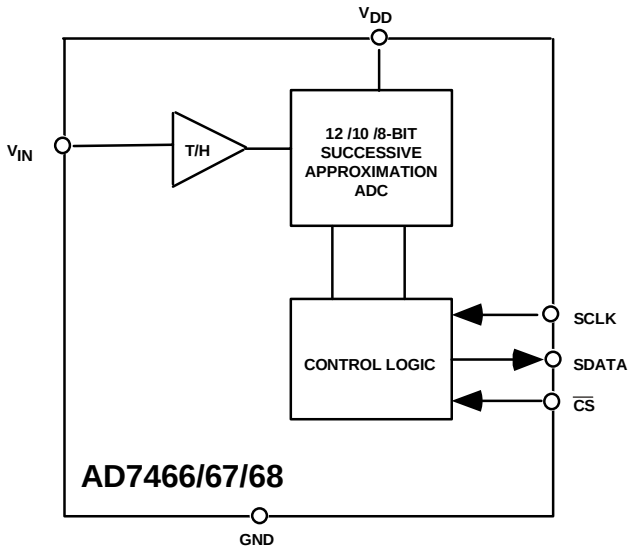
FEATURES

Specified for V_{DD} of 1.6 V to 3.6 V
Low Power:
0.62 typ mW at 100 kSPS with 3V Supplies
0.48 typ mW at 50 kSPS with 3.6 V Supplies
0.12 typ mW at 100 kSPS with 1.6V Supplies
Fast Throughput Rate: 200KSPS
Wide Input Bandwidth:
71dB SNR at 30 kHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High Speed Serial Interface
SPI/QSPI/μWire/DSP Compatible
Automatic Power Down
Standby Mode: 0.5 μA max
6-Lead SOT-23 Package
8-Lead MSOP Package

APPLICATIONS

Battery Powered Systems
Medical Instruments
Remote Data Acquisition
Isolated Data Acquisition

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7466/AD7467/AD7468 are 12-/10-/8-bit, high speed, low power, successive-approximation ADCs respectively. The parts operate from a single 1.6V to 3.6V power supply and feature throughput rates up to 200kSPS. The parts contain a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of TBDkHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. There are no pipelined delays associated with the part.

The AD7466/AD7467/AD7468 use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the part is taken internally from V_{DD}. This allows the widest dynamic input range to the ADC. Thus the analog input range for the part is 0 to V_{DD}. The conversion rate is determined by the SCLK.

PRODUCT HIGHLIGHTS

1. Specified for Supply voltages of 1.6V to 3.6V.
2. 8-/10-/12-Bit ADCs in a SOT-23 package.
3. High Throughput rate with Low Power Consumption.
4. Flexible Power/Serial Clock Speed Management. The conversion rate is determined by the serial clock allowing the conversion time to be reduced through the serial clock speed increase. Automatic Power down after conversion, which allows the average power consumption to be reduced when in power down. Current consumption is 0.5μA max when in power down.
5. Reference derived from the power supply.
6. No Pipeline Delay. The part features a standard successive-approximation ADC with accurate control of the conversions via a $\overline{CS}$ input.

REV. PrF 11/02

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AD7466–SPECIFICATIONS[1] (V_{DD} = 1.6 V to 3.6 V, f_{SCLK} = 3.4 MHz, f_{SAMPLE} = 100 kSPS unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1, 2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[2]	70	dB min	
Signal-to-Noise Ratio (SNR)[2]	71	dB min	
Total Harmonic Distortion (THD)[2]	–78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	–80	dB typ	
Intermodulation Distortion (IMD)[2]			fa = 29.1 kHz, fb = 29.9 kHz
Second Order Terms	–78	dB typ	
Third Order Terms	–78	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	TBD	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[2]	±1.5	LSB max	
	±0.6	LSB typ	
Differential Nonlinearity[2]	–0.9/+1.5	LSB max	Guaranteed No Missed Codes to 12 Bits
	±0.75	LSB typ	
Offset Error[3]	±1.5	LSB max	
Gain Error[3]	±1.5	LSB max	
Total Unadjusted Error (TUE)[3]	TBD	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7(V_{DD})	V min	1.6V ≤Vdd< 2.7V
	2	V min	2.7V ≤Vdd≤ 3.6V
Input Low Voltage, V_{INL}	0.2(V_{DD})	V max	1.6V ≤Vdd< 1.8V
	0.3(V_{DD})	V max	1.8V ≤Vdd< 2.7V
	0.8	V max	2.7V ≤Vdd≤ 3.6V
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}[3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} – 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 1.6 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	4.70	µs max	16 SCLK Cycles
Throughput Rate	200	kSPS max	See Serial Interface Section
POWER REQUIREMENTS			
V_{DD}	1.6/3.6	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	TBD	µA typ	V_{DD} = 2.7V to 3.6V, SCLK On or Off
	TBD	µA typ	V_{DD} = 1.6V to 2.5V, SCLK On or Off
Normal Mode (Operational)[4]	220	µA max	V_{DD} = 3 V, f_{SAMPLE} = 100 KSPS
	110	µA typ	V_{DD} = 3 V, f_{SAMPLE} = 50 KSPS
	20	µA typ	V_{DD} = 3 V, f_{SAMPLE} = 10 KSPS
	165	µA max	V_{DD} = 2.5 V, f_{SAMPLE} = 100 KSPS
	80	µA typ	V_{DD} = 2.5 V, f_{SAMPLE} = 50 KSPS
	16	µA typ	V_{DD} = 2.5 V, f_{SAMPLE} = 10 KSPS
	100	µA max	V_{DD} = 1.8 V, f_{SAMPLE} = 100 KSPS
	50	µA typ	V_{DD} = 1.8 V, f_{SAMPLE} = 50 KSPS
	10	µA typ	V_{DD} = 1.8 V, f_{SAMPLE} = 10 KSPS

AD7466–SPECIFICATIONS[1] (V_{DD} = 1.6 V to 3.6 V, f_{SCLK} = 3.4 MHz, f_{SAMPLE} = 100 kSPS unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1, 2]	Unit	Test Conditions/Comments
POWER REQUIREMENTS *(continued)*			
Power-Down	0.5	µA max	SCLK Off
	TBD	µA max	SCLK On
Power Dissipation[5]			
Normal Mode (Operational)	0.66	mW max	V_{DD}= 3V, f_{SAMPLE}=100KSPS
	0.42	mW max	V_{DD}= 2.5V, f_{SAMPLE}=100KSPS
	0.18	mW max	V_{DD}= 1.8V, f_{SAMPLE}=100KSPS
Power-Down	TBD	µW max	V_{DD}= 3V, SCLK Off
	TBD	µW max	V_{DD}= 2.5V, SCLK Off
	TBD	µW max	V_{DD}= 1.8V, SCLK Off

NOTES
[1]Temperature ranges as follows: B Versions: –40°C to +85°C.
[2]See Terminology.
[3]Sample tested at 25°C to ensure compliance.
[4]See TPC10 Supply current vs Supply voltage.
[5]See Power Consumption section.
Specifications subject to change without notice.

AD7467–SPECIFICATIONS[1] (V_{DD} = 1.6 V to 3.6 V, f_{SCLK} = 3.4 MHz, f_{SAMPLE} = 100 kSPS unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1, 2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz Sine Wave,
Signal-to-Noise + Distortion (SINAD)[2]	61	dB min	
Total Harmonic Distortion (THD)[2]	–73	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	–74	dB max	
Intermodulation Distortion (IMD)[2]			fa = 29.1 kHz, fb = 29.9 kHz
Second Order Terms	–78	dB typ	
Third Order Terms	–78	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	TBD	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±0.9	LSB max	Guaranteed No Missed Codes to 10 Bits
Offset Error	±1	LSB max	
Gain Error	±1	LSB max	
Total Unajusted Error (TUE)	TBD	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7(V_{DD})	V min	1.6V ≤Vdd< 2.7V
	2	V min	2.7V ≤Vdd≤ 3.6V
Input Low Voltage, V_{INL}	0.2(V_{DD})	V max	1.6V ≤Vdd< 1.8V
	0.3(V_{DD})	V max	1.8V ≤Vdd< 2.7V
	0.8	V max	2.7V ≤Vdd≤ 3.6V
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}[3]	10	pF max	

AD7467–SPECIFICATIONS[1] (V_{DD} = 1.6 V to 3.6 V, f_{SCLK} = 3.4 MHz, f_{SAMPLE} = 100 kSPS unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1, 2]	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} – 0.2	V min	I_{SOURCE} = 200 µA;
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	3.52	µs max	12 SCLK Cycles with SCLK at 3.4 MHz
Throughput Rate	275	kSPS max	See Serial Interface Section
POWER REQUIREMENTS			
V_{DD}	1.6/3.6	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	TBD	µA typ	V_{DD} = 2.7V to 3.6V, SCLK On or Off
	TBD	µA typ	V_{DD} = 1.6V to 2.5V, SCLK On or Off
Normal Mode (Operational)	200	µA max	V_{DD} = 3V, f_{SAMPLE}=100 KSPS
	150	µA max	V_{DD} = 2.5V, f_{SAMPLE}=100 KSPS
	90	µA max	V_{DD} = 1.8V, f_{SAMPLE}=100 KSPS
Power-Down	0.5	µA max	SCLK Off
	TBD	µA max	SCLK On
Power Dissipation[4]			
Normal Mode (Operational)	0.6	mW max	V_{DD}= 3V, f_{SAMPLE}=100KSPS
	0.38	mW max	V_{DD}= 2.5V, f_{SAMPLE}=100KSPS
	0.17	mW max	V_{DD}= 1.8V, f_{SAMPLE}=100KSPS
Power-Down	TBD	µW max	V_{DD}= 3V, SCLK Off
	TBD	µW max	V_{DD}= 2.5V, SCLK Off
	TBD	µW max	V_{DD}= 1.8V, SCLK Off

NOTES
[1]Temperature ranges as follows: B Versions: –40°C to +85°C.
[2]See Terminology.
[3]Sample tested at 25°C to ensure compliance.
[4]See Power Consumption section.
Specifications subject to change without notice.

AD7468–SPECIFICATIONS[1] (V_{DD} = 1.6 V to 3.6 V, f_{SCLK} = 3.4 MHz, f_{SAMPLE} = 100 kSPS unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1, 2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} =30 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[2]	49	dB min	
Total Harmonic Distortion (THD)[2]	–65	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	–65	dB max	
Intermodulation Distortion (IMD)[2]			fa = 29.1 kHz, fb = 29.9 kHz
Second Order Terms	–68	dB typ	
Third Order Terms	–68	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	TBD	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	8	Bits	
Integral Nonlinearity	±0.5	LSB max	
Differential Nonlinearity	±0.5	LSB max	Guaranteed No Missed Codes to 8 Bits
Offset Error	±0.5	LSB max	
Gain Error	±0.5	LSB max	
Total Unadjusted Error (TUE)	±0.5	LSB max	

AD7468–SPECIFICATIONS[1] (V_{DD} = 1.6 V to 3.6 V, f_{SCLK} = 3.4 MHz, f_{SAMPLE} = 100 kSPS unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1, 2]	Unit	Test Conditions/Comments
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7(V_{DD})	V min	1.6V ≤Vdd< 2.7V
	2	V min	2.7V ≤Vdd≤ 3.6V
Input Low Voltage, V_{INL}	0.2(V_{DD})	V max	1.6V ≤Vdd< 1.8V
	0.3(V_{DD})	V max	1.8V ≤Vdd< 2.7V
	0.8	V max	2.7V ≤Vdd≤ 3.6V
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}[3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} – 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 1.6 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	2.94	µs max	10 SCLK Cycles with SCLK at 3.4 MHz
Throughput Rate	320	kSPS max	See Serial Interface Section
POWER REQUIREMENTS			
V_{DD}	1.6/3.6	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	TBD	µA typ	V_{DD} = 2.7V to 3.6V, SCLK On or Off
	TBD	µA typ	V_{DD} = 1.6V to 2.5V, SCLK On or Off
Normal Mode (Operational)	175	µA max	V_{DD} = 3 V, f_{SAMPLE}= 100 KSPS
	135	µA max	V_{DD} = 2.5 V, f_{SAMPLE}= 100 KSPS
	80	µA max	V_{DD} = 1.8 V, f_{SAMPLE}= 100 KSPS
Power-Down	0.5	µA max	SCLK Off
	TBD	µA max	SCLK On
Power Dissipation[4]			
Normal Mode (Operational)	0.54	mW max	V_{DD}= 3V, f_{SAMPLE}=100KSPS
	0.34	mW max	V_{DD}= 2.5V, f_{SAMPLE}=100KSPS
	0.15	mW max	V_{DD}= 1.8V, f_{SAMPLE}=100KSPS
Power-Down	TBD	µW max	V_{DD}= 3V, SCLK Off
	TBD	µW max	V_{DD}= 2.5V, SCLK Off
	TBD	µW max	V_{DD}= 1.8V, SCLK Off

NOTES
[1]Temperature ranges as follows: B Versions: –40°C to +85°C.
[2]See Terminology.
[3]Sample tested at 25°C to ensure compliance.
[4]See Power Consumption section.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +1.6 V to +3.6 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7466/AD7467/AD7468	Units	Description
f_{SCLK} [2]	10	kHz min[3]	
	3.4	MHz max	
$t_{CONVERT}$	16 x t_{SCLK}		AD7466
	12 x t_{SCLK}		AD7467
	10 x t_{SCLK}		AD7468
t_{QUIET}	TBD	ns min	Minimum Quiet Time required between Bus Relinquish and start of next conversion
t_1	TBD	ns min	Minimum $\overline{CS}$ Pulsewidth
t_2	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3[4]	TBD	ns max	Delay from $\overline{CS}$ Until SDATA 3-State Disabled
t_4[4]	TBD	ns max	Data Access Time After SCLK Falling Edge
t_5	0.4t_{SCLK}	ns min	SCLK Low Pulse Width
t_6	0.4t_{SCLK}	ns min	SCLK High Pulse Width
t_7	TBD	ns min	SCLK to Data Valid Hold Time
t_8[5]	TBD	ns max	SCLK falling Edge to SDATA High Impedance
$t_{power-up}$	TBD	µs max	Power up time from Power down.

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of TBD Volts.

[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[3]Minimum f_{sclk} at which specifications are guaranteed.

[4]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross the Vih or Vil voltage.

[5]t_8 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

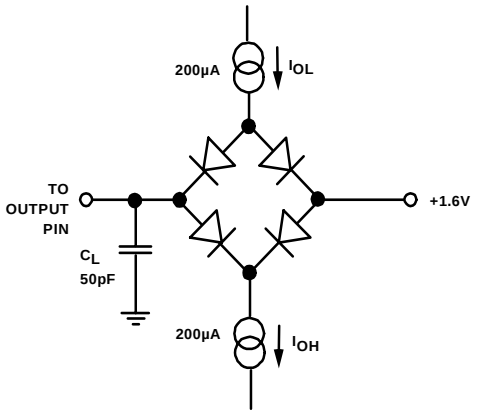


Figure 1. Load Circuit for Digital Output Timing Specifications

Figures 2 and 3 show some of the timing parameters from the Timing Specifications Section.

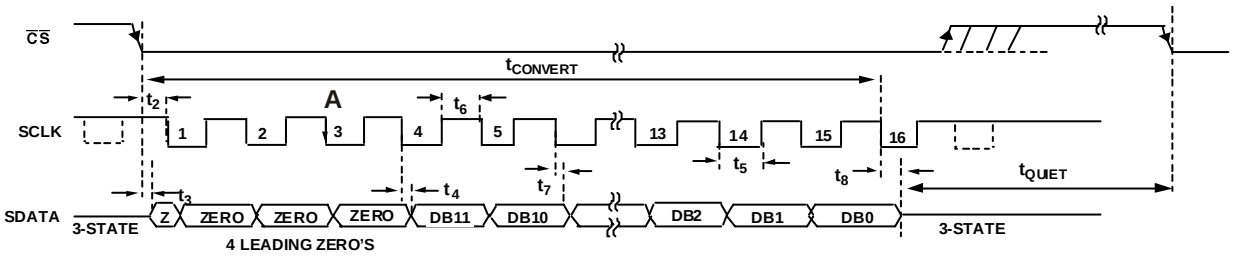


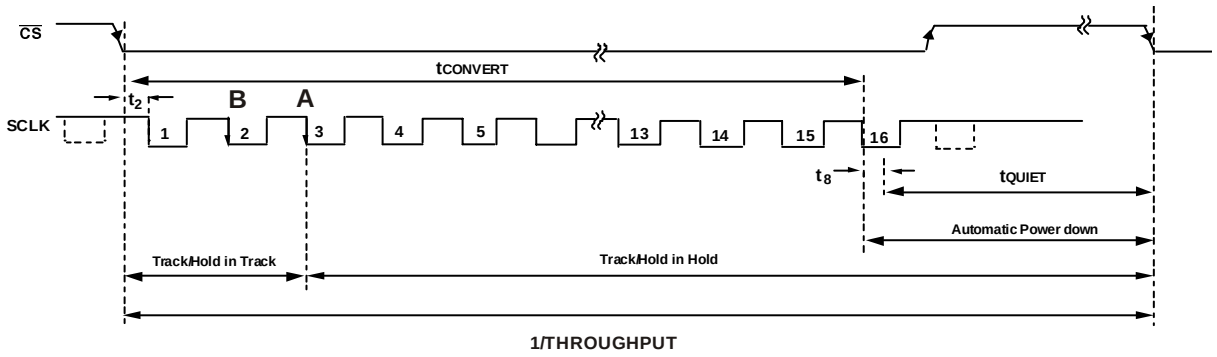
Figure 2. AD7466 Serial InterfaceTiming Diagram

Timing Example 1

From Figure 3, having f_{SCLK} = 3.4MHz and a throughput of 100 KSPS, gives a cycle time of $t_{CONVERT}$+ t_8 + t_{QUIET} = 10 µs. With $t_{CONVERT}$ = t_2 + 15(1/f_{SCLK}) = 10 ns + 4.41μs = 4.42 μs, and t_8 = TBD ns min, this leaves t_{QUIET} to be TBD ns. This TBD ns satisfies the requirement of TBD ns for t_{QUIET}. The part is fully powered up and the signal is fully acquired at point A, that means the acquisition/power up time is t_2 + 2(1/f_{SCLK}) = 10 ns + 0.588 μs = 0.59 μs satisfying the maximum requirement of TBD μs for the power up time.

Timing Example 2

The AD7466 can also operate with slower clock frequencies. From Figure 3, having f_{SCLK} = 2MHz and a throughput of 50 KSPS, gives a cycle time of $t_{CONVERT}$+ t_8 + t_{QUIET} = 20µs. With $t_{CONVERT}$ = t_2 + 15(1/f_{SCLK}) = 10 ns + 7.5μs = 7.51 μs, and t_8 = TBD ns min, this leaves t_{QUIET} to be TBD ns. This TBD ns satisfies the requirement of TBD ns for t_{QUIET}. The part is fully powered up and the signal is fully acquired at point A, that means the acquisition/power up time is t_2 + 2(1/f_{SCLK}) = 10 ns + 1 μs = 1.01 μs, satisfying the maximum requirement of TBD μs for the power up time. As in this example and with other slower clock values, the part will be fully powered up and the signal already be acquired before the third SCLK falling edge, however the Track and Hold will not go into hold mode until that point. In this example, the part may be powered up and the signal may be fully acquired at approximately point B in Figure 3.



Point A: The part is fully powered up with V_{IN} fully acquired

Figure 3. Serial InterfaceTiming Example

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

V_{DD} to GND.....–0.3 V to TBD V
Analog Input Voltage to GND.....–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND.....–0.3 V to 7 V
Digital Output Voltage to GND....–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] .....±10 mA
Operating Temperature Range
Commercial (A, B Version).....–40°C to +85°C
Storage Temperature Range.....–65°C to +150°C
Junction Temperature.....+150°C
SOT-23 Package
θ_{JA} Thermal Impedance.....229.6°C/W
θ_{JC} Thermal Impedance.....91.99°C/W
MSOP Package
θ_{JA} Thermal Impedance.....205.9°C/W
θ_{JC} Thermal Impedance.....43.74°C/W
Lead Temperature, Soldering
Vapor Phase (60 secs).....+215°C
Infared (15 secs).....+220°C
ESD.....TBD KV

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Option[2]	Branding Information
AD7466BRT	–40°C to +85°C	±1.5 max	RT-6	CLB
AD7466BRM	–40°C to +85°C	±1.5 max	RM-8	CLB
AD7467BRT	–40°C to +85°C	±1 max	RT-6	CMB
AD7467BRM	–40°C to +85°C	±1 max	RM-8	CMB
AD7468BRT	–40°C to +85°C	±0.5 max	RT-6	CNB
AD7468BRM	–40°C to +85°C	±0.5 max	RM-8	CNB
EVAL-AD7466CB[3]				
EVAL-AD7467CB[3]				
EVAL-CONTROL BRD2[4]				

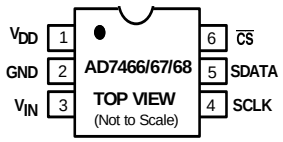
NOTES
[1]Linearity error here refers to integral nonlinearity.
[2]RT = SOT-23, RM = MSOP.
[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demostration purposes.
[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete Evaluation Kit you will need to order the particular ADC evaluation board, e.g. EVAL-AD7466CB, the EVAL-CONTROL BRD2 and a 12V AC transformer. See relevant Evaluation Board Technical Note for more information.

CAUTION

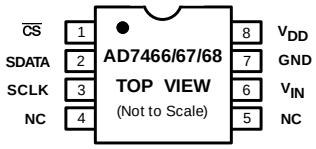
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7466/AD7467/AD7468 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD7466/67/68 PIN CONFIGURATION

6-Lead SOT-23



8-Lead MSOP



PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7466/AD7467/AD7468 and also frames the serial data transfer.
V_{DD}	Power Supply Input. The V_{DD} range for the AD7466/AD7467/AD7468 is from +1.6V to +3.6V.
GND	Analog Ground. Ground reference point for all circuitry on the AD7466/AD7467/AD7468. All analog input signals should be referred to this GND voltage.
V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 to V_{DD}.
SDATA	Data Out. Logic Output. The conversion result from the AD7466/AD7467/AD7468 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7466 consists of four leading zeros followed by the 12 bits of conversion data which is provided MSB first. The data stream from the AD7467 consists of four leading zeros followed by the 10 bits of conversion data, which is provided MSB first. The data stream from the AD7468 consists of four leading zeros followed by the 8 bits of conversion data, which is provided MSB first.
SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7466/AD7467/AD7468's conversion process.
NC	No connect.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7466/67/68 the endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 1 LSB.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time
The Track/Hold acquisition time is the time required for the part to acquire a worse case input value within ±0.5 LSB. For the AD7466/67/68 the part enters Track mode on the $\overline{CS}$ falling edge and it returns to Hold mode on the third SCLK falling edge. The part remains in Hold mode until the following $\overline{CS}$ falling edge. See Figure 3 and the Serial interface section for more details.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter this is 62dB.

Total Unadjusted Error
This is a comprehensive specification which includes gain error, linearity error and offset error.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7466/AD7467/AD7468, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7466/AD7467/AD7468 are tested using the CCIF standard where two input frequencies are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PERFORMANCE CURVES

Dynamic Performance curves

TPC 1, TPC 2 and TPC 3 show a typical FFT plot for the AD7466, AD7467 and AD7468 respectively, at 100KSPS sample rate and 30 KHz input frequency.

TPC 4 shows the Signal-to-(Noise+Distortion) Ratio performance versus Input frequency for various supply voltages while sampling at 100KSPS with a SCLK frequency of 3.4MHz for the AD7466.

TPC 5 shows the Signal to Noise Ratio (SNR) performance versus Input frequency for various supply voltages while sampling at 100KSPS with a SCLK frequency of 3.4MHz for the AD7466.

TPC 6 shows a graph of the Total Harmonic Distortion versus Analog input signal frequency for various supply voltages while sampling at 100KSPS with a SCLK frequency of 3.4MHz for the AD7466.

TPC 7 shows a graph of the Total Harmonic Distortion versus Analog input frequency for different source impedances when using a supply voltage of 2.7V, SCLK frequency of 3.4MHz and sampling at a rate of 100KSPS for the AD7466. See Analog Input section.

DC Accuracy curves

TPC 8 and TPC 9 show typical INL and DNL performance for the AD7466.

Power Requirements curves

TPC10 shows the Supply current versus Supply voltage for the AD7466 at -40°C, 25°C and 85°C, with SCLK frequency of 3.4MHz and a sampling rate of 100KSPS.

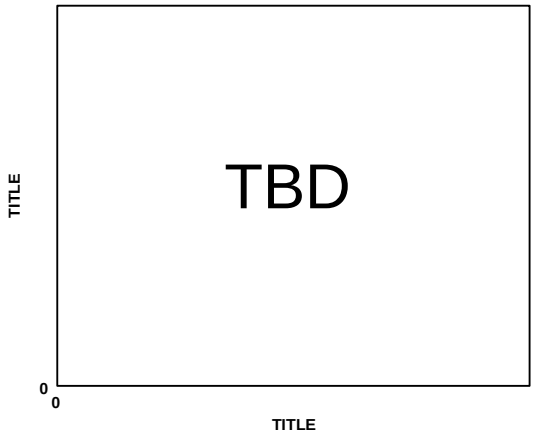
TPC11 shows the Peak current versus Supply voltage for the AD7466 with SCLK frequency of 3.4MHz.

TPC12 shows the Shutdown current versus Supply voltage

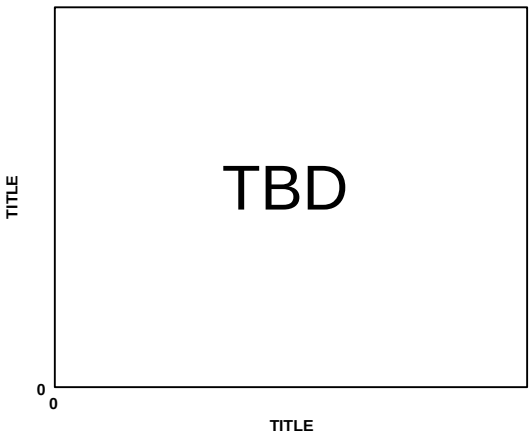
TPC13 shows the Power consumption vs Throughput rate for the AD7466 with a SCLK of 3.4MHz and different supply voltages.

See Power Consumption section for more details.

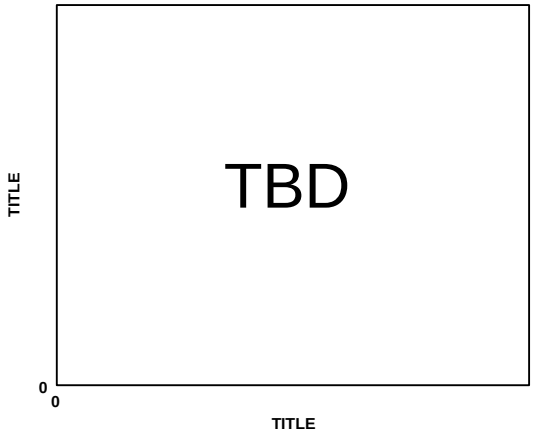
Typical Performance Characteristics



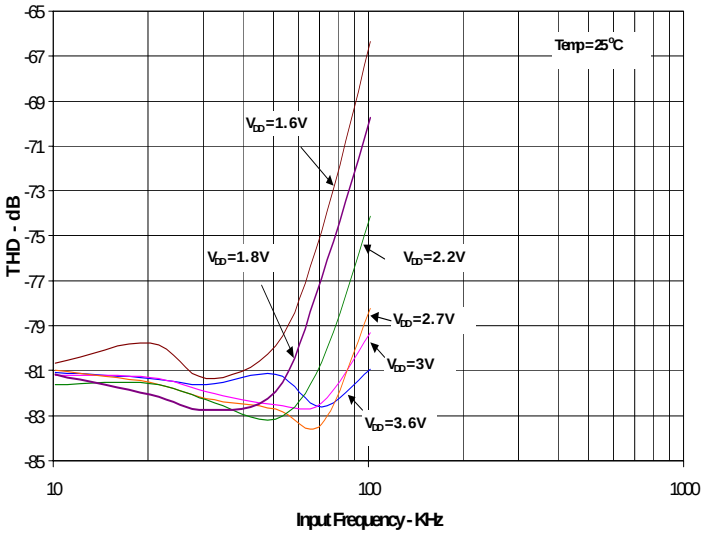
TPC 1. AD7466 Dynamic performance at 100KSPS



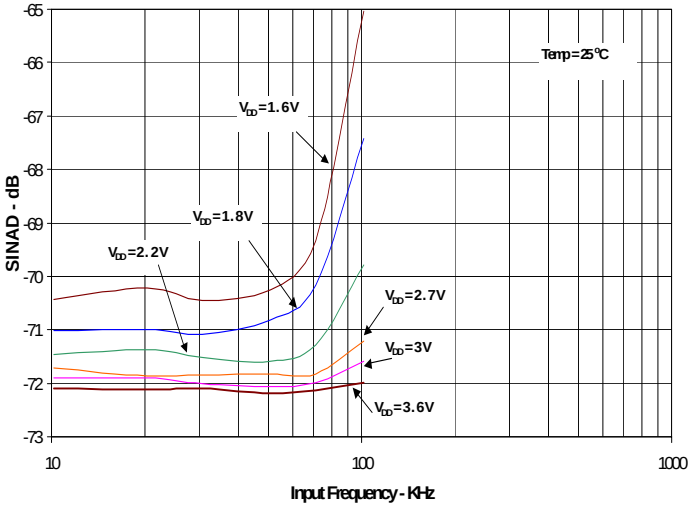
TPC 2. AD7467 Dynamic performance at 100KSPS



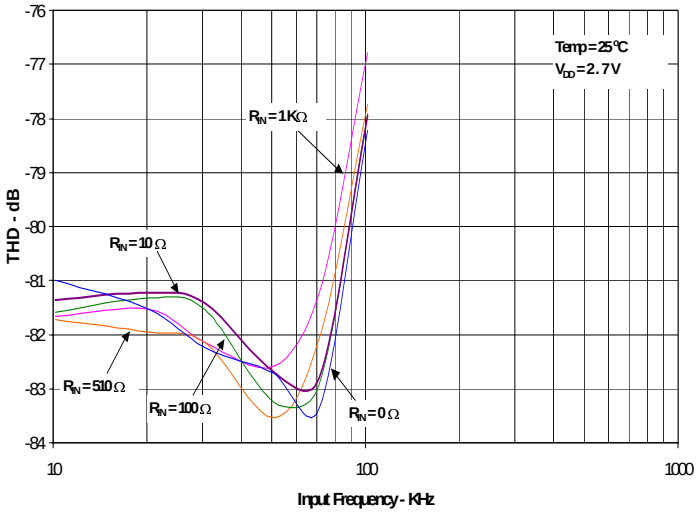
TPC 3. AD7468 Dynamic performance at 100KSPS



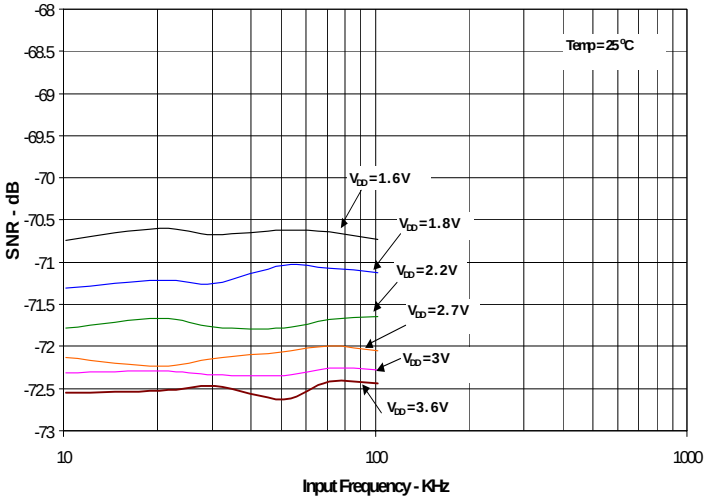
TPC 6. THD vs. Analog Input Frequency at 100KSPS for various Supply voltages



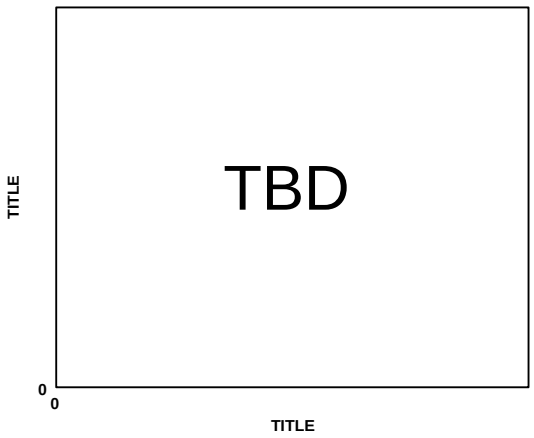
TPC 4. AD7466 SINAD vs Analog Input Frequency at 100KSPS for various Supply voltages



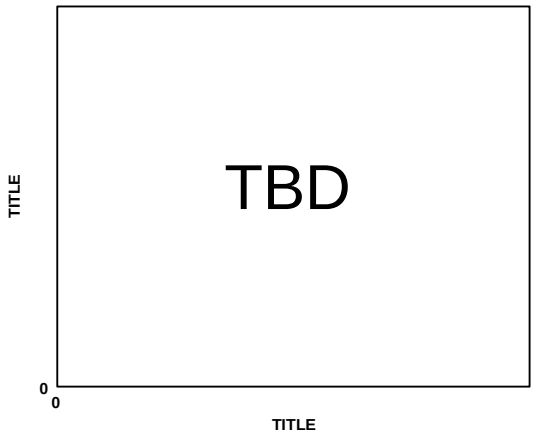
TPC 7. THD vs. Analog Input Frequency for various Source impedance



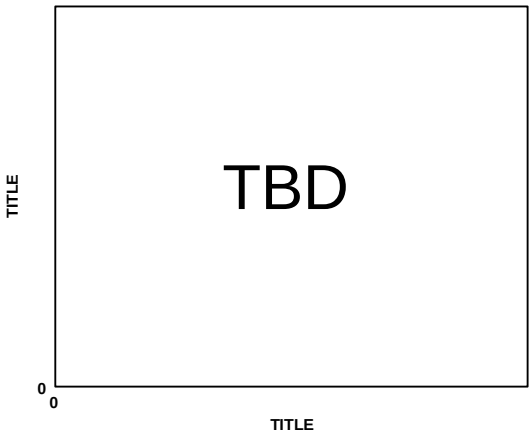
TPC 5. AD7466 SNR vs Analog Input Frequency at 100KSPS for various Supply voltages



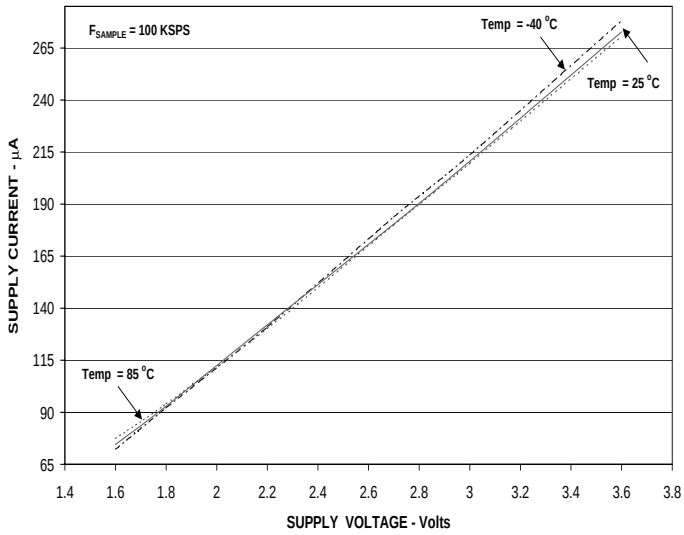
TPC 8. AD7466 INL performance



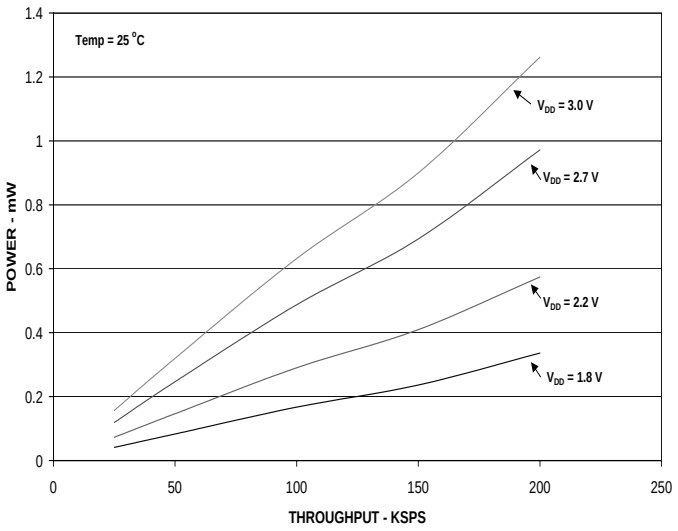
TPC 9. AD7466 DNL performance



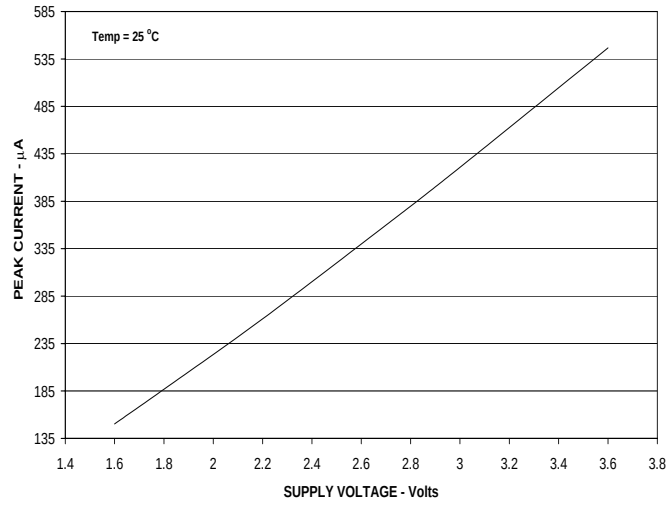
TPC 12. Shutdown current vs Supply Voltage



TPC 10. Supply current vs Supply voltage, SCLK 3.4MHz



TPC 13. Power consumption vs Throughput rate, SCLK 3.4MHz



TPC 11. Peak current vs Supply voltage, SCLK 3.4MHz

CIRCUIT INFORMATION

The AD7466/AD7467/AD7468 are fast, micro-power, 12-/10-/8-bit, A/D converters respectively. The parts can be operated from a +1.6 V to +3.6 V supply. When operated from any supply voltage within this range, the AD7466/AD7467/AD7468 is capable of throughput rates of 200kSPS when provided with a 3.4 MHz clock.

The AD7466/AD7467/AD7468 provides the user with an on-chip Track/Hold, A/D converter, and a serial interface housed in a tiny 6-lead SOT-23 or 8-lead MSOP package, which offer the user considerable space saving advantages over alternative solutions. The serial clock input accesses data from the part but also provides the clock source for the successive-approximation A/D converter. The analog input range is 0 to V_{DD}. An external reference is not required for the ADC and neither is there a reference on-chip. The reference for the AD7466/AD7467/AD7468 is derived from the power supply and thus giving the widest dynamic input range.

The AD7466/AD7467/AD7468 also features an Automatic Power-down mode option to allow power saving between conversions. The Power-down feature is implemented across the standard serial interface as described in the Mode of Operation section.

CONVERTER OPERATION

The AD7466/AD7467/AD7468 is a successive approximation analog-to-digital converter based around a charge redistribution DAC. Figures 4 and 5 show simplified schematics of the ADC. Figure 4 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

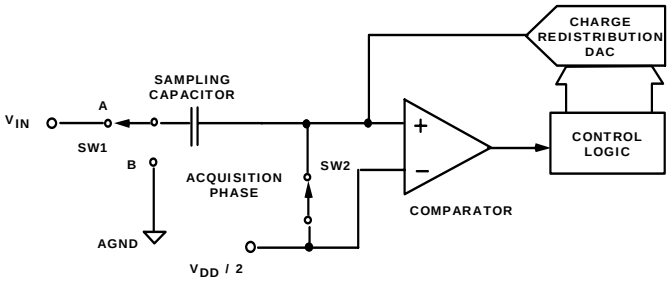


Figure 4. ADC Acquisition Phase

When the ADC starts a conversion, see Figure 5, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The control logic generates the ADC output code. Figure 6 shows the ADC transfer function.

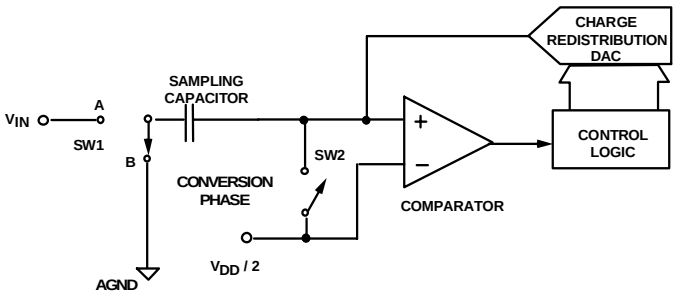


Figure 5. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7466/AD7467/AD7468 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1LSB, 2LSBs, etc.). The LSB size is $V_{DD}/4096$ for the AD7466, $V_{DD}/1024$ for the AD7467, and $V_{DD}/256$ for the AD7468 . The ideal transfer characteristic for the AD7466/AD7467/AD7468 is shown in Figure 6.

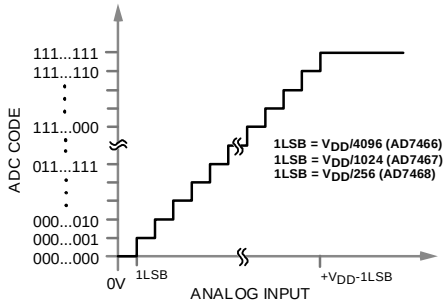


Figure 6. AD7466/AD7467/AD7468 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 7 shows a typical connection diagram for the AD7466/AD7467/AD7468. V_{REF} is taken internally from V_{DD} and therefore V_{DD} should be well decoupled. This provides an analog input range of 0V to V_{DD}.

The conversion result consists of four leading zeros followed by the MSB of the 12-bit, 10-bit or 8-bit result from the AD7466, AD7467 or AD7468 respectively. See Serial Interface section.

Alternatively, because the supply current required by the AD7466/AD7467/AD7468 is so low, a precision reference can be used as the supply source to the AD7466/AD7467/ AD7468.

The REF19X Series are precision micropower, low dropout voltage references. For the AD7466/67/68 voltage range operation, the REF193 for 3V, REF192 for 2.5 V and REF191 for 2.048V can be used to supply the required voltage to the ADC - see Figure 7. This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 3V or 2.5V (e.g. 5V). The REF19x will output a steady voltage to the AD7466/AD7467/AD7468. If the low dropout REF191 is used, the current it needs to supply to the AD7466/AD7467/AD7468 is typically TBDμA. When the ADC is converting at a rate of 100KSPS the REF191 will need to supply a maximum of 150μA to the AD7466/AD7467/AD7468. The load regulation of the REF191 is typically 10 ppm/mA (REF191, V_S= 5V), which results in an error of 1.5 ppm (3.07μV) for the 150μA drawn from it. This corresponds to a 0.0061 LSB error for the AD7466 with V_{DD}= 2.048V from the REF191, a 0.0015 LSB error for the AD7467, and a 0.00038 LSB error for the AD7468. For applications where power consumption is important, the Automatic Power down mode of the ADC and the sleep mode of the REF19x reference should be used to improve power performance. See Mode of Operation section of the datasheet.

Table I provides some typical performance data with various references used as a V_{DD} source with a low frequency analog input under the same set-up conditions.

Reference Tied To V_{DD}	AD7466 SNR performance 10kHz Input
REF191@2.048V	TBD dB
ADR420	TBD dB
REF192@2.5	TBD dB
AD780	TBD dB
REF43	TBD dB
ADR421	TBD dB
REF193@3V	TBD dB
AD780	TBD dB
ADR423	TBD dB

Table I. AD7466 performance for various Voltage References IC.

Analog Input

Figure 8 shows an equivalent circuit of the analog input structure of the AD7466/AD7467/7468. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300mV. This will cause these diodes to become forward biased and start conducting current into the substrate. The capacitor C1 in Figure 8 is typically about 4pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 200Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 16pF typically.

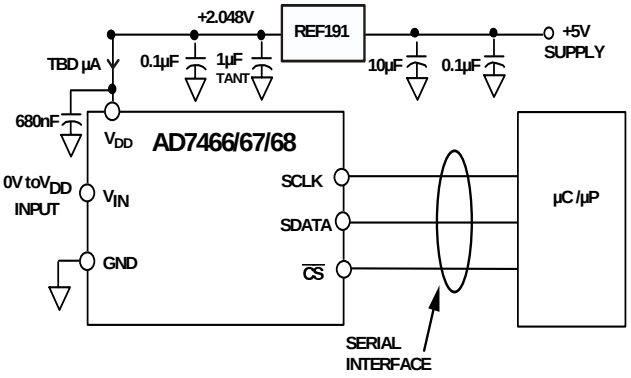


Figure 7. REF191 as Power Supply to AD7466/AD7467/AD7468

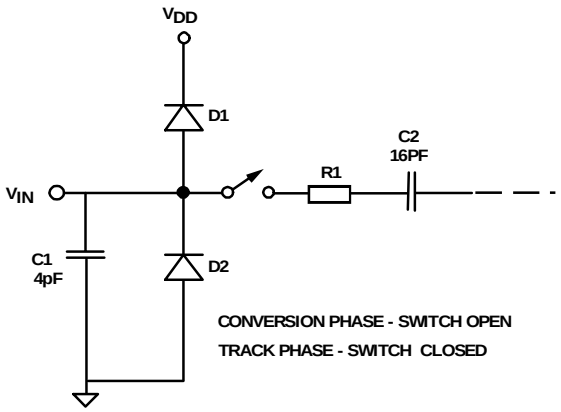


Figure 8. Equivalent Analog Input Circuit

For ac applications, removing high frequency components from the analog input signal is recommended by use of a band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal to noise ratio are critical the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

Table II provides some typical performance data with various op amps used as the input buffer with a low frequency analog input under the same set-up conditions.

Op amp in the input buffer	AD7466 SNR Performance 10kHz Input
AD711	TBD dB
AD820	TBD dB
AD8631	TBD dB

Table II. AD7466 performance for various Input Buffers.

The AD8631 low power op-amp is ideal for battery-powered applications. It works from single supply voltages as low as 1.8V, it has low supply current and the small package, 5-lead SOT-23, offers considerable space saving advantages.

When no amplifier is used to drive the analog input the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. TPC7 shows a graph of the Total Harmonic Distortion vs. Analog input signal frequency for different source impedances when using a supply voltage of TBDV and sampling at a rate of 100 kSPS.

Digital Inputs

The digital inputs applied to the AD7466/AD7467/AD7468 are not limited by the maximum ratings which limit the analog inputs. Instead, the digitals inputs applied can go to 7V and are not restricted by the V_{DD} + 0.3V limit as on the analog input. For example, if the AD7466/AD7467/AD7468 were operated with a V_{DD} of 3V then 5V logic levels could be used on the digital inputs. However, it is important to note that the data output on SDATA will still have 3V logic levels when V_{DD}= 3V. Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3V limit is the fact that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK are applied before V_{DD} then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3V was applied prior to V_{DD}.

MODE OF OPERATION

The AD7466/AD7467/AD7468 automatically enters power down at the end of each conversion. This mode of operation is designed to provide flexible power management options and to optimize the power dissipation/throughput rate ratio for low power applications requirements. Figure 9 shows the general diagram of the operation for the AD7466/AD7467/AD7468. On the $\overline{CS}$ falling edge the part begins to power up and the Track and Hold, which was in hold while the part was in power down, will go into track mode. The conversion is also initiated at this point. When operating the part with a 3.4 MHz clock it will take 2 clock cycles to fully power up the part and acquire the input signal. On the third SCLK falling edge after the $\overline{CS}$ falling edge the Track and Hold will return to hold mode.

For the AD7466 sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. The AD7466 will automatically enter power down mode on the 16th SCLK falling edge.
For the AD7467 fourteen serial clock cycles are required to complete the conversion and access the complete conversion result. The AD7467 will automatically enter power down mode on the 14th SCLK falling edge.

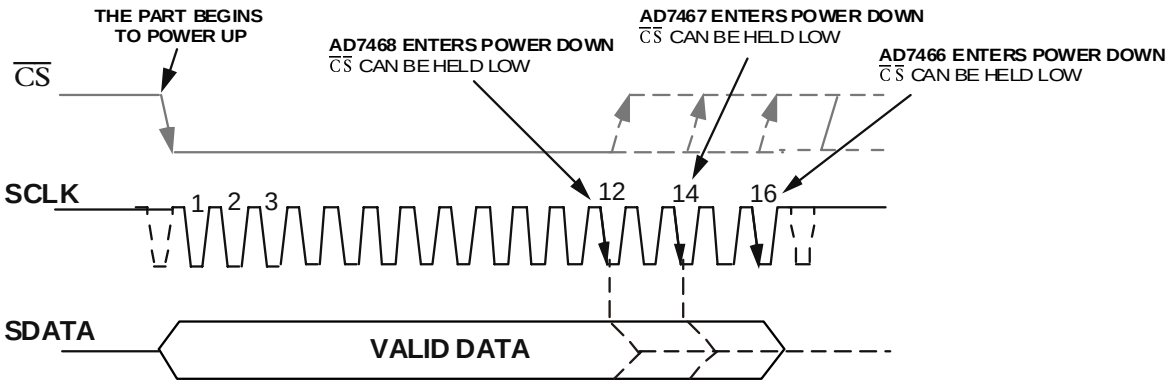


Figure 9. Normal Mode Operation

For the AD7468 twelve serial clock cycles are required to complete the conversion and access the complete conversion result. The AD7468 will automatically enter power down mode on the 12th SCLK falling edge.

The AD7466 will also enter power down mode, if $\overline{CS}$ is brought high any time before the 16th SCLK falling edge. The conversion that was initiated by the $\overline{CS}$ falling edge will be terminated and SDATA will go back into three-state. This also applies for the AD7467 and AD7468, if $\overline{CS}$ is brought high before the conversion is complete (the 14th SCLK falling edge for the AD7467, and the 12th SCLK falling edge for the AD7468) the part will enter power down, the conversion will be terminated and SDATA will go back into three-state.
When supplies are first applied to the AD7466/AD7467/AD7468 a dummy conversion should be performed to ensure that the part is in power down mode.

$\overline{CS}$ may idle high until the next conversion or may idle low until $\overline{CS}$ returns high sometime prior to the next conversion, (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{quiet}, has elapsed by bringing $\overline{CS}$ low again.

POWER CONSUMPTION

The AD7466/67/68 automatically enters power down mode at the end of each conversion or if $\overline{CS}$ is brought high before the conversion is finished.

When the AD7466/67/68 is in power down mode all the analog circuitry is powered down and the current consumption is typically TBD μA.

To achieve the lowest power dissipation, there are some considerations the user should bear in mind.

The conversion time is determined by the serial clock frequency. The faster the SCLK frequency, the shorter the conversion time. This implies as the frequency increases the part will be dissipating power for a shorter period of time, when the conversion is taking place, and it will remain in power down mode for a longer period of time.

Figure 10 shows two AD7466 running with two different SCLK frequencies, SCLK A and SCLK B, SCLK A having the higher SCLK frequency. For the same throughput rate, the AD7466 using SCLK A will have a shorter conversion time than the AD7466 using SCLK B and it will remain in power down mode for longer. The current consumption in power down mode is very low, and the average power consumption will be greatly reduced.

This can be seen in Figure 11. This figure shows the Supply current versus SCLK frequency for various supply voltages at a throughput rate of 100KSPS. For a fixed throughput rate, the supply current (average current) will drop as the SCLK frequency increases, due to the fact that the part will be in power down mode most of the time. It can also be seen, that for a lower supply voltage the supply current drops accordingly.

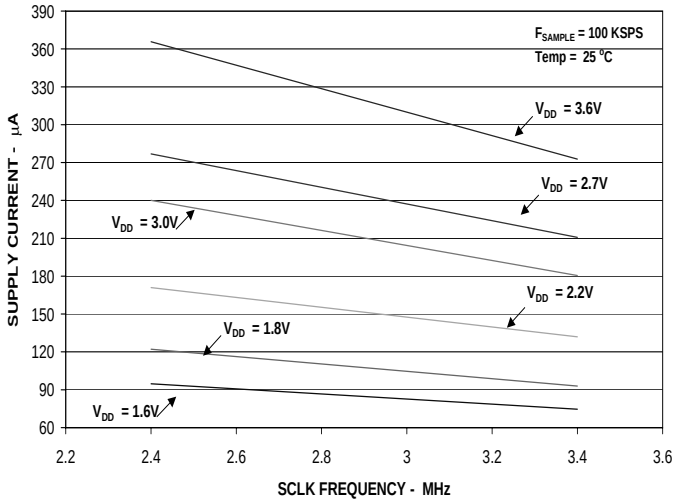


Figure 11. Supply current vs SCLK frequency for a fixed throughput rate and different supply voltages

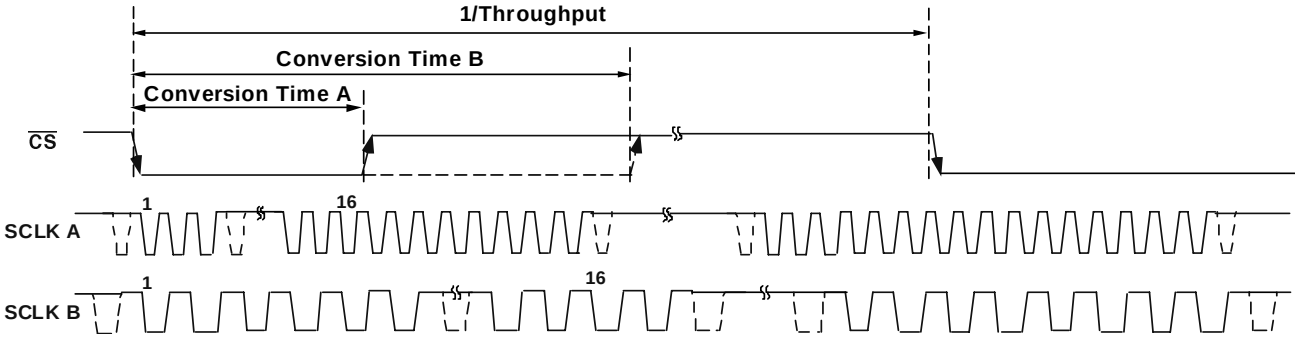


Figure 10. Conversion Time comparison for different SCLK frequencies for a fixed Throughput rate

TPC14 in the Performance Curves section, shows Power consumption versus Throughput rate for a 3.4MHz SCLK frequency. In this case the conversion time will be the same for all the cases, as the SCLK frequency is a fixed parameter. Low throughput rates will lead to lower current consumptions, with a higher percentage of the time in power down mode. Figure 12 shows two AD7466 running with the same SCLK frequency but at different throughput rates. The throughput rate for the AD7466 called A is higher than for the AD7466 called B. The slower the throughput rate, the longer the period of time the part will be in power down mode, and the average power consumption will drop accordingly.

Figure 13 shows Power versus Throughput rate for different supply voltages and SCLK frequencies. In this plot all the elements that have been explained above, that is, the influence of the SCLK frequency, the influence of the throughput rate and the influence of the supply voltage, in the power consumption are taken into consideration.

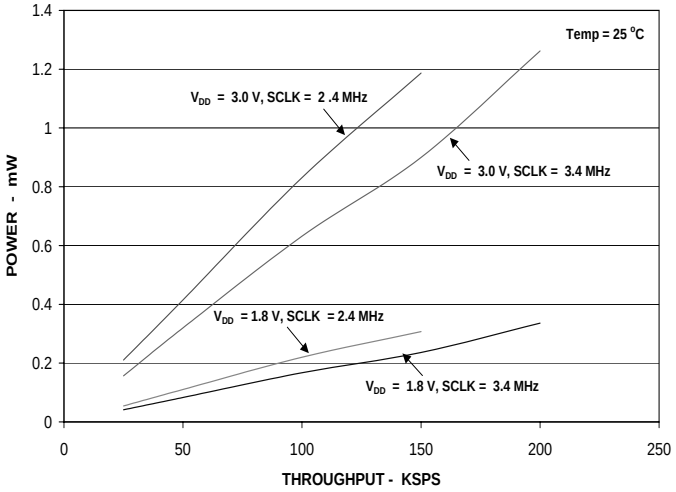


Figure 13. Power vs Throughput for different SCLK and supply voltages

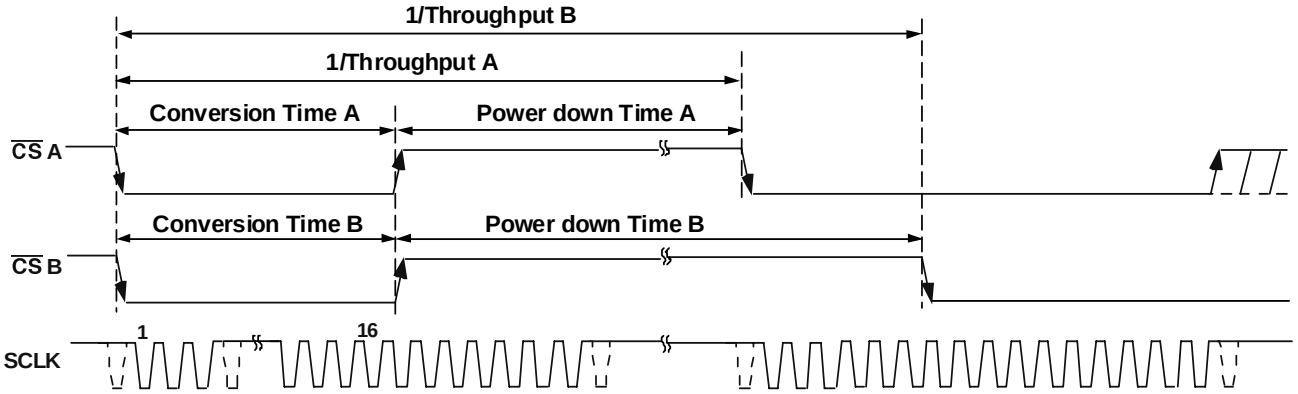


Figure 12. Conversion Time vs Power down Time for a fixed SCLK frequency and different Throughput rates

The following two examples will illustrate by means of some calculations, what has been explained in this section.

Power Consumption Example 1

This example shows that for a fixed throughput rate, as the SCLK frequency increases the average power consumption drops. From Figure 10, having SCLK A= 3.4 MHz, SCLK B= 1.2 MHz and a throughput rate of 50KSPS, which gives a cycle time of 20µs, the following values can be obtained:

Conversion time A= 16 x (1/SCLK A) = 4.7µs (23.5% of the cycle time)
Power down time A= (1/throughput) - Conversion time A = 20µs - 4.7µs = 15.3µs (76.5% of the cycle time)

Conversion time B= 16 x (1/SCLK B) = 13µs (65% of the cycle time)
Power down time B= (1/throughput) - Conversion time B = 20µs - 13µs = 7µs (35% of the cycle time)

The average power consumption includes the power dissipated when the part is converting and the power dissipated when the part is in power down mode. The average power dissipated during conversion is calculated as the percentage of the cycle time spent when converting multiplied by the peak current during conversion. The average power dissipated when in power down mode is calculated as the percentage of the cycle time spent in power down mode multiplied by the current figure for power down mode. In order to obtain the value for the average power, these terms must be multiplied by the voltage.

Considering the peak current for each SCLK frequency for V_{DD}= 1.8V,

Power consumption A= ((4.7/20) x 186µA + (15.3/20) x 1µA) x 1.8V = (43.71+0.765) µA x1.8V = 80µW = **0.08 mW**
Power consumption B= ((13/20) x 108µA + (7/20) x 1µA) x 1.8V = (70.2+0.35) µA x1.8V = 126.99µW = **0.127 mW**

It can be concluded that for a fixed throughput rate, the average power consumption drops as the SCLK frequency increases.

Power Consumption Example 2

This example shows that for a fixed SCLK frequency, as the throughput rate decreases the average power consumption drops. From Figure 12, for SCLK = 3.4 MHz, Throughput A = 100KSPS (which gives a cycle time of 10µs) and Throughput B = 50KSPS (which gives a cycle time of 20µs) the following values can be obtained:

Conversion time A= 16 x (1/SCLK) = 4.7µs (47% of the cycle time for a throughput of 100KSPS)
Power down time A= (1/throughput A) - Conversion time A = 10µs - 4.7µs = 5.3µs (53% of the cycle time)

Conversion time B= 16 x (1/SCLK) = 4.7µs (23.5% of the cycle time for a throughput of 50KSPS)
Power down time B= (1/throughput B) - Conversion time B = 20µs - 4.7µs = 15.3µs (76.5% of the cycle time)

The average power consumption is calculated as it has been explained in the Power Consumption Example1, considering the peak current for a 3.4MHz SCLK frequency for V_{DD}= 1.8V.

Power consumption A= ((4.7/10) x 186µA + (5.3/10) x 1µA)x 1.8V= (87.42+0.53)µA x1.8V= 158.3µW= **0.156 mW**
Power consumption B= ((4.7/20) x 186µA + (15.3/20) x 1µA) x 1.8V= (43.7+0.765)µA x1.8V = 80µW = **0.08 mW**

It can be concluded that for a fixed SCLK frequency, the average power consumption drops as the throughput rate decreases.

SERIAL INTERFACE

Figures 14, 15, 16 show the detailed timing diagram for serial interfacing to the AD7466/AD7467/AD7468.The serial clock provides the conversion clock and also controls the transfer of information from the ADC during a conversion.

On the $\overline{CS}$ falling edge the part begins to power up. The falling edge of $\overline{CS}$ puts the Track and Hold into track mode and takes the bus out of three-state. The conversion is also initiated at this point. On the third SCLK falling edge after the $\overline{CS}$ falling edge, the part should be fully powered up, as shown in Figure 14 at point B, and the Track and Hold will return to hold.

For the AD7466, on the 16th SCLK falling edge the SDATA line will go back into three-state and the part will enter power down. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed then the conversion will be terminated, the SDATA line will go back into three-state and the part will enter power down, otherwise SDATA returns to three-state on the 16th SCLK falling edge as shown in Figure 14. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7466.

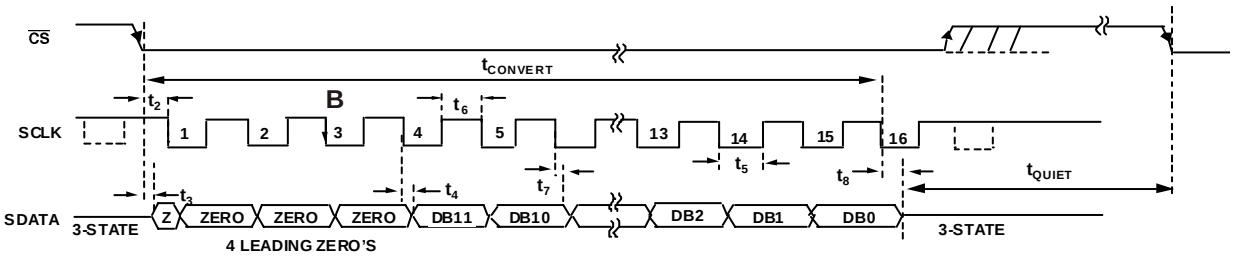


Figure 14. AD7466 Serial Interface Timing Diagram

For the AD7467, the 14th SCLK falling edge will cause the SDATA line to go back into three-state and the part will enter power down. If the rising edge of $\overline{CS}$ occurs before 14 SCLKs have elapsed then the conversion will be terminated, the SDATA line will go back into three-state and the AD7467 will enter power down, otherwise SDATA returns to three-state on the 14th SCLK falling edge as shown in Figure 15. Fourteen serial clock cycles are required to perform the conversion process and to access data from the AD7467.

For the AD7468, the 12th SCLK falling edge will cause the SDATA line to go back into three-state and the part will enter power down. If the rising edge of $\overline{CS}$ occurs before 12 SCLKs have elapsed then the conversion will be terminated, the SDATA line will go back into three-state and the AD7468 will enter power down, otherwise SDATA returns to three-state on the 12th SCLK falling edge as shown in Figure 16. Twelve serial clock cycles are required to perform the conversion process and to access data from the AD7468.

$\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the 2nd leading zero, thus the first clock falling edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. For the AD7466 the final bit in the data transfer is valid on the 16th SCLK falling edge, having being clocked out on the previous (15th) SCLK falling edge.

In applications with a slow SCLK, it is possible to read in data on each SCLK rising edge. In that case, the first falling edge of SCLK will clock out the second leading zero and it could be read in the first rising edge. However, the first leading zero that was clocked out when $\overline{CS}$ went low will be missed unless it was not read in the first falling edge. The 15th falling edge of SCLK will clock out the last bit and it could be read in the 15th rising SCLK edge.

If $\overline{CS}$ goes low just after one the SCLK falling edge has elapsed, $\overline{CS}$ will clock out the first leading zero as before and it may be read in the SCLK rising edge. The next SCLK falling edge will clock out the second leading zero and it could be read in the following rising edge.

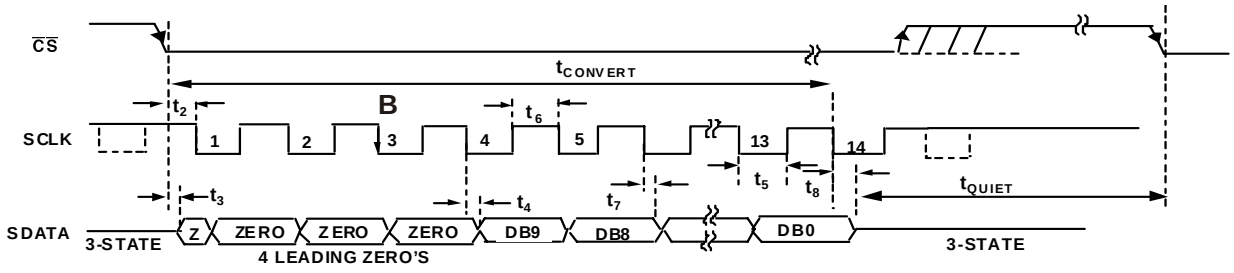


Figure 15. AD7467 Serial Interface Timing Diagram

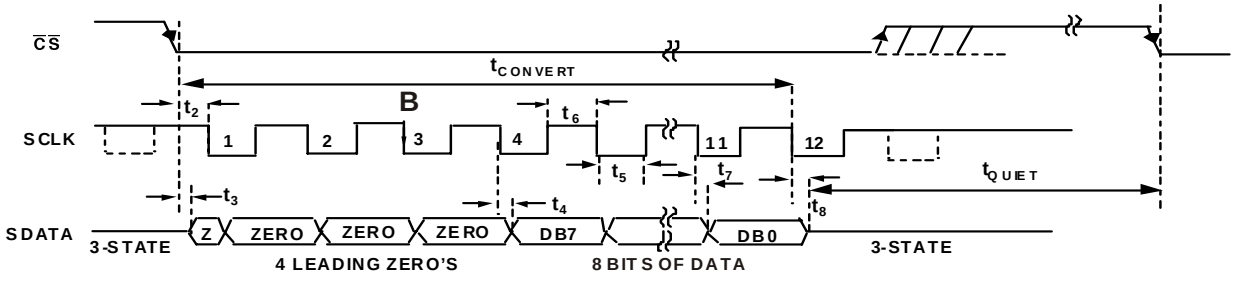


Figure 16. AD7468 Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7466/AD7467/AD7468 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7466/AD7467/AD7468 with some of the more common microcontroller and DSP serial interface protocols.

AD7466/67/68 to TMS320C541 Interface

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7466/67/68. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7466/67/68 without any glue logic required. The serial port of the TMS320C541 is set up to operate in burst mode (FSM=1 in the Serial Port Control register, SPC) with internal CLKX (MCM=1 in the SPC register) and interanl frame signal (TXM = 1 in the SPC register), so both pins are configured as outputs. For the AD7466 the word length should be set to 16 bits (FO=0 in the SPC register). This DSP only allows frames with a word length of 16 or 8 bits. Therefore, for the AD7467 and AD7468 where 14 and 12 bits are required, the FO bit would be set up to 16 bits also. In these cases, the user should keep in mind that, the last two and four bits for the AD7467 and AD7468 respectively, will be invalid data as the SDATA line goes back into three-state on the 14th and 12th SCLK falling edge.

To summarise, the values in the SPC register are:

FO=0
FSM=1
MCM=1
TXM=1

The connection diagram is shown in Figure 17. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the TMS320C541 will provide equidistant sampling.

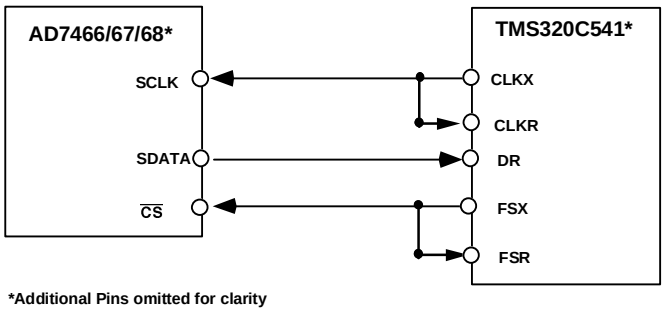


Figure 17. Interfacing to the TMS320C541

AD7466/67/68 to ADSP218x

The ADSP218x family of DSPs are interfaced directly to the AD7466/67/68 without any glue logic required. The SPORT control register should be set up as follows:

TFSW= RFSW= 1, Alternate Framing
INVRFS= INVTFS= 1, Active Low Frame Signal
DTYPE= 00, Right Justify Data
ISCLK= 1, Internal Serial Clock
TFSR= RFSR= 1, Frame Every Word
IRFS= 0, it sets up RFS as an Input
ITFS= 1, it sets up TFS as an Output
SLEN= 1111, 16 bits for the AD7466
SLEN= 1101, 14 bits for the AD7467
SLEN= 1011, 12 bits for the AD7468

The connection diagram is shown in Figure 18. The ADSP218x has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in Alternate Framing Mode and the SPORT control register is set up as described. The frame synchronisation signal generated on the TFS is tied to $\overline{CS}$ and as with all signal processing applications equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and, under certain conditions, equidistant sampling may not be achieved.

The timer registers etc., are loaded with a value which will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, i.e. AX0= TX0, the state of the SCLK is checked. The DSP will wait until the SCLK has gone high, low and high before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP2111 has a master clock frequency of 16MHz. If the SCLKDIV register is loaded with the value 3 then a SCLK of 2MHz is obtained, and 8 master clock periods will elapse for every one SCLK period. If the timer registers are loaded with the value 803, 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in non-equidistant sampling as the transmit instruction is occuring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N then equidistant sampling will be implemented by the DSP.

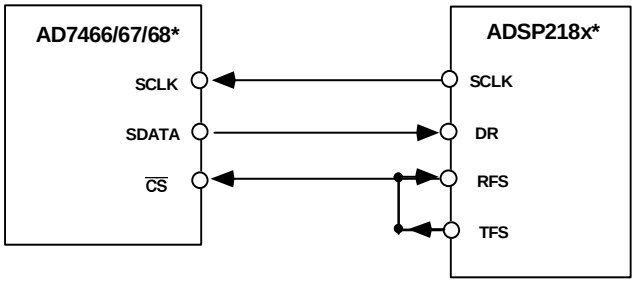


Figure 18. Interfacing to the ADSP218x

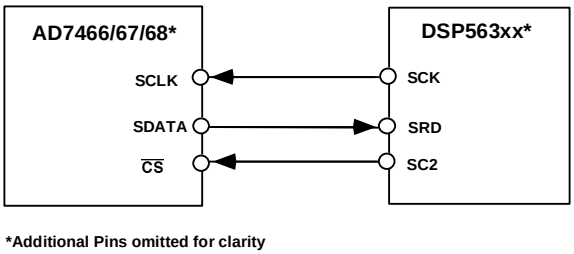


Figure 19. Interfacing to the DSP563xx

AD7466/67/68 to DSP563xx Interface
The connection diagram in Figure 19 shows how the AD7466/67/68 can be connected to the SSI (Synchronous Serial Interface) of the DSP563xx family of DSPs from Motorola. The SSI is operated in Synchronous and Normal Mode (SYN=1 and MOD=0 in the Control Register B, CRB) with internally generated 1-bit clock period frame sync for both Tx and Rx (bits FSL1=1 and FSL0=0 in the CRB). Set the word length in the Control Register A (CRA) to 16 by setting bits WL2=0, WL1=1 and WL0=0 for the AD7466. The word length for the AD7468 can be set to 12 bits (WL2=0, WL1=0 and WL0=1). This DSP does not offer the option for a 14 bits word length, so the AD7467 word length will be set up to 16 bits like the AD7466. In this case, the user should bear in mind that the last two bits will be invalid data as the SDATA goes back into three-state on the 14th SCLK falling edge.

The FSP bit in the CRB register can be set to 1, that means that the frame goes low and a conversion starts. Likewise, by means of the bits SCD2, SCKD and SHFD in the CRB register, it will be established that the pin SC2 (the frame sync signal) and SCK in the serial port will be configured as outputs and the MSB will be shifted first. To sum up,

MOD=0
SYN=1
WL2, WL1, WL0 depend on the word length
FSL1=1, FSL0=0
FSP=1, negative frame sync
SCD2=1
SCKD=1
SHFD=0

It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the DSP563xx will provide equidistant sampling.

APPLICATION HINTS

Grounding and Layout

The printed circuit board that houses the AD7466/67/68 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined at only one place. If the AD7466/67/68 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD7466/67/68.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7466/67/68 to avoid noise coupling. The power supply lines to the AD7466/67/68 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also very important. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND. All digital supplies should have a 0.1 µF disc ceramic capacitor to DGND. To achieve the best performance from these decoupling components, the user should endeavour to keep the distance between the decoupling capacitor and the V_{DD} and GND pins to a minimum with short track lenghts connecting the respective pins.

Evaluating the AD7466/67 Performance

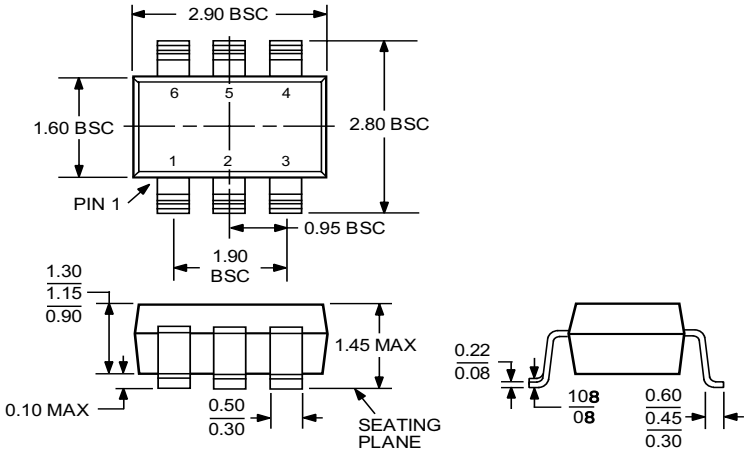
The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the EVAL-BOARD CONTROLLER. The EVAL-BOARD CONTROLLER can be used in conjunction with the AD7466/67CB Evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7466/67.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7466/67. See the evaluation board technical note for more information.

OUTLINE DIMENSIONS

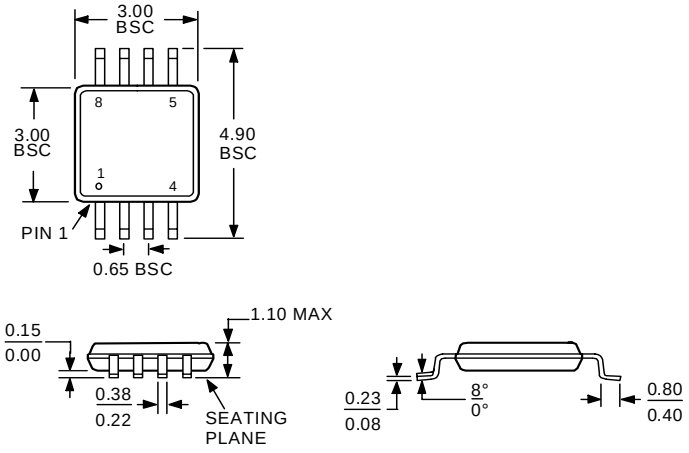
Dimensions shown in millimeters

6-lead SOT23 (RJ-6)



COMPLIANT TO JEDEC STANDARDS MO-178AB

8-lead MSOP (RM-8)



COMPLIANT TO JEDEC STANDARDS MO-187AA