1.8 V, Micro-Power, 8/10/12-Bit ADCs in 6 Lead SOT-23

Preliminary Technical Data AD7466/AD7467/AD7468

FEATURES

Specified for V_{DD} of 1.8 V to 3.6 V
Low Power:
0.9 mW max at 60 kSPS with 3.6 V Supplies
0.4 mW max at 100 kSPS with 1.8 V Supplies
Fast Throughput Rate: 100 kSPS

Wide Input Bandwidth:
70dB SNR at 30 kHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High Speed Serial Interface
SPI/QSPI/µWire/DSP Compatible

Standby Mode: 0.5 µA max
6-Lead SOT-23 Package and 8 lead µSOIC

APPLICATIONS

Battery Powered Systems

Medical Instruments

Ramote Data Acquisition

Isolated Data Acquisition

GENERAL DESCRIPTION

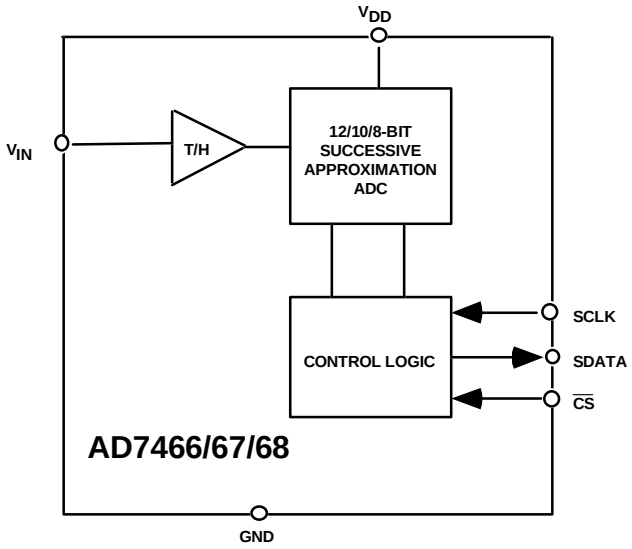
The AD7466/AD7467/AD7468 are 12/10/8-bit, high speed, low power, successive-approximation ADCs respectively. The parts operate from a single 1.8 V to 3.6 V power supply and feature throughput rates up to 100 kSPS. The parts contain a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of 100 kHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. There are no pipelined delays associated with the part.

The AD7466/AD7467/AD7468 use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the part is taken internally from V_{DD}. This allows the widest dynamic input range to the ADC. Thus the analog input range for the part is 0 to V_{DD}. The conversion rate is determined by the SCLK.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Specified for Supply voltages of 1.8 V to 3.6 V
2. 8/10/12-Bit ADCs in a SOT-23 package.
3. High Throughput with Low Power Consumption
4. Flexible Power/Serial Clock Speed Management
   The conversion rate is determined by the serial clock allowing the conversion time to be reduced through the serial clock speed increase. Automatic power down after conversion, which allows the average power cunsumption to be reduced when in powerdown. Power consumption is 0.5 µA max when in powerdown.
5. Reference derived from the power supply.
6. No Pipeline Delay
   The part features a standard successive-approximation ADC with accurate control of the conversions via a $\overline{CS}$ input.

REV. PrC 07/01

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AD7466–SPECIFICATIONS[1] (V_{DD} = 1.8 V to 3.6 V, f_{SCLK} = 2.4 MHz, f_{SAMPLE} = 100 kSPS unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1, 2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[2]	70	dB min	
Signal-to-Noise Ratio (SNR)[2]	71	dB min	
Total Harmonic Distortion (THD)[2]	–78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	–80	dB typ	
Intermodulation Distortion (IMD)[2]			fa = 29.1 kHz, fb = 29.9 kHz
Second Order Terms	–78	dB typ	
Third Order Terms	–78	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	TBD	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[2]	±1.5	LSB max	
	±0.6	LSB typ	
Differential Nonlinearity[2]	–0.9/+1.5	LSB max	Guaranteed No Missed Codes to 12 Bits
	±0.75	LSB typ	
Offset Error[3]	±1.5	LSB max	
Gain Error[3]	±1.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7(V_{DD})	V min	V_{DD} = 1.8 V to 3.6 V
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}[2,3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} – 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 1.8 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[2,3]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	6.66	µs max	Sixteen SCLK Cycles
Track/Hold Acquisition Time	TBD	ns max	Full-Scale Step Input
	TBD	ns max	Sine Wave Input
Throughput Rate	100	kSPS max	See Serial Interface Section
POWER REQUIREMENTS			
V_{DD}	1.8/3.6	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Operational)	350	µA max	V_{DD} = 3 V. SCLK On or Off
	200	µA max	V_{DD} = 1.8 V. SCLK On or Off
Power-Down	0.5	µA max	SCLK Off
	80	µA max	SCLK On
Power Dissipation[4]			
Normal Mode (Operational)	TBD	mW max	V_{DD} = 3 V. f_{SAMPLE} = TBD
		mW max	V_{DD} = 1.8 V. f_{SAMPLE} = TBD
Power-Down	1.5	µW max	V_{DD} = 3 V. SCLK Off
	0.9	µW max	V_{DD} = 1.8 V. SCLK Off

NOTES
[1]Temperature ranges as follows: B Versions: –40°C to +85°C.
[2]See Terminology.
[3]Sample tested at 25°C to ensure compliance.
[4]See Power Versus Throughput Rate section.

Specifications subject to change without notice.

AD7467–SPECIFICATIONS[1]

(V_{DD} = 1.8 V to 3.6 V, f_{SCLK} = 2.4 MHz, f_{SAMPLE} = 100 kSPS unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1, 2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz Sine Wave,
Signal-to-Noise + Distortion (SINAD)[2]	61	dB min	
Total Harmonic Distortion (THD)[2]	–73	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	–74	dB max	
Intermodulation Distortion (IMD)[2]			fa = 29.1 kHz, fb = 29.9 kHz
Second Order Terms	–78	dB typ	
Third Order Terms	–78	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	TBD	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±0.9	LSB max	Guaranteed No Missed Codes to 10 Bits
Offset Error	±1	LSB max	
Gain Error	±1	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7(V_{DD})	V min	V_{DD} = 1.8 to 3.6 V
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}[2,3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} – 0.2	V min	I_{SOURCE} = 200 µA;
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[2,3]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	5	µs max	12 SCLK Cycles with SCLK at 20 MHz
Track/Hold Acquisition Time	TBD	ns max	
Throughput Rate	100	kSPS max	See Serial Interface Section
POWER REQUIREMENTS			
V_{DD}	1.8/3.6	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Operational)	350	µA max	V_{DD} = 3 V . SCLK On or Off
	200	µA max	V_{DD} = 1.8 V . SCLK On or Off
Power-Down Mode	0.5	µA max	SCLK Off
	80	µA max	SCLK On
Power Dissipation[4]			
Normal Mode (Operational)	TBD	mW max	V_{DD} = 3 V. f_{SAMPLE} = 100 kSPS
	TBD	mW max	V_{DD} = 1.8 V. f_{SAMPLE} = TBD
Power-Down	1.5	µW max	V_{DD} = 3 V. SCLK Off
	0.9	µW max	V_{DD} = 1.8 V. SCLK Off

NOTES
[1]Temperature ranges as follows: B Versions: –40°C to +85°C.
[2]See Terminology.
[3]Sample tested at 25°C to ensure compliance.
[4]See Power Versus Throughput Rate section.
Specifications subject to change without notice.

AD7468–SPECIFICATIONS[1]

(V_{DD} = 1.8 V to 3.6 V, f_{SCLK} = 2.4 MHz, f_{SAMPLE} = 100 kSPS unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1, 2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} =30 kHz Sine Wave, f_{SAMPLE}=100kSPS
Signal-to-Noise + Distortion (SINAD)[2]	49	dB min	
Total Harmonic Distortion (THD)[2]	–65	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	–65	dB max	
Intermodulation Distortion (IMD)[2]			fa = 29.1 kHz, fb = 29.9 kHz
Second Order Terms	–68	dB typ	
Third Order Terms	–68	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	TBD	MHz typ	@ 3 dB
Full Power Bandwidth	TBD	MHz typ	@ 0.1 dB
DC ACCURACY[2]			
Resolution	8	Bits	
Integral Nonlinearity	±0.5	LSB max	
Differential Nonlinearity	±0.5	LSB max	Guaranteed No Missed Codes to 8 Bits
Offset Error	±0.5	LSB max	
Gain Error	±0.5	LSB max	
Total Unadjusted Error (TUE)	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7(V_{DD})	V min	V_{DD} = 1.8 to 3.6 V
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}[2,3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} – 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 1.8 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[3, 4]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	4.166	µs max	10 SCLK Cycles with SCLK at 2.4 MHz
Track/Hold Acquisition Time	TBD	ns max	
Throughput Rate	100	kSPS max	See Serial Interface Section
POWER REQUIREMENTS			
V_{DD}	1.8/3.6	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	350	µA max	V_{DD} = 3V. SCLK On or Off
	200	µA max	V_{DD} = 1.8 V . SCLK On or Off
Power-Down Mode	0.5	µA max	SCLK Off
	80	µA max	SCLK On
Power Dissipation[5]			
Normal Mode (Operational)	TBD	mW max	V_{DD} = 3 V. f_{SAMPLE} = TBD
	TBD	mW max	V_{DD} = 1.8 V. f_{SAMPLE} = TBD
Power-Down	1.5	µW max	V_{DD} = 3 V. SCLK Off
	0.9	µW max	V_{DD} = 1.8 V. SCLK Off

NOTES
[1]Temperature ranges as follows: B Versions: –40°C to +85°C.
[2]See Terminology.
[3]Sample tested at 25°C to ensure compliance.
[4]See Power Versus Throughput Rate section.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +1.8 V to +3.6 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD7466	Units	Description
f_{SCLK}[2]	10	kHz min	
	TBD	MHz max	
$t_{CONVERT}$	16* t_{SCLK}		
t_{quiet}	TBD	ns min	Minimum Quiet Time required between Bus Relinquish and start of next conversion
t_1	TBD	ns min	Minimum $\overline{CS}$ Pulse Width
t_2	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3[3]	TBD	ns max	Delay from $\overline{CS}$ Until SDATA 3-State Disabled
t_4[3]	TBD	ns max	Data Access Time After SCLK Falling Edge
t_5	$0.4t_{SCLK}$	ns min	SCLK Low Pulse Width
t_6	$0.4t_{SCLK}$	ns min	SCLK High Pulse Width
t_7	TBD	ns min	SCLK to Data Valid Hold Time
t_8[4]	TBD	ns max	SCLK falling Edge to SDATA High Impedance
$t_{power\text{-}up}$[5]	TBD	µs typ	Power up time from Full Power-down.

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts.
[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.
[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.
[4]t_8 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.
[5]See Power-up Time section.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3 V to TBD V
Analog Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	–0.3 V to TBDV
Digital Output Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	
Commercial (A, B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
SOT-23 Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	229.6°C/W (SOT23)
	205.9°C/W (µSOIC)
θ_{JC} Thermal Impedance	91.99°C/W (SOT23)
	43.74°C/W (µSOIC)
Lead Temperature, Soldering	
Vapor Phase (60 secs)	+215°C
Infared (15 secs)	+220°C
ESD	TBD

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

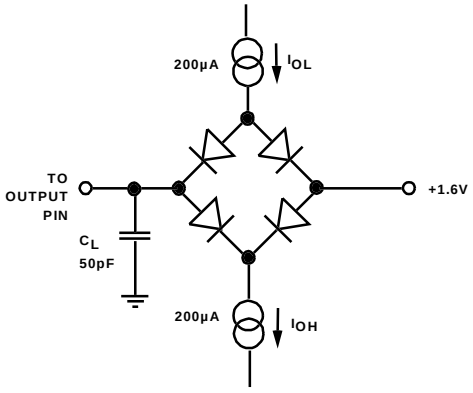


Figure 1. Load Circuit for Digital Output Timing Specifications

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7466/AD7467/AD7468 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
6	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7466/AD7467/AD7468 and also frames the serial data transfer.
1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7466/67/68 is from +1.8 V to +3.6 V.
2	GND	Analog Ground. Ground reference point for all circuitry on the AD7466/AD7467/AD7468. All analog input signals should be referred to this GND voltage.
3	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 to V_{DD}.
5	SDATA	Data Out. Logic Output. The conversion result from the AD7466/AD7467/AD7468 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7466 consists of four leading zeros followed by the 12 bits of conversion data which is provided MSB first. The data stream for the AD7467 consists of four leading zeros followed by 10 bits of data. The datastream for the AD7468 consists of four leading zeros followed by 8 bits of data.
4	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7466/AD7467/AD7468 conversion process.

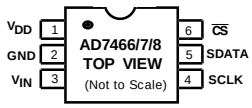
ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Option[2]	Branding Information
AD7466BRT	–40°C to +85°C	±1 max	RT-6	CLB
AD7467BRT	–40°C to +85°C	±1 max	RT-6	CMB
AD7468BRT	–40°C to +85°C	±0.5 max	RT-6	CNB
AD7466BRM	–40°C to +85°C	±1 max	RM-8	CQB
AD7467BRM	–40°C to +85°C	±1 max	RM-8	CRB
AD7468BRM	–40°C to +85°C	±0.5 max	RM-8	CSB
EVAL-AD7466CB[3]				
EVAL-AD7467CB[3]				
EVAL-CONTROL BRD2[4]				

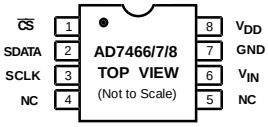
NOTES
[1]Linearity Error here refers to integral linearity error.
[2]RT = SOT-23, RM = µSOIC.
[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

AD7466/67/68 PINCONFIGURATION

AD7466/67/68 SOT-23



AD7466/67/68 µSOIC



TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7466/67/68 the endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 1 LSB.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode at the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion. See serial interface timing section for more details.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise + Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter this is 62dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7466/AD7467/AD7468, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7466/AD7467/AD7468 are tested using the CCIF standard where two input frequencies are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

AD7466/AD7467/AD7468 TYPICAL PERFORMANCE CURVES

Figure 2 shows a typical FFT plot for the AD7466 at 100 kHz sample rate and 30 kHz input frequency.

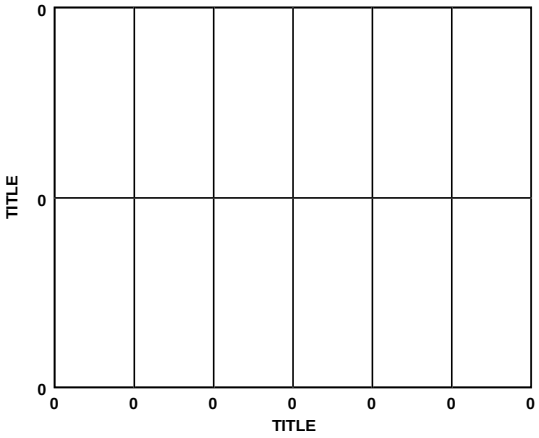


Figure 2. AD7466 Dynamic Performance at 100 kSPS

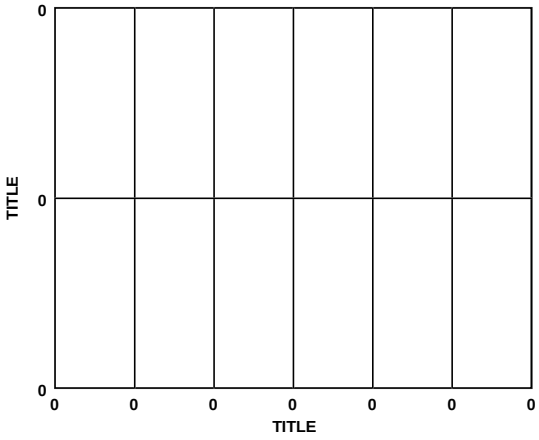


Figure 4. PSRR vs Supply Ripple Frequency

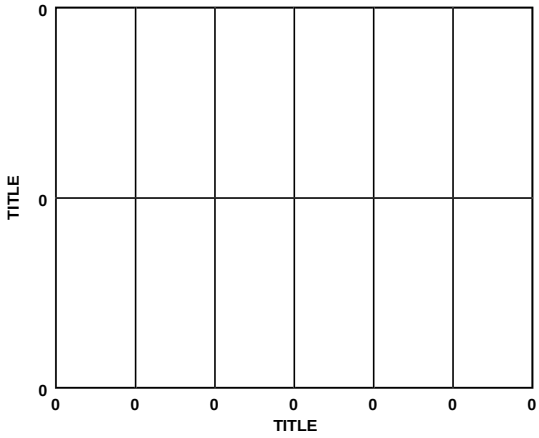


Figure 3. AD7466 SINAD vs Analog Input Frequency at 100 kSPS

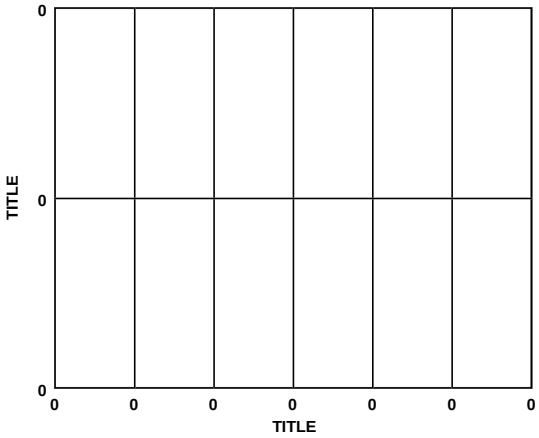


Figure 5. AD7466 THD vs Analog Input Frequency at 100 kSPS

CIRCUIT INFORMATION

The AD7466/AD7467/AD7468 are fast, micro-power, 12/10/8-bit, A/D converters respectively. The parts can be operated from a +1.8 V to +3.6 V supply. When operated from any supply voltage within this range, the AD7466/AD7467/AD7468 is capable of throughput rates of 100 kSPS when provided with a 2 MHz clock.

The AD7466/AD7467/AD7468 provides the user with an on-chip track/hold, A/D converter, and a serial interface housed in a tiny 6-pin SOT-23 package, which offers the user considerable space saving advantages over alternative solutions. The serial clock input accesses data from the part but also provides the clock source for the successive-approximation A/D converter. The analog input range is 0 to V_{DD}. An external reference is not required for the ADC and neither is there a reference on-chip. The reference for the AD7466/AD7467/AD7468 is derived from the power supply and thus gives the widest dynamic input range.

The AD7466/AD7467/AD7468 also features an automatic power-down mode option to allow power saving between conversions. The power-down feature is implemented across the standard serial interface as described in the "Modes of Operation" section.

CONVERTER OPERATION

The AD7466/AD7467/AD7468 is a successive approximation analog-to-digital converter based around a charge redistribution DAC. Figures 8 and 9 show simplified schematics of the ADC. Figure 8 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

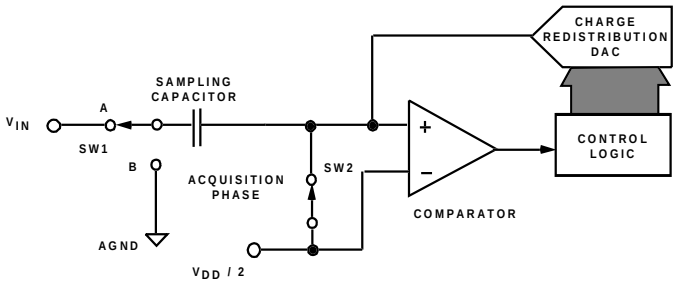


Figure 8. ADC Acquisition Phase

When the ADC starts a conversion, see figure 9, SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The Control Logic and the Charge Redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The Control Logic generates the ADC output code. Figure 10 shows the ADC transfer function.

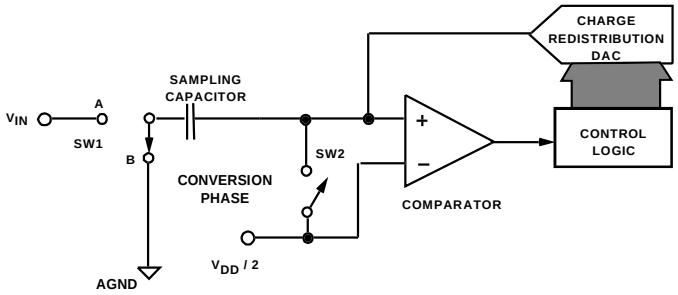


Figure 9. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7466/AD7467/AD7468 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1LSB, 2LSBs, etc.). The LSB size is = V_{DD}/4096 for the AD7466,the LSB size is = V_{DD}/1024 for the AD7467, and the LSB size is = V_{DD}/256 for the AD7468 . The ideal transfer characteristic for the AD7466/AD7467/AD7468 is shown in figure 10 below.

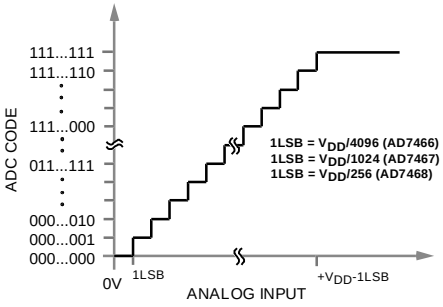


Figure 10. AD7466/67/68 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 11 shows a typical connection diagram for the AD7466/AD7467/AD7468. V_{REF} is taken internally from V_{DD} and as such V_{DD} should be well decoupled. This provides an analog input range of 0V to V_{DD}. For the AD7466 the conversion result is output in a 16-bit word with four leading zeroes followed by the MSB of the 12-bit result. The AD7467 conversion result consists of four leading zeros followed by the MSB of the 10-bit result. The AD7468 conversion result consists of four leading zeros followed by the MSB of the 8-bit result.

Alternatively, because the supply current required by the AD7466/AD7467/AD7468 is so low, a presision reference can be used as the supply source to the AD7466/AD7467/AD7468. A REF19x voltage reference (REF193 for 3V, REF192 for 2.5 V) can be used to supply the required voltage to the ADC - see figure 11. This configuration is especially useful if your power supply is quite noisy or if the system supply voltages are at some value other than 3V (e.g. 2.5V). The REF19x will output a steady voltage to the AD7466/AD7467/AD7468. In applications where power consumption is important, the automatic power down mode of the ADC and the sleep mode of the REF19x reference should be used to improve power performance. See Modes of Operation section of the datasheet.

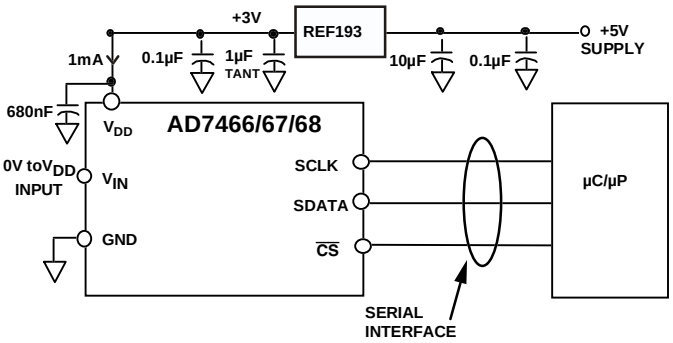


Figure 11. REF193 as Power Supply to AD7466/AD7467/AD7468

Analog Input

Figure 12 shows an equivalent circuit of the analog input sturcture of the AD7466/AD7467/7468. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200mV. This will cause these diodes to become forward biased and start conducting current into the substrate. The capacitor C1 in figure 12 is typically about 4pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 100Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 16pF typically. For ac applications, removing high frequency components from the analog input signal is recommended by use of a band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal to noise ratio are critical the analog input should be driven

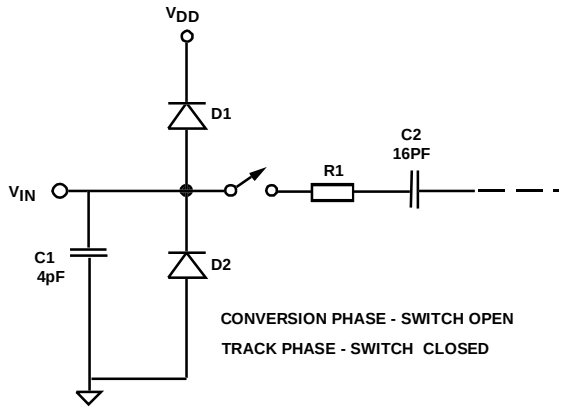


Figure 12. Equivalent Analog Input Circuit

from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

When no amplifier is used to drive the analog input the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 13 shows a graph of the Total Harmonic Distortion vs. analog input signal frequency for different source impedances when using a supply voltage of 2.7V and sampling at a rate of 100 kSPS.

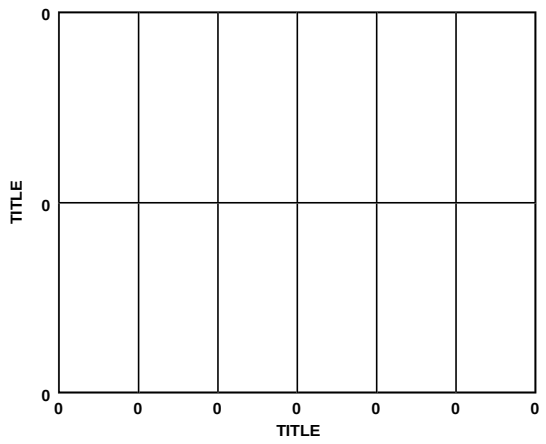


Figure 13. THD vs. Analog Input Frequency for Various Source Impedance

Digital Inputs

The digital inputs applied to the AD7466/AD7467/AD7468 are not limited by the maximum ratings which limit the analog inputs. One advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3V limit is the fact that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK are applied before V_{DD} then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3V was applied prior to V_{DD}.

MODE OF OPERATION

The AD7466/AD7467/AD7468 automatically enters powerdown at the end of each conversion. This mode of operation is designed to provide flexible power management options and to optimize the power dissipation/ throughput rate ratio for differing application requirements. Figure 14 shows the general diagram of the operaion of the AD7466/AD7467/AD7468. On the falling $\overline{CS}$ edge the part begins to power up and the Track and Hold, which was in Hold while the part was in power down, will go into track mode. When operating the part with a 2.4 MHz clock it will take 2 clock cycles to fully power up the part and acquire the input signal. On the third SCLK falling edge after the $\overline{CS}$ falling edge the Track and Hold will return to hold mode. For the AD7466 sixteen serial clock cycles are required to complete the conversion and access the complete conversion result.On the 16th SCLK falling edge the part will automatically enter power down . The AD7467 will automatically enter powerdown on the fourteenth SCLK falling edge. The AD7468 will automatically enter powerdown on the twelveth SCLK falling edge. When supplies are first applied to the AD7466/AD7467/AD7468 a dummy conversion should be performed to ensure that the part is in powerdown mode.

The conversion is iniated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. For the AD7466 if $\overline{CS}$ is brought high any time before the 16th SCLK falling edge the part will enter power down and the conversion that was initiated by the falling edge of $\overline{CS}$ will be terminated and SDATA will go back into tri-state. This also applies for the AD7467/AD7468, if $\overline{CS}$ is brought high before the conversion is complete (the 14th SCLK falling edge for the AD7467, and the 12th SCLK falling edge for the AD7468) the part will enter powerdown and the conversion will be terminated.

Once a data transfer is complete (SDATA has returned to tri-state), another conversion can be initiated after the quiet time, t_{quiet}, has elapsed by bringing $\overline{CS}$ low again.

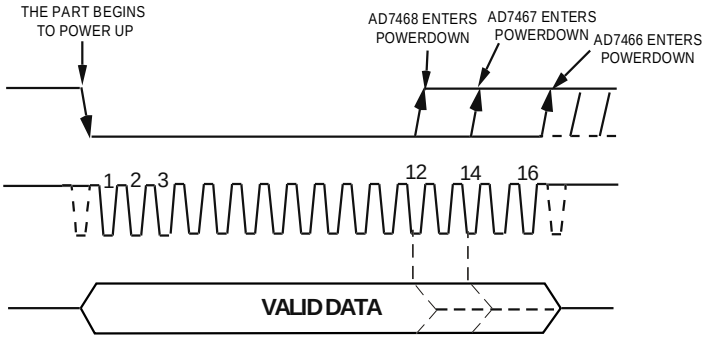


Figure 14. Normal Mode Operation

SERIAL INTERFACE

Figure 15, 16, 17 show the detailed timing diagram for serial interfacing to the AD7466/AD7467/AD7468.The serial clock provides the conversion clock and also controls the transfer of information from the ADC during a conversion.

On the $\overline{CS}$ falling edge the part begins to power up. The falling edge of $\overline{CS}$ puts the track and hold into track mode and takes the bus out of tristate. The conversion is also initiated at this point and will require 16 SCLK cycles to complete. On the third SCLK falling edge the part should be fully powered up, as shown in figure 15 at point B. On the third SCLK falling edge after the CS falling edge the track and hold will return to hold. On the 16th SCLK falling edge the SDATA line will go back into tristate and the AD7466 will enter power down. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed then the conversion will be terminated and the SDATA line will go back into tri-state and the part will enter power down, otherwise SDATA returns to tri-state on the 16th SCLK falling edge as shown in Figure 15. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7466.

For the AD7467, the fourteenth SCLK falling edge will cause the SDATA line to go back into tri-state and the part will enter powerdown. If the rising edge of CS occurs before 14 SCLKs have elapsed then the conversion will be terminated and the SDATA line will go back into tri-state and the AD7467 will enter powerdown, otherwise SDATA returns to tri-state on the 14th SCLK falling edge as ahown in figure 16. Fourteen serial clock cycles are required to perform the conversion process and to access data from the AD7467.

For the AD7468, the 12th SCLK falling edge will cause the SDATA line to go back into tri-state and the part will enter powerdown. If the rising edge of CS occurs before 12 SCLKs have elapsed then the conversion will be terminated and the SDATA line will go back into tri-state and the AD7468 will enter powerdown, otherwise SDATA returns to tri-state on the 12th SCLK falling edge as ahown in figure 17. Twelve serial clock cycles are required to perform the conversion process and to access data from the AD7468.

$\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the 2nd leading zero, thus the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. For the Ad7466 the final bit in the data transfer is valid on the sixteenth falling edge, having being clocked out on the previous (15th) falling edge.

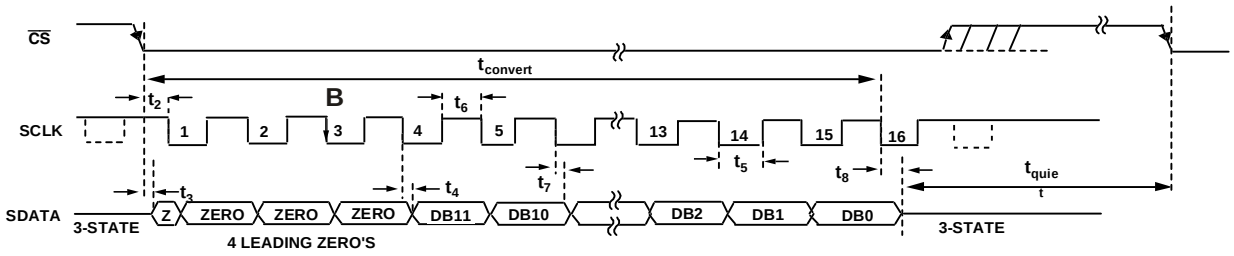


Figure 15. AD7466 Serial Interface Timing Diagram

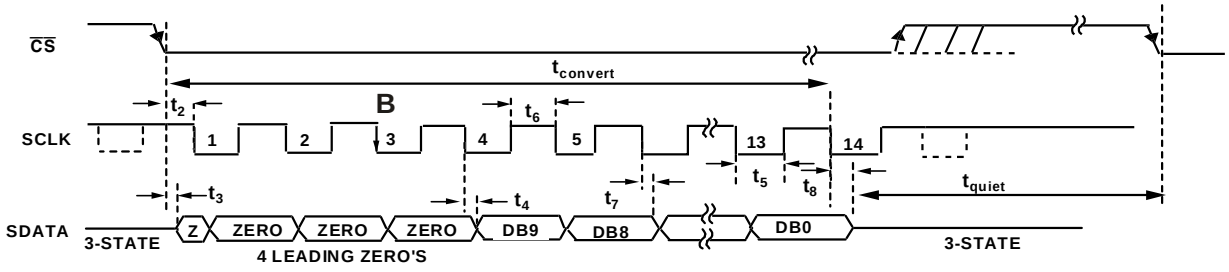


Figure 16. AD7467 Serial Interface Timing Diagram

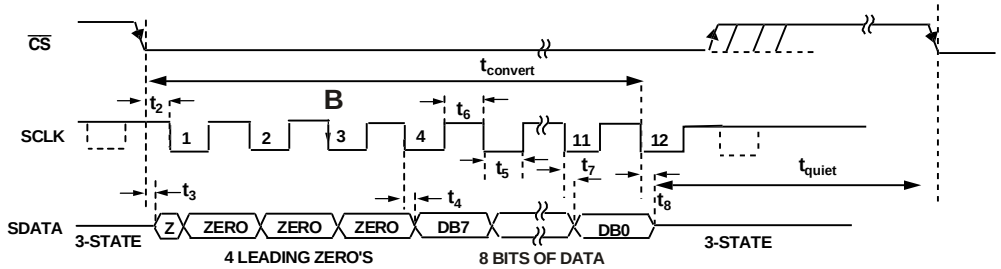


Figure 17. AD7468 Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7466/AD7467/AD7468 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7466/AD7467/AD7468 with some of the more common microcontroller and DSP serial interface protocols.

AD7466/7/8 to TMS320C5xC54x

The serial interface on the TMS320C5x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7466/67/68. The $\overline{CS}$ input allows easy interfacing between the TMS320C5x and the AD7466/67/68 without any glue logic required. The serial port of the TMS320C5x/C54x is set up to operate in burst mode with internal CLKX (TX serial clock) and FSX (TX frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1 and TXM = 1. The format bit, FO, may be set to 1 to set the word length to 8-bits, in order to implement the power-down mode on the AD7466/67/68.

The connection diagram is shown in Figure 18. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the TMS320C5x/C54x will provide equidistant sampling.

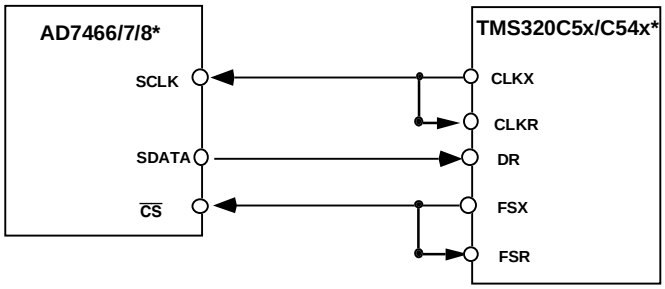


Figure 18. Interfacing to the TMS320C5x

AD7466/7/8 to ADSP21xx

The ADSP21xx family of DSPs are interfaced directly to the AD7466/67/68 without any glue logic required. The SPORT control register should be set up as follows:
TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data words
ISCLK = 1, Internal serial clock
TFSR = RFSR = 1, Frame every word
IRFS = 0,
ITFS = 1.

The connection diagram is shown in Figure 19. The ADSP21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in Alternate Framing Mode and the SPORT control register is set up as described. The Frame synchronisation signal generated on the TFS is tied to $\overline{CS}$ and as with all signal processing applications equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and under certain conditions, equidistant sampling may not be acheived.

The Timer registers etc. are loaded with a value which will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instrustion to transmit with TFS is given, (i.e. AX0=TX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone High, Low and High before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, then the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP2111 has a master clock frequency of 16MHz. If the SCLKDIV register is loaded with the value 3 then a SCLK of 2MHz is obtained, and 8 master clock periods will elapse for every 1 SCLK period. If the timer registers are loaded with the value 803, then 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in non-equidistant sampling as the transmit instruction is occuring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N then equidistant sampling will be implemented by the DSP.

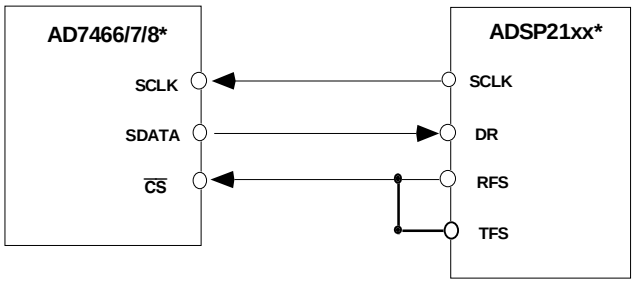


Figure 19. Interfacing to the ADSP-21xx

AD7466/67/68 to DSP56xxx

The connection diagram in figure 20 shows how the AD7466/67/68 can be connected to the SSI (Synchronous Serial Interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in Synchronous Mode (SYN bit in CRB =1) with internally generated 1-bit clock period frame sync for both TX and RX (bits FSL1 =1 and FSL0 =0 in CRB). Set the word length to 16 by setting bits WL1 =1 and WL0 = 0 in CRA. It should be noted that for signal processing applications, it is imperative that the frame synchronisation signal from the DSP56xxx will provide equidistant sampling.

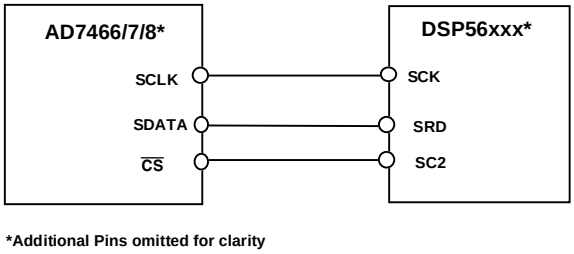


Figure 20. Interfacing to the DSP56xx

AD7466/67/68 to MC68HC16

The Serial Peripheral Interface (SPI) on the MC68HC16 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 1 and the Clock Phase Bit (CPHA) = 0. The SPI is configured by writing to the SPI Control Register (SPCR) - see 68HC16 user manual. The serial transfer will take place as a 16-bit operation when the SIZE bit in the SPCR register is set to SIZE = 1. A connection diagram is shown in figure 21.

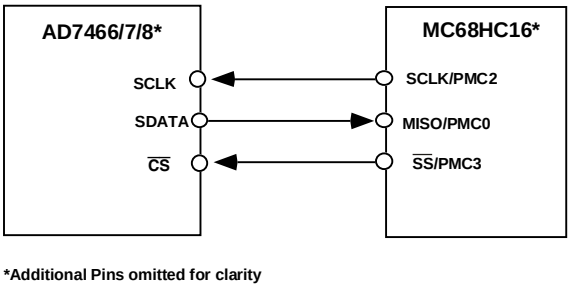
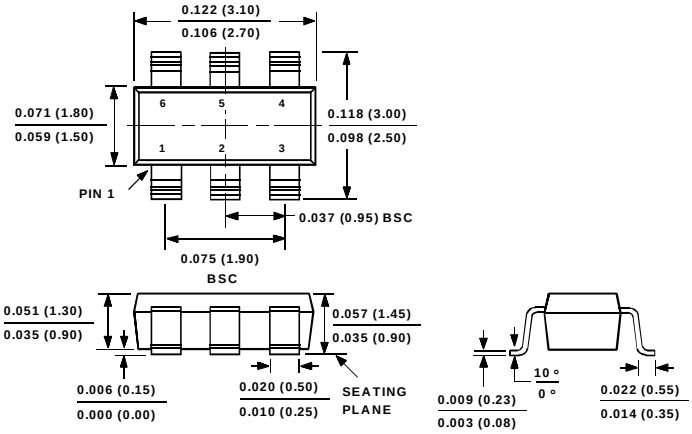


Figure 21. Interfacing to the MC68HC16

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-lead SOT23 (RT-6)



8-lead microSOIC (RM-8)