14-Bit, 1 MSPS, Differential, Programmable Input PulSAR® ADC

Data Sheet

AD7952

FEATURES

Multiple pins/software-programmable input ranges
- **+5 V (10 V p-p), +10 V (20 V p-p), ±5 V (20 V p-p), ±10 V (40 V p-p)**

Pins or serial SPI®-compatible input ranges/mode selection
Throughput
- **1 MSPS (warp mode)**
- **800 kSPS (normal mode)**
- **670 kSPS (impulse mode)**

14-bit resolution with no missing codes
INL: ±0.3 LSB typical, ±1 LSB maximum (±61 ppm of FSR)
SNR: 85 dB @ 2 kHz
***i*CMOS® process technology**
5 V internal reference: typical drift 3 ppm/°C; TEMP output
No pipeline delay (SAR architecture)
Parallel (14- or 8-bit bus) and serial 5 V/3.3 V interface
SPI-/QSPI™-/MICROWIRE™-/DSP-compatible
Power dissipation
- **235 mW @ 1 MSPS**
- **10 mW @ 1 kSPS**

48-lead LQFP and 48-lead LFCSP (7 mm × 7 mm)

APPLICATIONS

Process controls
Medical instruments
High speed data acquisition
Digital signal processing
Instrumentation
Spectrum analysis
ATE

GENERAL DESCRIPTION

The AD7952 is a 14-bit, charge redistribution, successive approximation register (SAR) architecture analog-to-digital converter (ADC) fabricated on Analog Devices, Inc.'s *i*CMOS high voltage process. The device is configured through hardware or via a dedicated write-only serial configuration port for input range and operating mode. The AD7952 contains a high speed 14-bit sampling ADC, an internal conversion clock, an internal reference (and buffer), error correction circuits, and both serial and parallel system interface ports. A falling edge on $\overline{\text{CNVST}}$ samples the fully differential analog inputs on IN+ and IN−. The AD7952 features four different analog input ranges and three different sampling modes: warp mode for the fastest throughput, normal mode for the fastest asynchronous throughput, and impulse mode where power is scaled with throughput. Operation is specified from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

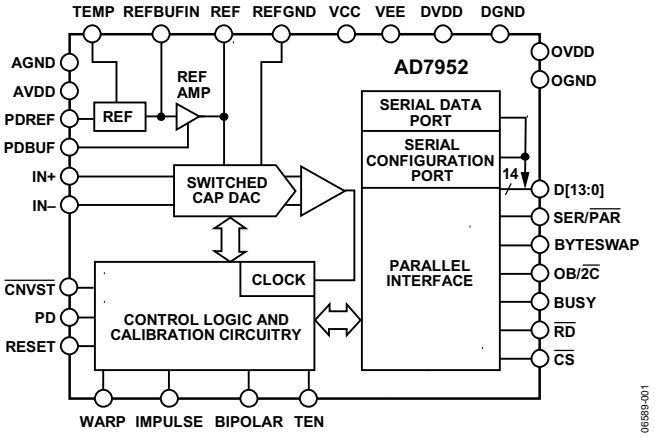

Figure 1.

Table 1. 48-Lead PulSAR Selection

Input Type	Res (Bits)	100 to 250 (kSPS)	500 to 570 (kSPS)	570 to 1000 (kSPS)	>1000 kSPS
Bipolar	14			AD7951	
Differential Bipolar	14			AD7952	
Unipolar	16	AD7651		AD7653	
		AD7660	AD7650	AD7667	
		AD7661	AD7652		
			AD7664		
			AD7666		
Bipolar	16	AD7610	AD7665	AD7612	
		AD7663		AD7671	
Differential Unipolar	16	AD7675	AD7676	AD7677	AD7621
					AD7622
					AD7623
Simultaneous/ Multichannel Unipolar	16		AD7654		
			AD7655		
Differential Unipolar	18	AD7678	AD7679	AD7674	AD7641
					AD7643
Differential Bipolar	18	AD7631		AD7634	

Rev. A **Document Feedback**

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REVISION HISTORY

12/12—Rev. 0 to Rev. A

Added Exposed Pad Note ... 8
Changes to Power Sequencing Section ... 23
Deleted Evaluating Performance Section ... 31
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2/07—Revision 0: Initial Version

SPECIFICATIONS

AVDD = DVDD = 5 V; OVDD = 2.7 V to 5.5 V; VCC = 15 V; VEE = −15 V; V_{REF} = 5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ANALOG INPUTS					
Differential Voltage Range, V_{IN}	$(V_{IN+}) - (V_{IN-})$				
0 V to 5 V	V_{IN} = 10 V p-p	$-V_{REF}$		$+V_{REF}$	V
0 V to 10 V	V_{IN} = 20 V p-p	$-2\ V_{REF}$		$+2\ V_{REF}$	V
±5 V	V_{IN} = 20 V p-p	$-2\ V_{REF}$		$+2\ V_{REF}$	V
±10 V	V_{IN} = 40 V p-p	$-4\ V_{REF}$		$+4\ V_{REF}$	V
Operating Voltage Range	V_{IN+}, V_{IN-} to AGND				
0 V to 5 V		−0.1		+5.1	V
0 V to 10 V		−0.1		+10.1	V
±5 V		−5.1		+5.1	V
±10 V		−10.1		+10.1	V
Common-Mode Voltage Range	V_{IN+}, V_{IN-}				
5 V		$V_{REF}/2 - 0.1$	$V_{REF}/2$	$V_{REF}/2 + 0.1$	V
10 V		$V_{REF} - 0.2$	V_{REF}	$V_{REF} + 0.2$	V
Bipolar Ranges		−0.1	0	+0.1	V
Analog Input CMRR	f_{IN} = 100 kHz		75		dB
Input Current	V_{IN} = ±5 V, ±10 V @ 670 kSPS		220[1]		µA
Input Impedance	See Analog Inputs section				
THROUGHPUT SPEED					
Complete Cycle	In warp mode			1	µs
Throughput Rate	In warp mode	1		1	MSPS
Time Between Conversions	In warp mode			1	ms
Complete Cycle	In normal mode			1.25	µs
Throughput Rate	In normal mode	0		800	kSPS
Complete Cycle	In impulse mode			1.49	µs
Throughput Rate	In impulse mode	0		670	kSPS
DC ACCURACY					
Integral Linearity Error[2]		−1	±0.3	+1	LSB[3]
No Missing Codes[2]		14			Bits
Differential Linearity Error[2]		−1		+1	LSB
Transition Noise			0.55		LSB
Zero Error (Unipolar or Bipolar)		−15		+15	LSB
Zero-Error Temperature Drift			±1		ppm/°C
Full-Scale Error (Unipolar or Bipolar)		−20		+20	LSB
Full-Scale Error Temperature Drift			±1		ppm/°C
Power Supply Sensitivity	AVDD = 5 V ± 5%		±0.8		LSB
AC ACCURACY					
Dynamic Range	f_{IN} = 2 kHz, −60 dB	84.5	85.5		dB[4]
Signal-to-Noise Ratio, SNR	f_{IN} = 2 kHz	84.5	85.5		dB
	f_{IN} = 20 kHz		85.5		dB
Signal-to-(Noise + Distortion), SINAD	f_{IN} = 2 kHz	83	85.4		dB
Total Harmonic Distortion	f_{IN} = 2 kHz		−105		dB
Spurious-Free Dynamic Range	f_{IN} = 2 kHz		102		dB
−3 dB Input Bandwidth	V_{IN} = 0 V to 5 V		45		MHz
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-scale step			500	ns

Parameter	Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE	PDREF = PDBUF = low				
Output Voltage	REF @ 25°C	4.965	5.000	5.035	V
Temperature Drift	−40°C to +85°C		±3		ppm/°C
Line Regulation	AVDD = 5 V ± 5%		±15		ppm/V
Long-Term Drift	1000 hours		50		ppm
Turn-On Settling Time	C_{REF} = 22 µF		10		ms
REFERENCE BUFFER	PDREF = high				
REFBUFIN Input Voltage Range		2.4	2.5	2.6	V
EXTERNAL REFERENCE	PDREF = PDBUF = high				
Voltage Range	REF	4.75	5	AVDD + 0.1	V
Current Drain	1 MSPS throughput		200		µA
TEMPERATURE PIN					
Voltage Output	@ 25°C		311		mV
Temperature Sensitivity			1		mV/°C
Output Resistance			4.33		kΩ
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.6	V
V_{IH}		2.1		OVDD + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format	Parallel or serial 14-bit				
Pipeline Delay[5]					
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	OVDD − 0.6			V
POWER SUPPLIES					
Specified Performance					
AVDD		4.75[6]	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25	V
VCC		7	15	15.75	V
VEE		−15.75	−15	0	V
Operating Current[7, 8]	@ 1 MSPS throughput				
AVDD					
With Internal Reference			20		mA
With Internal Reference Disabled			18.5		mA
DVDD			7		mA
OVDD			0.5		mA
VCC	VCC = 15 V, with internal reference buffer		4		mA
	VCC = 15 V		3		mA
VEE	VEE = −15 V		2		mA
Power Dissipation	@ 1 MSPS throughput				
With Internal Reference	PDREF = PDBUF = low		235	260	mW
With Internal Reference Disabled	PDREF = PDBUF = high		215	240	mW
In Power-Down Mode[9]	PD = high		10		µW
TEMPERATURE RANGE[10]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With V_{IN} = unipolar 5 V or unipolar 10 V ranges, the input current is typically 70 µA. In all input ranges, the input current scales with throughput. See the Analog Inputs section.
[2] Linearity is tested using endpoints, not best fit. All linearity is tested with an external 5 V reference.
[3] LSB means least significant bit. All specifications in LSB do not include the error contributed by the reference.
[4] All specifications in dB are referred to a full-scale range input, FSR. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[5] Conversion results are available immediately after completed conversion.
[6] 4.75 V or V_{REF} − 0.1 V, whichever is larger.
[7] Tested in parallel reading mode.
[8] With internal reference, PDREF = PDBUF = low; with internal reference disabled, PDREF = PDBUF = high. With internal reference buffer, PDBUF = low.
[9] With all digital inputs forced to OVDD.
[10] Consult sales for extended temperature range.

TIMING SPECIFICATIONS

AVDD = DVDD = 5 V; OVDD = 2.7 V to 5.5 V; VCC = 15 V; VEE = −15 V; V_{REF} = 5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
CONVERSION AND RESET (See Figure 34 and Figure 35)					
Convert Pulse Width	t_1	10			ns
Time Between Conversions	t_2				
Warp Mode/Normal Mode/Impulse Mode[1]		1/1.25/1.49			µs
$\overline{CNVST}$ Low to BUSY High Delay	t_3			35	ns
BUSY High All Modes (Except Master Serial Read After Convert)	t_4				
Warp Mode/Normal Mode/Impulse Mode				850/1100/1350	ns
Aperture Delay	t_5		2		ns
End of Conversion to BUSY Low Delay	t_6	10			ns
Conversion Time	t_7				
Warp Mode/Normal Mode/Impulse Mode				850/1100/1350	ns
Acquisition Time	t_8				
Warp Mode/Normal Mode/Impulse Mode		200			ns
RESET Pulse Width	t_9	10			ns
PARALLEL INTERFACE MODES (See Figure 36 and Figure 38)					
$\overline{CNVST}$ Low to DATA Valid Delay	t_{10}				
Warp Mode/Normal Mode/Impulse Mode				850/1100/1350	ns
DATA Valid to BUSY Low Delay	t_{11}	20			ns
Bus Access Request to DATA Valid	t_{12}			40	ns
Bus Relinquish Time	t_{13}	2		15	ns
MASTER SERIAL INTERFACE MODES[2] (See Figure 40 and Figure 41)					
$\overline{CS}$ Low to SYNC Valid Delay	t_{14}			10	ns
$\overline{CS}$ Low to Internal SDCLK Valid Delay[2]	t_{15}			10	ns
$\overline{CS}$ Low to SDOUT Delay	t_{16}			10	ns
$\overline{CNVST}$ Low to SYNC Delay, Read During Convert	t_{17}				
Warp Mode/Normal Mode/Impulse Mode			50/290/530		ns
SYNC Asserted to SDCLK First Edge Delay	t_{18}	3			ns
Internal SDCLK Period[3]	t_{19}	30		45	ns
Internal SDCLK High[3]	t_{20}	15			ns
Internal SDCLK Low[3]	t_{21}	10			ns
SDOUT Valid Setup Time[3]	t_{22}	4			ns
SDOUT Valid Hold Time[3]	t_{23}	5			ns
SDCLK Last Edge to SYNC Delay[3]	t_{24}	5			ns
$\overline{CS}$ High to SYNC High-Z	t_{25}			10	ns
$\overline{CS}$ High to Internal SDCLK High-Z	t_{26}			10	ns
$\overline{CS}$ High to SDOUT High-Z	t_{27}			10	ns
BUSY High in Master Serial Read After Convert[3]	t_{28}		See Table 4		
$\overline{CNVST}$ Low to SYNC Delay, Read After Convert	t_{29}				
Warp Mode/Normal Mode/Impulse Mode			710/950/1190		ns
SYNC Deasserted to BUSY Low Delay	t_{30}		25		ns

Parameter	Symbol	Min	Typ	Max	Unit
SLAVE SERIAL/SERIAL CONFIGURATION INTERFACE MODES[2] (See Figure 43, Figure 44, and Figure 46)					
External SDCLK, SCCLK Setup Time	t_{31}	5			ns
External SDCLK Active Edge to SDOUT Delay	t_{32}	2		18	ns
SDIN/SCIN Setup Time	t_{33}	5			ns
SDIN/SCIN Hold Time	t_{34}	5			ns
External SDCLK/SCCLK Period	t_{35}	25			ns
External SDCLK/SCCLK High	t_{36}	10			ns
External SDCLK/SCCLK Low	t_{37}	10			ns

[1] In warp mode only, the time between conversions is 1 ms; otherwise, there is no required maximum time.
[2] In serial interface modes, the SYNC, SDSCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.
[3] In serial master read during convert mode. See Table 4 for serial master read after convert mode.

Table 4. Serial Clock Timings in Master Read After Convert Mode

DIVSCLK[1]		**0**	**0**	**1**	**1**	
DIVSCLK[0]	**Symbol**	**0**	**1**	**0**	**1**	**Unit**
SYNC to SDCLK First Edge Delay Minimum	t_{18}	3	20	20	20	ns
Internal SDCLK Period Minimum	t_{19}	30	60	120	240	ns
Internal SDCLK Period Maximum	t_{19}	45	90	180	360	ns
Internal SDCLK High Minimum	t_{20}	12	30	60	120	ns
Internal SDCLK Low Minimum	t_{21}	10	25	55	115	ns
SDOUT Valid Setup Time Minimum	t_{22}	4	20	20	20	ns
SDOUT Valid Hold Time Minimum	t_{23}	5	8	35	90	ns
SDCLK Last Edge to SYNC Delay Minimum	t_{24}	5	7	35	90	ns
BUSY High Width Maximum	t_{28}					
Warp Mode		1.60	2.35	3.75	6.75	µs
Normal Mode		1.85	2.60	4.00	7.00	µs
Impulse Mode		2.10	2.85	4.25	7.25	µs

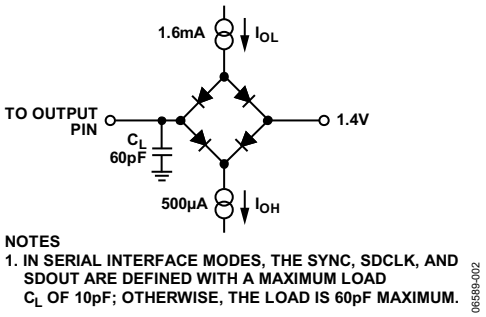


Figure 2. Load Circuit for Digital Interface Timing, SDOUT, SYNC, and SDCLK Outputs, C_L = 10 pF

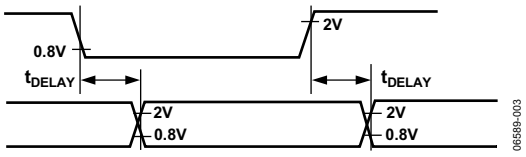


Figure 3. Voltage Reference Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs/Outputs	
IN+[1], IN−[1] to AGND	VEE − 0.3 V to VCC + 0.3 V
REF, REFBUFIN, TEMP, REFGND to AGND	AVDD + 0.3 V to AGND − 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD, OVDD	−0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD	±7 V
DVDD to OVDD	±7 V
VCC to AGND, DGND	−0.3 V to +16.5 V
VEE to GND	+0.3 V to −16.5 V
Digital Inputs	−0.3 V to OVDD + 0.3 V
PDREF, PDBUF	±20 mA
Internal Power Dissipation[2]	700 mW
Internal Power Dissipation[3]	2.5 W
Junction Temperature	125°C
Storage Temperature Range	−65°C to +125°C

[1] See the Analog Inputs section.
[2] Specification is for the device in free air: 48-Lead LQFP; θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.
[3] Specification is for the device in free air: 48-Lead LFCSP; θ_{JA} = 26°C/W.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

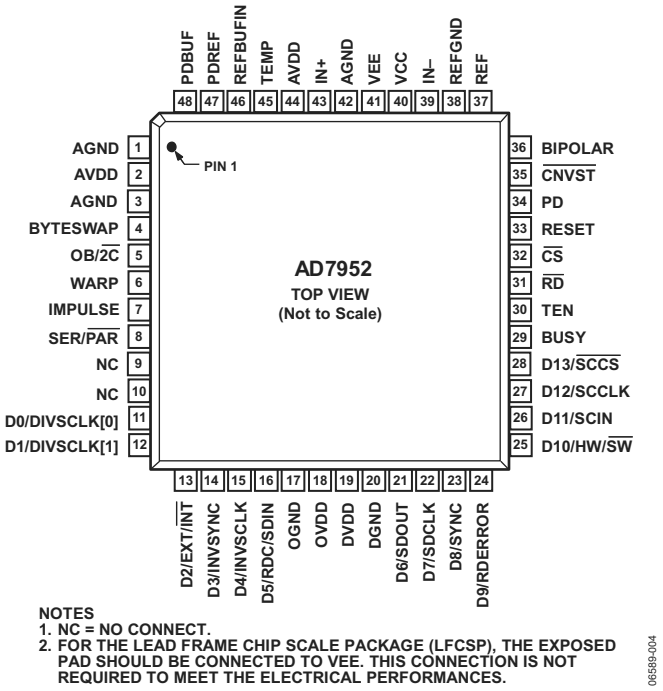


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 3, 42	AGND	P	Analog Power Ground Pins. Ground reference point for all analog I/O. All analog I/O should be referenced to AGND and should be connected to the analog ground plane of the system. In addition, the AGND, DGND, and OGND voltages should be at the same potential.
2, 44	AVDD	P	Analog Power Pins. Nominally 4.75 V to 5.25 V and decoupled with 10 µF and 100 nF capacitors.
4	BYTESWAP	DI	Parallel Mode Selection (8 Bit/14 Bit). When high, the LSB is output on D[15:8] and the MSB is output on D[7:0]; when low, the LSB is output on D[7:0] and the MSB is output on D[15:8].
5	OB/$\overline{2C}$	DI[2]	Straight Binary/Binary Twos Complement Output. When high, the digital output is straight binary. When low, the MSB is inverted resulting in a twos complement output from its internal shift register.
6	WARP	DI[2]	Conversion Mode Selection. Used in conjunction with the IMPULSE input per the following. **Conversion Mode** / **WARP** / **IMPULSE** Normal / Low / Low Impulse / Low / High Warp / High / Low Normal / High / High See the Modes of Operation section for a more detailed description.
7	IMPULSE	DI[2]	Conversion Mode Selection. See the WARP pin description in this table. See the Modes of Operation section for a more detailed description.
8	SER/$\overline{PAR}$	DI	Serial/Parallel Selection Input. When SER/$\overline{PAR}$ = low, the parallel mode is selected. When SER/$\overline{PAR}$ = high, the serial modes are selected. Some bits of the data bus are used as a serial port, and the remaining data bits are high impedance outputs.
9, 10	NC	DO	No Connect. Do not connect.

Pin No.	Mnemonic	Type[1]	Description
11, 12	D[0:1] or DIVSCLK[0:1]	DI/O	In parallel mode, these outputs are used as Bit 0 and Bit 1 of the parallel port data output bus. Serial Data Division Clock Selection. In serial master read after convert mode (SER/$\overline{PAR}$ = high, EXT/$\overline{INT}$ = low, RDC/SDIN = low), these inputs can be used to slow down the internally generated serial data clock that clocks the data output. In other serial modes, these pins are high impedance outputs.
13	D2 or EXT/$\overline{INT}$	DI/O	In parallel mode, this output is used as Bit 2 of the parallel port data output bus. Serial Data Clock Source Select. In serial mode, this input is used to select the internally generated (master) or external (slave) serial data clock for the AD7952 output data. When EXT/$\overline{INT}$ = low (master mode), the internal serial data clock is selected on SDCLK output. When EXT/$\overline{INT}$ = high (slave mode), the output data is synchronized to an external clock signal (gated by $\overline{CS}$) connected to the SDCLK input.
14	D3 or INVSYNC	DI/O	In parallel mode, this output is used as Bit 3 of the parallel port data output bus. Serial Data Invert Sync Select. In serial master mode (SER/$\overline{PAR}$ = high, EXT/$\overline{INT}$ = low), this input is used to select the active state of the SYNC signal. When INVSYNC = low, SYNC is active high. When INVSYNC = high, SYNC is active low.
15	D4 or INVSCLK	DI/O	In parallel mode, this output is used as Bit 4 of the parallel port data output bus. In all serial modes, invert SDCLK/SCCLK select. This input is used to invert both SDCLK and SCCLK. When INVSCLK = low, the rising edge of SDCLK/SCCLK are used. When INVSCLK = high, the falling edge of SDCLK/SCCLK are used.
16	D5 or RDC or	DI/O	In parallel mode, this output is used as Bit 5 of the parallel port data output bus. Serial Data Read During Convert. In serial master mode (SER/$\overline{PAR}$ = high, EXT/$\overline{INT}$ = low), RDC is used to select the read mode. Refer to the Master Serial Interface section. When RDC = low, the current result is read after conversion. Note the maximum throughput is not attainable in this mode. When RDC = high, the previous conversion result is read during the current conversion.
	SDIN		Serial Data In. In serial slave mode (SER/$\overline{PAR}$ = high, EXT/$\overline{INT}$ = high), SDIN can be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 16 SDCLK periods after the initiation of the read sequence.
17	OGND	P	Input/Output Interface Digital Power Ground. Ground reference point for digital outputs. Should be connected to the system digital ground ideally at the same potential as AGND and DGND.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface 2.5 V, 3 V, or 5 V and decoupled with 10 µF and 100 nF capacitors.
19	DVDD	P	Digital Power. Nominally at 4.75 V to 5.25 V and decoupled with 10 µF and 100 nF capacitors. Can be supplied from AVDD.
20	DGND	P	Digital Power Ground. Ground reference point for digital outputs. Should be connected to system digital ground ideally at the same potential as AGND and OGND.
21	D6 or SDOUT	DO	In parallel mode, this output is used as Bit 6 of the parallel port data output bus. Serial Data Output. In all serial modes, this pin is used as the serial data output synchronized to SDCLK. Conversion results are stored in an on-chip register. The AD7952 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of OB/$\overline{2C}$. When EXT/$\overline{INT}$ = low (master mode), SDOUT is valid on both edges of SDCLK. When EXT/$\overline{INT}$ = high (slave mode): When INVSCLK = low, SDOUT is updated on SDCLK rising edge. When INVSCLK = high, SDOUT is updated on SDCLK falling edge.
22	D7 or SDCLK	DI/O	In parallel mode, this output is used as Bit 7 of the parallel port data output bus. Serial Data Clock. In all serial modes, this pin is used as the serial data clock input or output, dependent on the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends on the logic state of the INVSCLK pin.

Pin No.	Mnemonic	Type[1]	Description
23	D8 or SYNC	DO	In parallel mode, this output is used as Bit 8 of the parallel port data output bus. Serial Data Frame Synchronization. In serial master mode (SER/$\overline{\text{PAR}}$ = high, EXT/$\overline{\text{INT}}$= low), this output is used as a digital output frame synchronization for use with the internal data clock. When a read sequence is initiated and INVSYNC = low, SYNC is driven high and remains high while the SDOUT output is valid. When a read sequence is initiated and INVSYNC = high, SYNC is driven low and remains low while the SDOUT output is valid.
24	D9 or RDERROR	DO	In parallel mode, this output is used as Bit 9 of the parallel port data output bus. Serial Data Read Error. In serial slave mode (SER/$\overline{\text{PAR}}$ = high, EXT/$\overline{\text{INT}}$ = high), this output is used as an incomplete data read error flag. If a data read is started and not completed when the current conversion is completed, the current data is lost and RDERROR is pulsed high.
25	D10 or HW/$\overline{\text{SW}}$	DI/O	In parallel mode, this output is used as Bit 10 of the parallel port data output bus. Serial Configuration Hardware/Software Select. In serial mode, this input is used to configure the AD7952 by hardware or software. See the Hardware Configuration section and Software Configuration section. When HW/$\overline{\text{SW}}$ = low, the AD7952 is configured through software using the serial configuration register. When HW/$\overline{\text{SW}}$ = high, the AD7952 is configured through dedicated hardware input pins.
26	D11 or SCIN	DI/O	In parallel mode, this output is used as Bit 11 of the parallel port data output bus. Serial Configuration Data Input. In serial software configuration mode (SER/$\overline{\text{PAR}}$ = high, HW/$\overline{\text{SW}}$ = low), this input is used to serially write in, MSB first, the configuration data into the serial configuration register. The data on this input is latched with SCCLK. See the Software Configuration section.
27	D12 or SCCLK	DI/O	In parallel mode, this output is used as Bit 12 of the parallel port data output bus. Serial Configuration Clock. In serial software configuration mode (SER/$\overline{\text{PAR}}$ = high, HW/$\overline{\text{SW}}$ = low), this input is used to clock in the data on SCIN. The active edge where the data SCIN is updated depends on the logic state of the INVSCLK pin. See the Software Configuration section.
28	D13 or $\overline{\text{SCCS}}$	DI/O	In parallel mode, this output is used as Bit 13 of the parallel port data output bus. Serial Configuration Chip Select. In serial software configuration mode (SER/$\overline{\text{PAR}}$ = high, HW/$\overline{\text{SW}}$ = low), this input enables the serial configuration port. See the Software Configuration section.
29	BUSY	DO	Busy Output. Transitions high when a conversion is started and remains high until the conversion is completed and the data is latched into the on-chip shift register. The falling edge of BUSY can be used as a data-ready clock signal. Note that in master read after convert mode (SER/$\overline{\text{PAR}}$ = high, EXT/$\overline{\text{INT}}$ = low, RDC = low), the busy time changes according to Table 4.
30	TEN	DI[2]	Input Range Select. Used in conjunction with BIPOLAR per the following. **Input Range (V)** / **BIPOLAR** / **TEN** 0 to 5 / Low / Low 0 to 10 / Low / High ±5 / High / Low ±10 / High / High
31	$\overline{\text{RD}}$	DI	Read Data. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the interface parallel or serial output bus is enabled.
32	$\overline{\text{CS}}$	DI	Chip Select. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the interface parallel or serial output bus is enabled. $\overline{\text{CS}}$ is also used to gate the external clock in slave serial mode (not used for serial configurable port).
33	RESET	DI	Reset Input. When high, reset the AD7952. Current conversion, if any, is aborted. The falling edge of RESET resets the data outputs to all zeros (with OB/$\overline{\text{2C}}$ = high) and clears the configuration register. See the Digital Interface section. If not used, this pin can be tied to OGND.
34	PD	DI[2]	Power-Down Input. When PD = high, powers down the ADC. Power consumption is reduced and conversions are inhibited after the current one is completed. The digital interface remains active during power-down.
35	$\overline{\text{CNVST}}$	DI	Conversion Start. A falling edge on $\overline{\text{CNVST}}$ puts the internal sample-and-hold into the hold state and initiates a conversion.
36	BIPOLAR	DI[2]	Input Range Select. See description for Pin 30.

Pin No.	Mnemonic	Type[1]	Description
37	REF	AI/O	Reference Input/Output. When PDREF/PDBUF = low, the internal reference and buffer are enabled, producing 5 V on this pin. When PDREF/PDBUF = high, the internal reference and buffer are disabled, allowing an externally supplied voltage reference up to AVDD volts. Decoupling with at least a 22 µF capacitor is required with or without the internal reference and buffer. See the Reference Decoupling section.
38	REFGND	AI	Reference Input Analog Ground. Connected to analog ground plane.
39	IN−	AI	Analog Input. Referenced to IN+. In the 0 V to 5 V input range, IN− is between 0 V and V_{REF} V centered about $V_{REF}/2$. In the 0 V to 10 V range, IN− is between 0 V and 2 V_{REF} V centered about V_{REF}. In the ±5 V and ±10 V ranges, IN− is true bipolar up to ±2 V_{REF} V (±5 V range) or ±4 V_{REF} V (±10 V range) and centered about 0 V. In all ranges, IN− must be driven 180° out of phase with IN+.
40	VCC	P	High Voltage Positive Supply. Normally 7 V to 15 V.
41	VEE	P	High Voltage Negative Supply. Normally 0 V to −15 V (0 V in unipolar ranges).
43	IN+	AI	Analog Input. Referenced to IN−. In the 0 V to 5 V input range, IN+ is between 0 V and V_{REF} V centered about $V_{REF}/2$. In the 0 V to 10 V range, IN+ is between 0 V and 2 V_{REF} V centered about V_{REF}. In the ±5 V and ±10 V ranges, IN+ is true bipolar up to ±2 V_{REF} V (±5 V range) or ±4 V_{REF} V (±10 V range) and centered about 0 V. In all ranges, IN+ must be driven 180° out of phase with IN−.
45	TEMP	AO	Temperature Sensor Analog Output. When the internal reference is enabled (PDREF = PDBUF = low), this pin outputs a voltage proportional to the temperature of the AD7952. See the Temperature Sensor section.
46	REFBUFIN	AI	Reference Buffer Input. When using an external reference with the internal reference buffer (PDBUF = low, PDREF = high), applying 2.5 V on this pin produces 5 V on the REF pin. See the Single-to-Differential Driver section.
47	PDREF	DI	Internal Reference Power-Down Input. When low, the internal reference is enabled. When high, the internal reference is powered down, and an external reference must be used.
48	PDBUF	DI	Internal Reference Buffer Power-Down Input. When low, the buffer is enabled (must be low when using internal reference). When high, the buffer is powered down.
49	EPAD[3]	NC	Exposed Pad. The exposed pad is not connected internally. It is recommended that the pad be soldered to VEE.

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DI/O = bidirectional digital; DO = digital output; P = power.

[2] In serial configuration mode (SER/$\overline{PAR}$ = high, HW/$\overline{SW}$ = low), this input is programmed with the serial configuration register, and this pin is a don't care. See the Hardware Configuration section and Software Configuration section.

[3] LFCSP_VQ package only.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = DVDD = 5 V; OVDD = 5 V; VCC = 15 V; VEE = −15 V; V_{REF} = 5 V; T_A = 25°C.

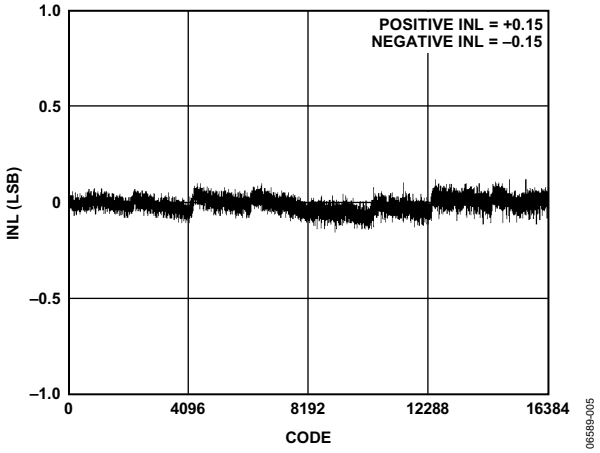


Figure 5. Integral Nonlinearity vs. Code

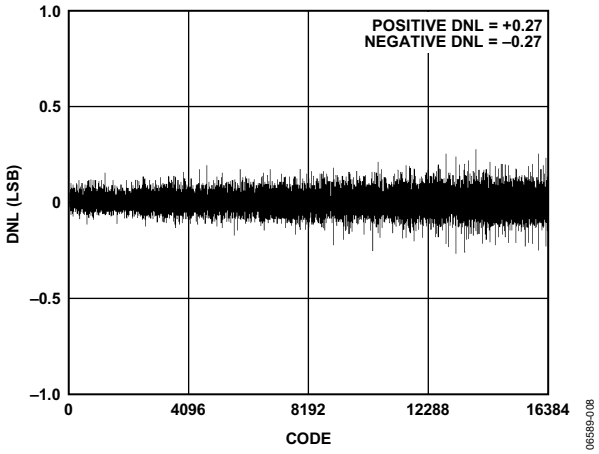


Figure 8. Differential Nonlinearity vs. Code

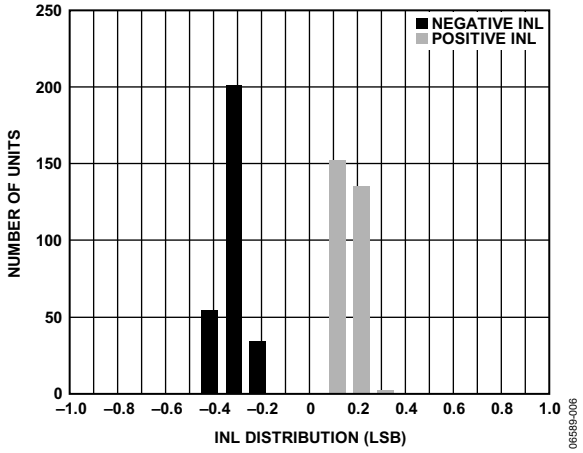


Figure 6. Integral Nonlinearity Distribution (239 Devices)

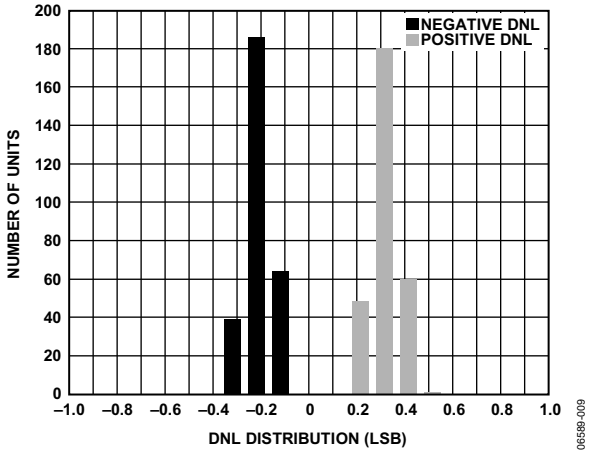


Figure 9. Differential Nonlinearity Distribution (239 Devices)

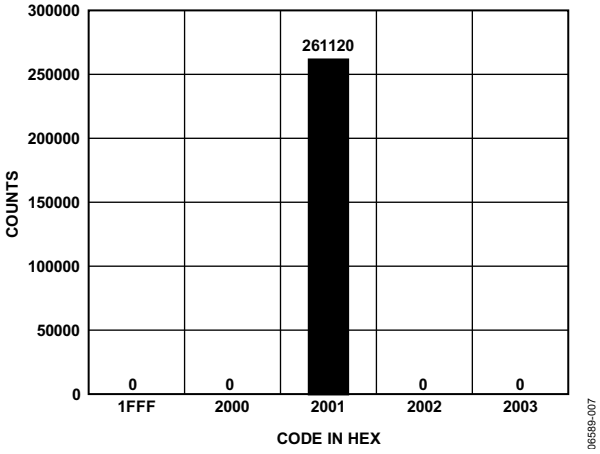


Figure 7. Histogram of 261,120 Conversions of a DC Input at the Code Center

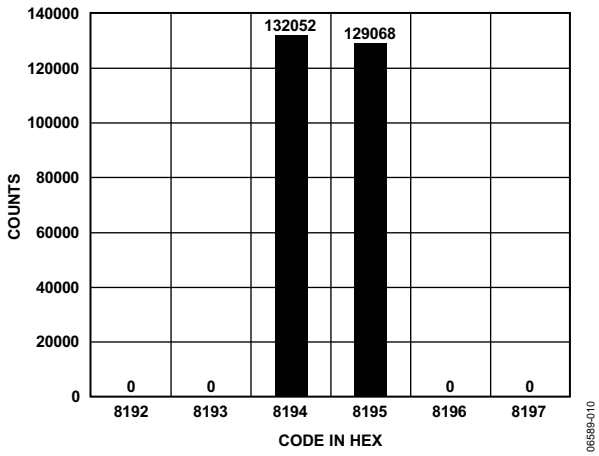


Figure 10. Histogram of 261,120 Conversions of a DC Input at the Code Transition

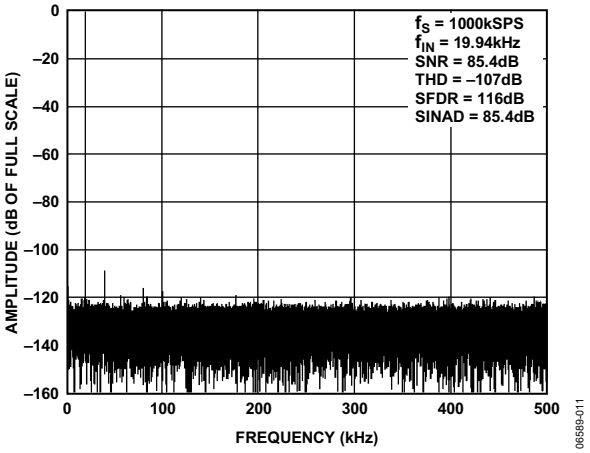


Figure 11. FFT 20 kHz

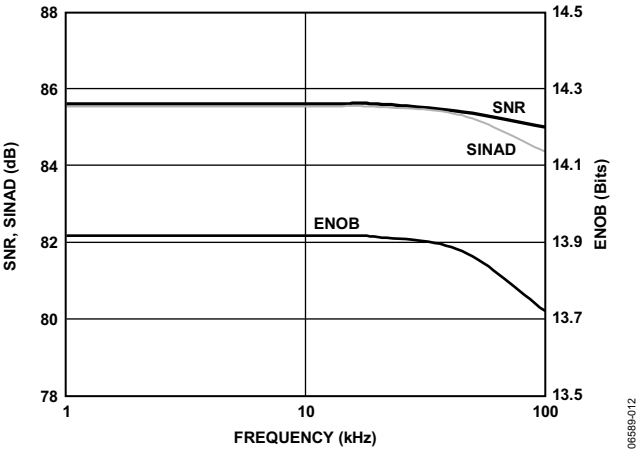


Figure 12. SNR, SINAD, and ENOB vs. Frequency

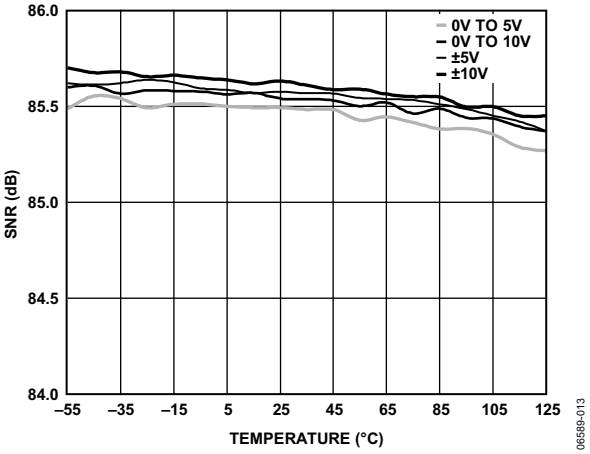


Figure 13. SNR vs. Temperature

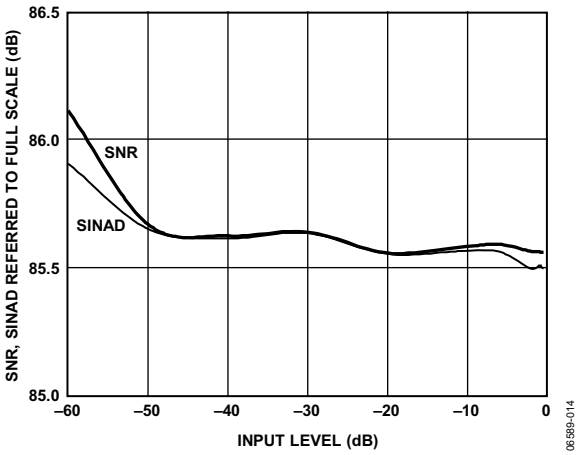


Figure 14. SNR and SINAD vs. Input Level (Referred to Full Scale)

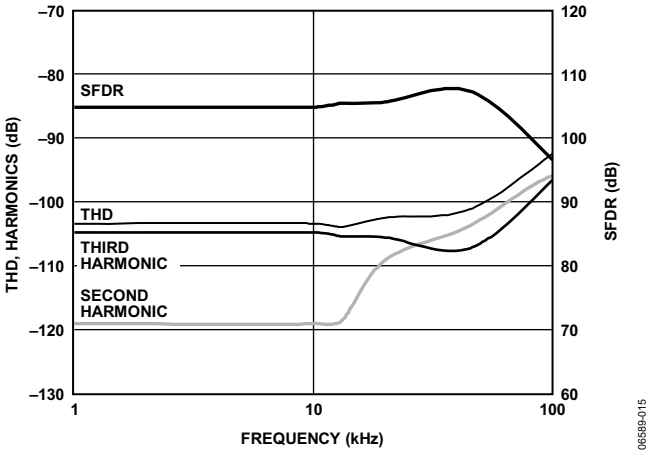


Figure 15. THD, Harmonics, and SFDR vs. Frequency

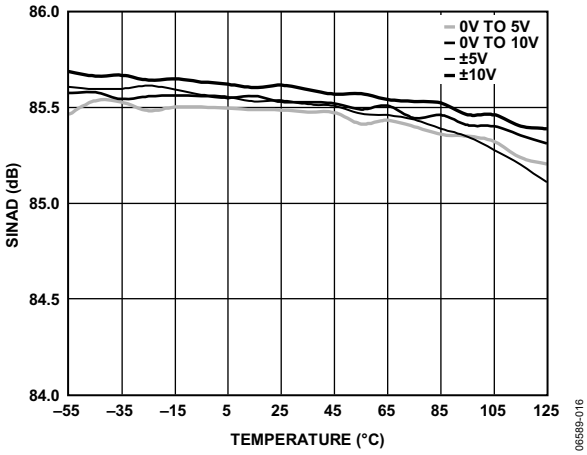


Figure 16. SINAD vs. Temperature

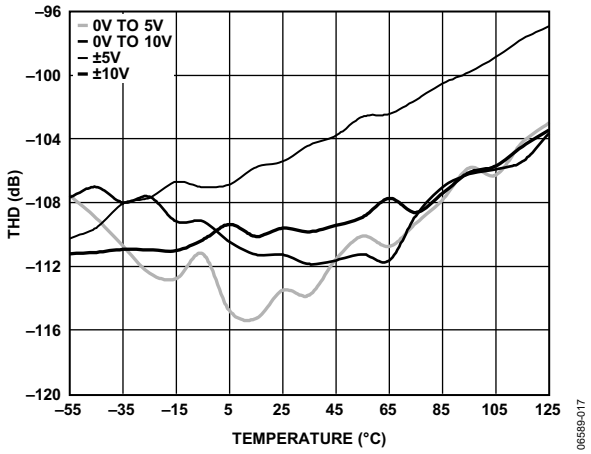


Figure 17. THD vs. Temperature

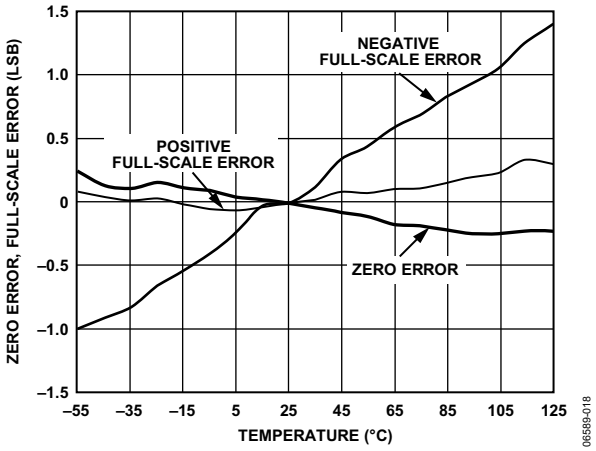


Figure 18. Zero Error, Positive and Negative Full-Scale Error vs. Temperature

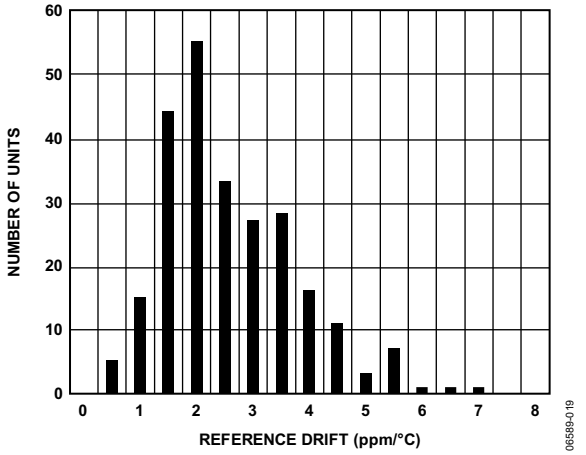


Figure 19. Reference Voltage Temperature Coefficient Distribution (247 Devices)

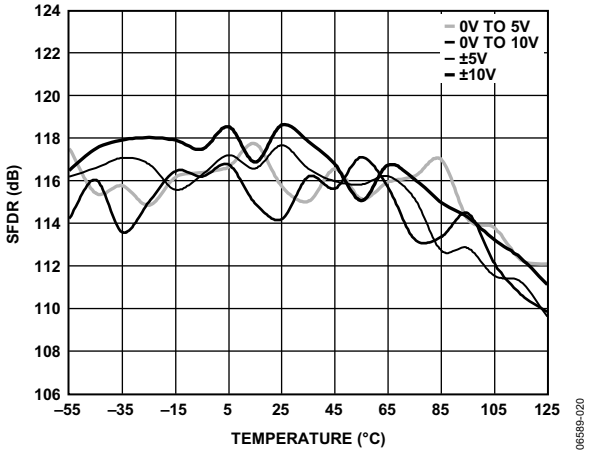


Figure 20. SFDR vs. Temperature (Excludes Harmonics)

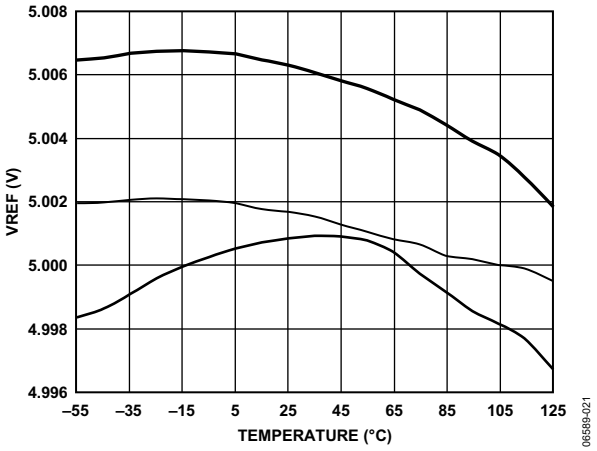


Figure 21. Typical Reference Voltage Output vs. Temperature (3 Devices)

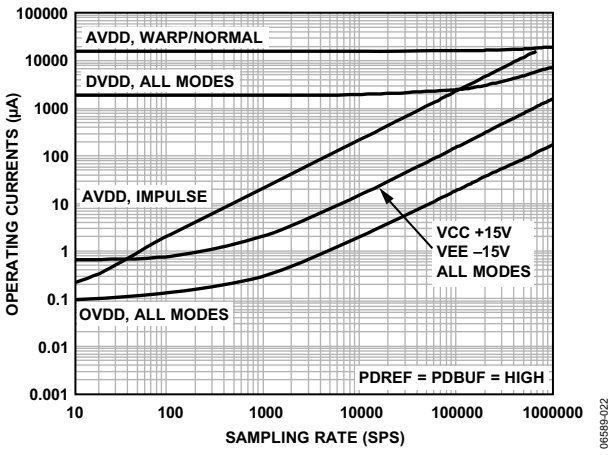


Figure 22. Operating Currents vs. Sample Rate

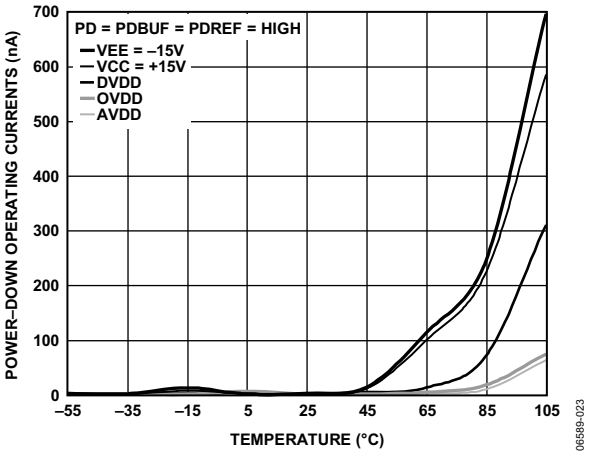


Figure 23. Power-Down Operating Currents vs. Temperature

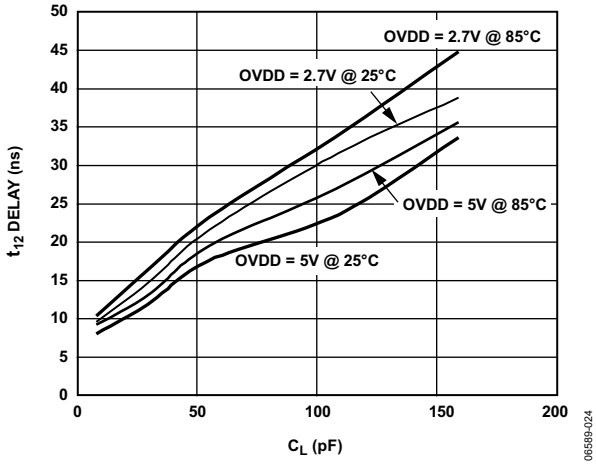


Figure 24. Typical Delay vs. Load Capacitance C_L

TERMINOLOGY

Least Significant Bit (LSB)

The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\,(V) = \frac{V_{INp\text{-}p}}{2^N}$$

Integral Nonlinearity Error (INL)

Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs a ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSBs beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Bipolar Zero Error

The difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Unipolar Offset Error

The first transition should occur at a level ½ LSB above analog ground. The unipolar offset error is the deviation of the actual transition from that point.

Full-Scale Error

The last transition (from 111…10 to 111…11) should occur for an analog voltage 1½ LSB below the nominal full scale. The full-scale error is the deviation in LSB (or % of full-scale range) of the actual level of the last transition from the ideal level and includes the effect of the offset error. Closely related is the gain error (also in LSB or % of full-scale range), which does not include the effects of the offset error.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the rms noise measured for an input typically at −60 dB. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

Aperture Delay

Aperture delay is a measure of the acquisition performance measured from the falling edge of the $\overline{CNVST}$ input to when the input signal is held for a conversion.

Transient Response

The time required for the AD7952 to achieve its rated accuracy after a full-scale step function is applied to its input.

Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the typical shift of the output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T (25°C), and T_{MAX}. It is expressed in ppm/°C as

$$TCV_{REF}(\text{ppm/}^\circ\text{C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25^\circ\text{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:

V_{REF} (*Max*) = maximum V_{REF} at T_{MIN}, T (25°C), or T_{MAX}.

V_{REF} (*Min*) = minimum V_{REF} at T_{MIN}, T (25°C), or T_{MAX}.

V_{REF} *(25°C)* = V_{REF} at 25°C.

T_{MAX} = +85°C.

T_{MIN} = −40°C.

THEORY OF OPERATION

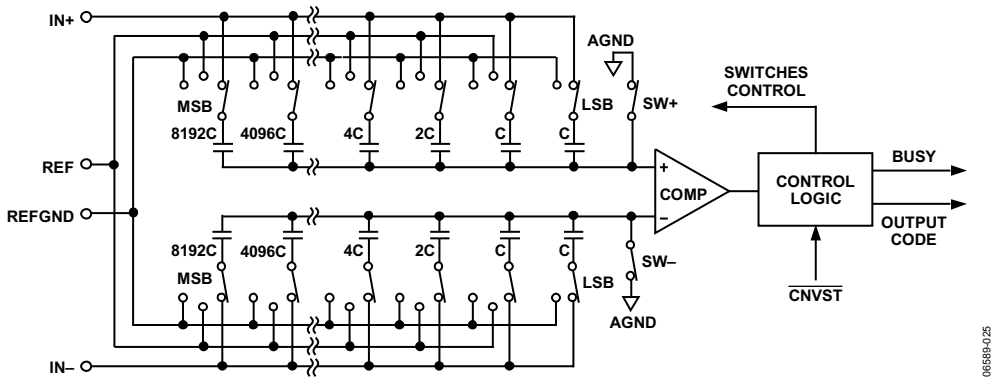


Figure 25. ADC Simplified Schematic

OVERVIEW

The AD7952 is a very fast, low power, precise, 14-bit ADC using successive approximation, capacitive digital-to-analog (CDAC) converter architecture.

The AD7952 can be configured at any time for one of four input ranges and conversion mode with inputs in parallel and serial hardware modes or by a dedicated write-only, SPI-compatible interface via a configuration register in serial software mode. The AD7952 uses Analog Devices' patented *i*CMOS high voltage process to accommodate 0 V to +5 V, 0 V to +10 V, ±5 V, and ±10 V input ranges without the use of conventional thin films. Only one acquisition cycle, t_8, is required for the inputs to latch to the correct configuration. Resetting or power cycling is not required for reconfiguring the ADC.

The AD7952 features different modes to optimize performance according to the applications. It is capable of converting 1,000,000 samples per second (1 MSPS) in warp mode, 800 kSPS in normal mode, and 670 kSPS in impulse mode.

The AD7952 provides the user with an on-chip, track-and-hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple, multiplexed channel applications.

For unipolar input ranges, the AD7952 typically requires three supplies: VCC, AVDD (which can supply DVDD), and OVDD (which can be interfaced to either 5 V, 3.3 V, or 2.5 V digital logic). For bipolar input ranges, the AD7952 requires the use of the additional VEE supply.

The device is housed in Pb-free, 48-lead LQFP or tiny, 48-lead LFCSP (7 mm × 7 mm) that combines space savings with flexibility. In addition, the AD7952 can be configured as either a parallel or a serial SPI-compatible interface.

CONVERTER OPERATION

The AD7952 is a successive approximation ADC based on a charge redistribution DAC. Figure 25 shows the simplified schematic of the ADC. The CDAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW+ and SW−. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN+ and IN− inputs. A conversion phase is initiated once the acquisition phase is completed and the $\overline{\text{CNVST}}$ input goes low. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the inputs (IN+ and IN−) captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ through $V_{REF}/16{,}384$). The control logic toggles these switches, starting with the MSB first, to bring the comparator back into a balanced condition.

After the completion of this process, the control logic generates the ADC output code and brings the BUSY output low.

MODES OF OPERATION

The AD7952 features three modes of operation: warp, normal, and impulse. Each of these modes is more suitable to specific applications. The mode is configured with the input pins, WARP and IMPULSE, or via the configuration register. See Table 6 for the pin details and the Hardware Configuration section and Software Configuration section for programming the mode selection with either pins or configuration register. Note that when using the configuration register, the WARP and IMPULSE inputs are don't cares and should be tied to either high or low.

Warp Mode

Setting WARP = high and IMPULSE = low allows the fastest conversion rate up to 1 MSPS. However, in this mode, the full specified accuracy is guaranteed only when the time between conversions does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms (after power-up), the first conversion result should be ignored because in warp mode, the ADC performs a background calibration during the SAR conversion process. This calibration can drift if the time between conversions exceeds 1 ms, thus causing the first conversion to appear offset. This mode makes the AD7952 ideal for applications where both high accuracy and fast sample rate are required.

Normal Mode

Setting WARP = IMPULSE = low or WARP = IMPULSE = high allows the fastest mode (800 kSPS) without any limitation on time between conversions. This mode makes the AD7952 ideal for asynchronous applications, such as data acquisition systems, where both high accuracy and fast sample rate are required.

Impulse Mode

Setting WARP = low and IMPULSE = high uses the lowest power dissipation mode and allows power saving between conversions. The maximum throughput in this mode is 670 kSPS, and in this mode, the ADC powers down circuits after conversion, making the AD7952 ideal for battery-powered applications.

TRANSFER FUNCTIONS

Using the OB/$\overline{2C}$ digital input or via the configuration register, the AD7952 offers two output codings: straight binary and twos complement. See Figure 26 and Table 7 for the ideal transfer characteristic and digital output codes for the different analog input ranges, V_{IN}. Note that when using the configuration register, the OB/$\overline{2C}$ input is a don't care and should be tied to either high or low.

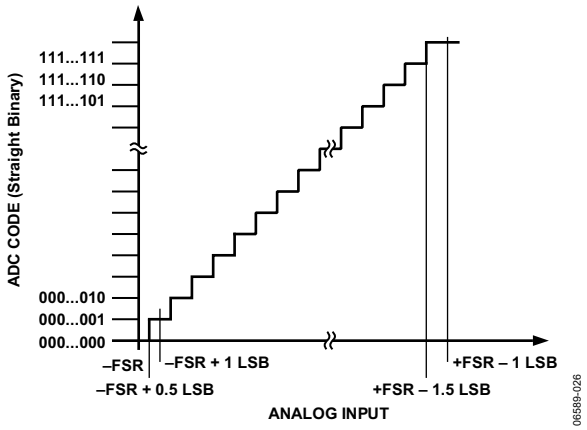


Figure 26. ADC Ideal Transfer Function

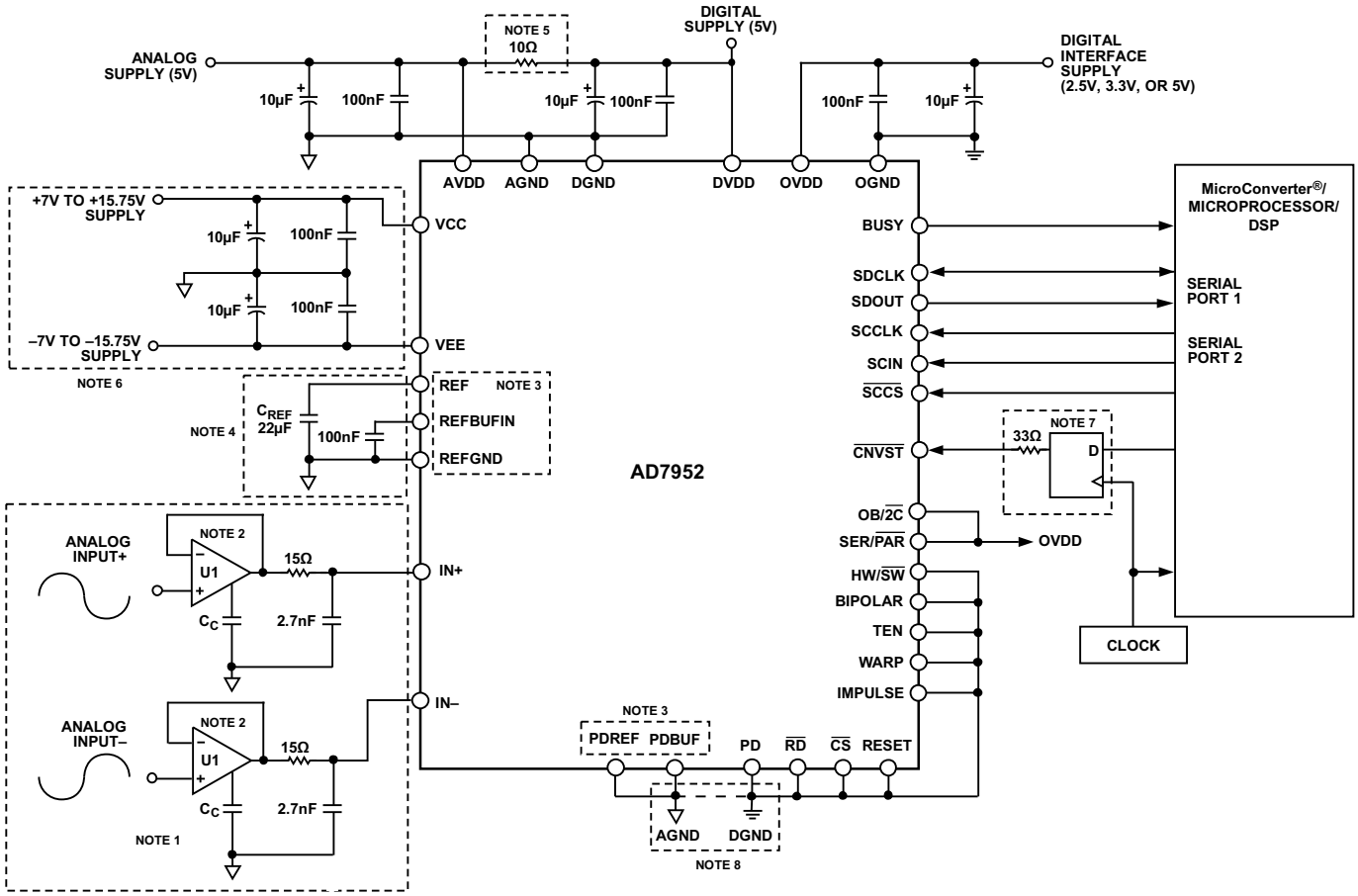
TYPICAL CONNECTION DIAGRAM

Figure 27 shows a typical connection diagram for the AD7952 using the internal reference, serial data, and serial configuration interfaces. Different circuitry from that shown in Figure 27 is optional and is discussed in the following sections.

Table 7. Output Codes and Ideal Input Voltages

	V_{REF} = 5 V				Digital Output Code	
Description	**V_{IN} = 0 V to 5 V (10 V p-p)**	**V_{IN} = 0 V to 10 V (20 V p-p)**	**V_{IN} = ±5 V (20 V p-p)**	**V_{IN} = ±10 V (40 V p-p)**	**Straight Binary**	**Twos Complement**
FSR – 1 LSB	4.999695 V	9.999389 V	+4.999389 V	+9.998779 V	0x3FFF[1]	0x1FFF[1]
FSR – 2 LSB	4.999390 V	9.998779 V	+4.998779 V	+9.997558 V	0x3FFE	0x1FFE
Midscale + 1 LSB	2.500610 V	5.000610 V	+1.228 mV	+2.442 mV	0x2001	0x0001
Midscale	2.5 V	5.000000 V	0 V	0 V	0x2000	0x0000
Midscale – 1 LSB	2.499390 V	4.999389 V	–1.228 mV	–2.442 mV	0x1FFF	0x3FFF
–FSR + 1 LSB	610.4 µV	1.228 mV	–4.999389 V	–9.998779 V	0x0001	0x2001
–FSR	0 V	0 V	–5 V	–10 V	0x0000[2]	0x2000[2]

[1] This is also the code for overrange analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{REFGND}).
[2] This is also the code for overrange analog input (V_{IN+} – V_{IN-} below V_{REF} – V_{REFGND}).



NOTES
1. ANALOG INPUTS ARE DIFFERENTIAL (ANTIPHASE). SEE ANALOG INPUTS SECTION.
2. THE AD8021 IS RECOMMENDED. SEE DRIVER AMPLIFIER CHOICE SECTION.
3. THE CONFIGURATION SHOWN IS USING THE INTERNAL REFERENCE. SEE VOLTAGE REFERENCE INPUT/OUTPUT SECTION.
4. A 22µF CERAMIC CAPACITOR (X5R, 1206 SIZE) IS RECOMMENDED (FOR EXAMPLE, PANASONIC ECJ4YB1A226M). SEE VOLTAGE REFERENCE INPUT/OUTPUT SECTION.
5. OPTIONAL, SEE POWER SUPPLIES SECTION.
6. THE VCC AND VEE SUPPLIES SHOULD BE VCC = [VIN(MAX) + 2V] AND VEE = [VIN(MIN) – 2V] FOR BIPOLAR INPUT RANGES. FOR UNIPOLAR INPUT RANGES, VEE CAN BE 0V. SEE POWER SUPPLIES SECTION.
7. OPTIONAL LOW JITTER $\overline{CNVST}$, SEE CONVERSION CONTROL SECTION.
8. A SEPARATE ANALOG AND DIGITAL GROUND PLANE IS RECOMMENDED, CONNECTED TOGETHER DIRECTLY UNDER THE ADC. SEE LAYOUT GUIDELINES SECTION.

06589-027

Figure 27. Typical Connection Diagram Shown with Serial Interface and Serial Programmable Port

ANALOG INPUTS

Input Range Selection

In parallel mode and serial hardware mode, the input range is selected by using the BIPOLAR (bipolar) and TEN (10 V range) inputs. See Table 6 for pin details and the Hardware Configuration section and Software Configuration section for programming the mode selection with either pins or the configuration register. Note that when using the configuration register, the BIPOLAR and TEN inputs are don't cares and should be tied high or low.

Input Structure

Figure 28 shows an equivalent circuit for the input structure of the AD7952.

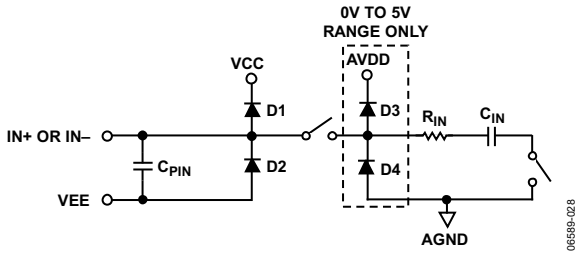


Figure 28. Simplified Analog Input

The four diodes, D1 to D4, provide ESD protection for the analog inputs, IN+ and IN–. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V because this causes the diodes to become forward-biased and to start conducting current. These diodes can handle a forward-biased current of 120 mA maximum. For instance, these conditions could eventually occur when the input buffer's U1 supplies are different from AVDD, VCC, and VEE. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part although most op amps' short-circuit current is <100 mA. Note that D3 and D4 are only used in the 0 V to 5 V range to allow for additional protection in applications that are switching from the higher voltage ranges.

This analog input structure allows the sampling of the differential signal between IN+ and IN–. By using this differential input, small signals common to both inputs are rejected as shown in Figure 29, which represents the typical CMRR over frequency. For instance, by using IN– to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated.

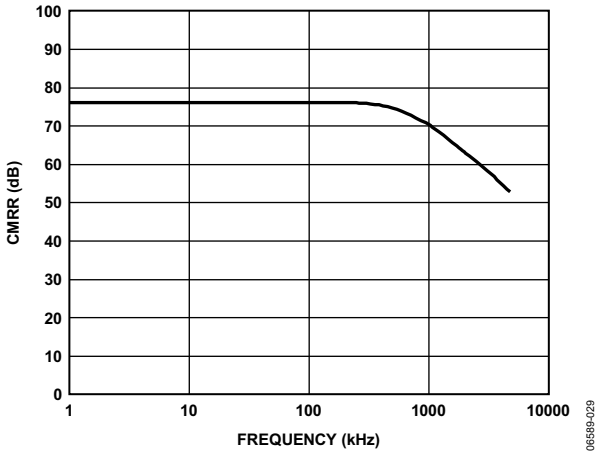


Figure 29. Analog Input CMRR vs. Frequency

During the acquisition phase for ac signals, the impedance of the analog inputs, IN+ and IN–, can be modeled as a parallel combination of Capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 70 Ω and is a lumped component comprised of serial resistors and the on resistance of the switches. C_{IN} is primarily the ADC sampling capacitor and depending on the input range selected is typically 48 pF in the 0 V to +5 V range, typically 24 pF in the 0 V to +10 V and ±5 V ranges, and typically 12 pF in the ±10 V range. During the conversion phase, when the switches are opened, the input impedance is limited to C_{PIN}.

Because the input impedance of the AD7952 is very high, it can be directly driven by a low impedance source without gain error. To further improve the noise filtering achieved by the AD7952 analog input circuit, an external, 1-pole RC filter between the amplifier's outputs and the ADC analog inputs can be used, as shown in Figure 27. However, large source impedances significantly affect the ac performance, especially THD. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7952 is easy to drive, the driver amplifier must meet the following requirements:

- For multichannel, multiplexed applications, the driver amplifier and the AD7952 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 14-bit level (0.006%). For the amplifier, settling at 0.1% to 0.01% is more commonly specified. This differs significantly from the settling time at a 14-bit level and should be verified prior to driver selection. The AD8021 op amp combines ultralow noise and high gain bandwidth and meets this settling time requirement even when used with gains of up to 13.
- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7952. The noise coming from the driver is filtered by the external 1-pole, low-pass filter, as shown in Figure 27. The SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20\log\left(\frac{V_{NADC}}{\sqrt{V_{NADC}^2 + \frac{\pi}{2} f_{-3dB}(Ne_{N+})^2 + \frac{\pi}{2} f_{-3dB}(Ne_{N-})^2}}\right)$$

where:

V_{NADC} is the noise of the ADC, which is:

$$V_{NADC} = \frac{\frac{V_{INp\text{-}p}}{2\sqrt{2}}}{10^{\frac{SNR}{20}}}$$

f_{-3dB} is the cutoff frequency of the input filter (3.9 MHz).

N is the noise factor of the amplifier (1 in the buffer configuration).

e_{N+} and e_{N-} are the equivalent input voltage noise densities of the op amps connected to IN+ and IN−, in nV/√Hz.

When the resistances used around the amplifiers are small, this approximation can be used. If larger resistances are used, their noise contributions should also be root-sum squared.

- The driver needs to have a THD performance suitable to that of the AD7952. Figure 15 shows the THD vs. frequency that the driver should exceed.

The AD8021 meets these requirements and is appropriate for almost all applications. The AD8021 needs a 10 pF external compensation capacitor that should have good linearity as an NPO ceramic or mica type. Moreover, the use of a noninverting +1 gain arrangement is recommended and helps to obtain the best SNR.

The AD8022 can also be used when a dual version is needed and a gain of 1 is present. The AD829 is an alternative in applications where high frequency performance (above 100 kHz) is not required. In applications with a gain of 1, an 82 pF compensation capacitor is required. The AD8610 is an option when low bias current is needed in low frequency applications.

Because the AD7952 uses a large geometry, high voltage input switch, the best linearity performance is obtained when using the amplifier at its maximum full power bandwidth. Gaining the amplifier to make use of the more dynamic range of the ADC results in increased linearity errors. For applications requiring more resolution, the use of an additional amplifier with gain should precede a unity follower driving the AD7952. See Table 8 for a list of recommended op amps.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
AD829	±15 V supplies, very low noise, low frequency
AD8021	±12 V supplies, very low noise, high frequency
AD8022	±12 V supplies, very low noise, high frequency, dual
ADA4922-1	±12 V supplies, low noise, high frequency, single-ended-to-differential driver
AD8610/ AD8620	±13 V supplies, low bias current, low frequency, single/dual

Single-to-Differential Driver

For single-ended sources, a single-to-differential driver, such as the ADA4922-1, can be used because the AD7952 needs to be driven differentially. The 1-pole filter using R = 15 Ω and C = 2.7 nF provides a corner frequency of 3.9 MHz.

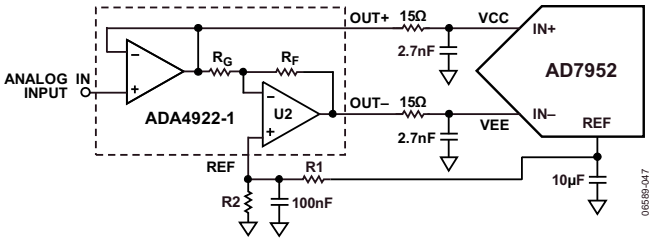


Figure 30. Single-to-Differential Driver Using the ADA4922-1

For unipolar 5 V and 10 V input ranges, the internal (or external) reference source can be used to level shift U2 for the correct input span. If using an external reference, the values for R1/R2 can be lowered to reduce resistive Johnson noise (1.29E − 10 × √R). For the bipolar ±5 V and ±10 V input ranges, the reference connection is not required because the common-mode voltage is 0 V. See Table 9 for R1/R2 for the different input ranges.

Table 9. R1/R2 Configuration

Input Range (V)	R1 (Ω)	R2 (Ω)	Common-Mode Voltage (V)
5	2.5 k	2.5 k	2.5
10	2.5 k	Open	5
±5, ±10		100	0

This circuit can also be made discretely, and thus more flexible, using any of the recommended low noise amplifiers in Table 8. Again, to preserve the SNR of the converter, the resistors, R_F and R_G, should be kept low.

VOLTAGE REFERENCE INPUT/OUTPUT

The AD7952 allows the choice of either a very low temperature drift internal voltage reference, an external reference, or an external buffered reference.

The internal reference of the AD7952 provides excellent performance and can be used in almost all applications. However, the linearity performance is guaranteed only with an external reference.

Internal Reference (REF = 5 V, PDREF = Low, PDBUF = Low)

To use the internal reference, the PDREF and PDBUF inputs must be low. This enables the on-chip, band gap reference, buffer, and TEMP sensor, resulting in a 5.00 V reference on the REF pin.

The internal reference is temperature-compensated to 5.000 V ± 35 mV. The reference is trimmed to provide a typical drift of 3 ppm/°C. This typical drift characteristic is shown in Figure 19.

External 2.5 V Reference and Internal Buffer (REF = 5 V, PDREF = High, PDBUF = Low)

To use an external reference with the internal buffer, PDREF should be high and PDBUF should be low. This powers down the internal reference and allows the 2.5 V reference to be applied to REFBUFIN, producing 5 V on the REF pin. The internal reference buffer is useful in multiconverter applications because a buffer is typically required in these applications.

External 5 V Reference (PDREF = High, PDBUF = High)

To use an external reference directly on the REF pin, PDREF and PDBUF should both be high. PDREF and PDBUF power down the internal reference and the internal reference buffer, respectively. For improved drift performance, an external reference, such as the ADR445 or the ADR435, is recommended.

Reference Decoupling

Whether using an internal or external reference, the AD7952 voltage reference input (REF) has a dynamic input impedance; therefore, it should be driven by a low impedance source with efficient decoupling between the REF and REFGND inputs. This decoupling depends on the choice of the voltage reference but usually consists of a low ESR capacitor connected to REF and REFGND with minimum parasitic inductance. A 22 µF (X5R, 1206 size) ceramic chip capacitor (or 47 µF tantalum capacitor) is appropriate when using either the internal reference or the ADR445/ADR435 external reference.

The placement of the reference decoupling is also important to the performance of the AD7952. The decoupling capacitor should be mounted on the same side as the ADC, right at the REF pin with a thick PCB trace. The REFGND should also connect to the reference decoupling capacitor with the shortest distance and to the analog ground plane with several vias.

For applications that use multiple AD7952s or other PulSAR devices, it is more effective to use the internal reference buffer to buffer the external 2.5 V reference voltage.

The voltage reference temperature coefficient (TC) directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the TC. For instance, a ±60 ppm/°C TC of the reference changes full scale by ±1 LSB/°C.

Temperature Sensor

When the internal reference is enabled (PDREF = PDBUF = low), the on-chip temperature sensor output (TEMP) is enabled and can be use to measure the temperature of the AD7952. To improve the calibration accuracy over the temperature range, the output of the TEMP pin is applied to one of the inputs of the analog switch (such as ADG779), and the ADC itself is used to measure its own temperature. This configuration is shown in Figure 31.

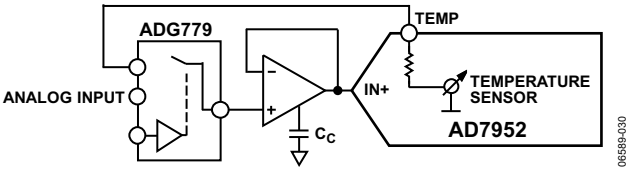


Figure 31. Use of the Temperature Sensor

POWER SUPPLIES

The AD7952 uses five sets of power supply pins:

- AVDD: analog 5 V core supply
- VCC: analog high voltage, positive supply
- VEE: high voltage, negative supply
- DVDD: digital 5 V core supply
- OVDD: digital input/output interface supply

Core Supplies

The AVDD and DVDD supply the AD7952 analog and digital cores, respectively. Sufficient decoupling of these supplies is required, consisting of at least a 10 µF capacitor and a 100 nF capacitor on each supply. The 100 nF capacitors should be placed as close as possible to the AD7952. To reduce the number of supplies needed, the DVDD can be supplied through a simple RC filter from the analog supply, as shown in Figure 27.

High Voltage Supplies

The high voltage bipolar supplies, VCC and VEE, are required and must be at least 2 V larger than the maximum input, V_{IN}. For example, if using the bipolar 10 V range, the supplies should be ±12 V minimum. Sufficient decoupling of these supplies is also required, consisting of at least a 10 µF capacitor and a 100 nF capacitor on each supply. For unipolar operation, the VEE supply can be grounded with some slight THD performance degradation.

Digital Output Supply

The OVDD supplies the digital outputs and allows direct interface with any logic working between 2.3 V and 5.25 V.

OVDD should be set to the same level as the system interface. Sufficient decoupling is required, consisting of at least a 10 µF capacitor and a 100 nF capacitor with the 100 nF capacitors placed as close as possible to the AD7952.

Power Sequencing

The AD7952 requires sequencing of the AVDD and DVDD supplies. AVDD should come up prior to or simultaneously with DVDD. This can be achieved using the configuration in Figure 27 or sequencing the supplies in that manner. The other supplies can be sequenced as desired as long as absolute maximum ratings are observed. The AD7952 is very insensitive to power supply variations on AVDD over a wide frequency range, as shown in Figure 32.

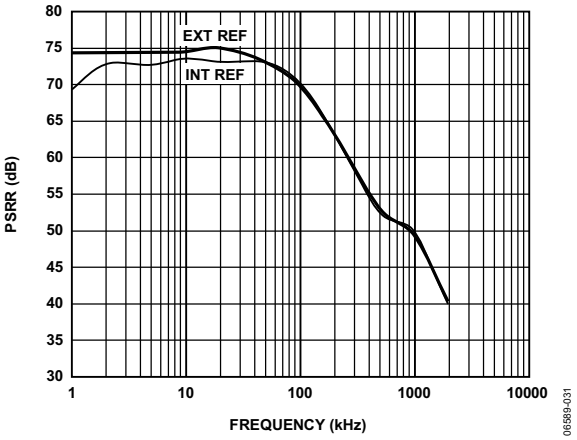


Figure 32. AVDD PSRR vs. Frequency

Power Dissipation vs. Throughput

In impulse mode, the AD7952 automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low, which allows a significant power savings when the conversion rate is reduced (see Figure 33). This feature makes the AD7952 ideal for very low power, battery-operated applications.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, drive the digital inputs close to the power rails (that is, OVDD and OGND).

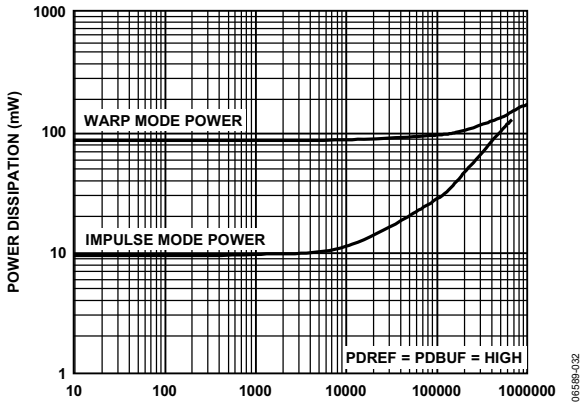


Figure 33. Power Dissipation vs. Sample Rate

Power Down

Setting PD = high powers down the AD7952, thus reducing supply currents to their minimums, as shown in Figure 23. When the ADC is in power-down, the current conversion (if any) is completed and the digital bus remains active. To further reduce the digital supply currents, drive the inputs to OVDD or OGND.

Power-down can also be programmed with the configuration register. See the Software Configuration section for details. Note that when using the configuration register, the PD input is a don't care and should be tied to either high or low.

CONVERSION CONTROL

The AD7952 is controlled by the $\overline{CNVST}$ input. A falling edge on $\overline{CNVST}$ is all that is necessary to initiate a conversion. A detailed timing diagram of the conversion process is shown in Figure 34. Once initiated, it cannot be restarted or aborted, even by the power-down input, PD, until the conversion is completed. The $\overline{CNVST}$ signal operates independently of the $\overline{CS}$ and $\overline{RD}$ signals.

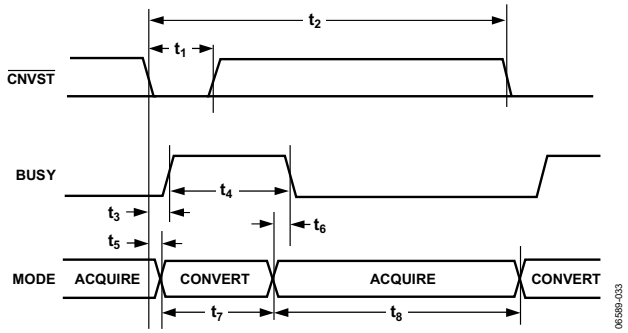


Figure 34. Basic Conversion Timing

Although $\overline{CNVST}$ is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot, undershoot, or ringing.

The $\overline{CNVST}$ trace should be shielded with ground, and a low value (such as 50 Ω) serial resistor termination should be added close to the output of the component that drives this line.

For applications where SNR is critical, the $\overline{CNVST}$ signal should have very low jitter. This can be achieved by using a dedicated oscillator for $\overline{CNVST}$ generation, or by clocking $\overline{CNVST}$ with a high frequency, low jitter clock, as shown in Figure 27.

INTERFACES

DIGITAL INTERFACE

The AD7952 has a versatile digital interface that can be set up as either a serial or a parallel interface with the host system. The serial interface is multiplexed on the parallel data bus. The AD7952 digital interface also accommodates 2.5 V, 3.3 V, or 5 V logic. In most applications, the OVDD supply pin is connected to the host system interface 2.5 V to 5.25 V digital supply. Finally, by using the OB/$\overline{2C}$ input pin, both twos complement or straight binary coding can be used.

Two signals, $\overline{CS}$ and $\overline{RD}$, control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{CS}$ allows the selection of each AD7952 in multicircuit applications and is held low in a single AD7952 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus.

RESET

The RESET input is used to reset the AD7952. A rising edge on RESET aborts the current conversion (if any) and tristates the data bus. The falling edge of RESET resets the AD7952 and clears the data bus and configuration register. See Figure 35 for the RESET timing details.

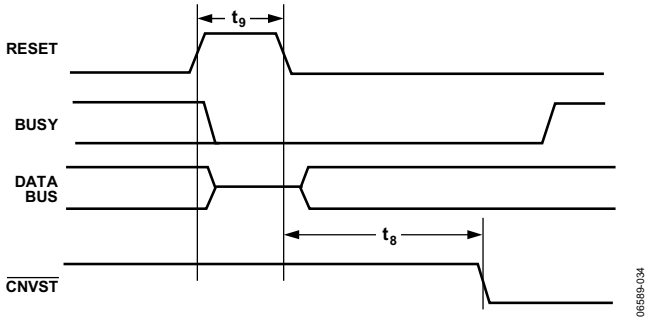


Figure 35. RESET Timing

PARALLEL INTERFACE

The AD7952 is configured to use the parallel interface when SER/$\overline{PAR}$ is held low.

Master Parallel Interface

Data can be continuously read by tying $\overline{CS}$ and $\overline{RD}$ low, thus requiring minimal microprocessor connections. However, in this mode, the data bus is always driven and cannot be used in shared bus applications (unless the device is held in RESET). Figure 36 details the timing for this mode.

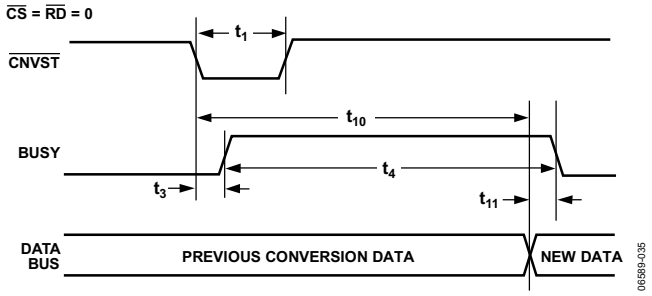


Figure 36. Master Parallel Data Timing for Reading (Continuous Read)

Slave Parallel Interface

In slave parallel reading mode, the data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion, as shown in Figure 37 and Figure 38, respectively. When the data is read during the conversion, it is recommended that it is read-only during the first half of the conversion phase. This avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

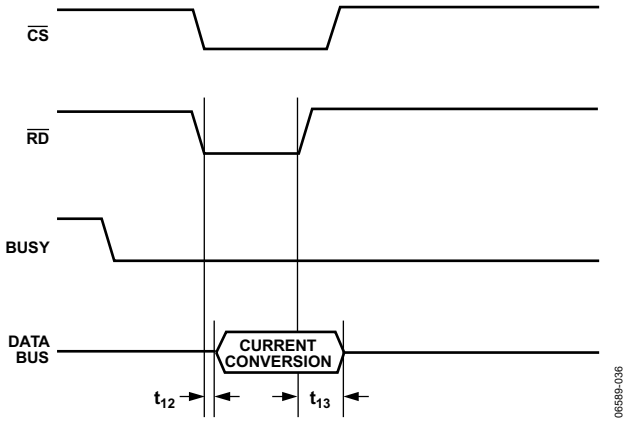


Figure 37. Slave Parallel Data Timing for Reading (Read After Convert)

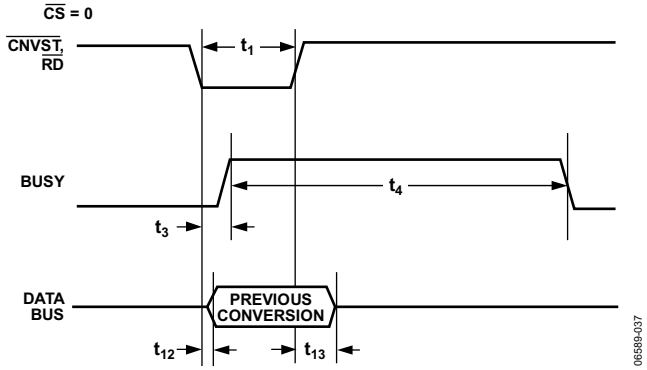


Figure 38. Slave Parallel Data Timing for Reading (Read During Convert)

8-Bit Interface (Master or Slave)

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 39, when BYTESWAP is low, the LSB byte is output on D[7:0] and the MSB is output on D[13:8]. When BYTESWAP is high, the LSB and MSB bytes are swapped; the LSB is output on D[13:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 14-bit data can be read in two bytes on either D[13:8] or D[7:0]. This interface can be used in both master and slave parallel reading modes.

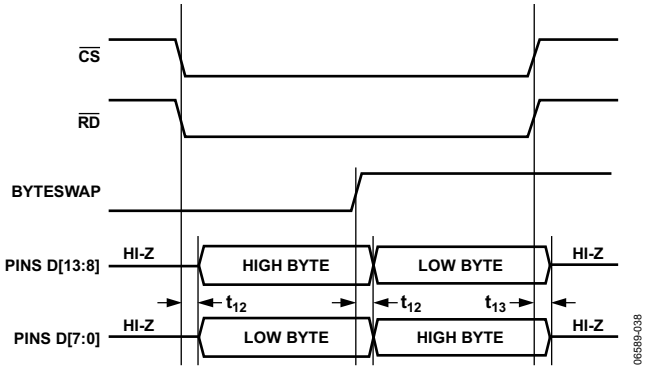


Figure 39. 8-Bit and 14-Bit Parallel Interface

SERIAL INTERFACE

The AD7952 has a serial interface (SPI-compatible) multiplexed on the data pins D[13:0]. The AD7952 is configured to use the serial interface when SER/$\overline{\text{PAR}}$ is held high.

Data Interface

The AD7952 outputs 14 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 14 clock pulses provided on the SDCLK pin. The output data is valid on both the rising and falling edge of the data clock.

Serial Configuration Interface

The AD7952 can be configured through the serial configuration register only in serial mode, because the serial configuration pins are also multiplexed on the data pins D[13:10]. See the Hardware Configuration section and Software Configuration section for more information.

MASTER SERIAL INTERFACE

The pins multiplexed on D[8:0] and used for master serial interface are: DIVSCLK[0], DIVSCLK[1], EXT/$\overline{\text{INT}}$, INVSYNC, INVSCLK, RDC, SDOUT, SDCLK, and SYNC.

Internal Clock (SER/$\overline{\text{PAR}}$ = High, EXT/$\overline{\text{INT}}$ = Low)

The AD7952 is configured to generate and provide the serial data clock, SDCLK, when the EXT/$\overline{\text{INT}}$ pin is held low. The AD7952 also generates a SYNC signal to indicate to the host when the serial data is valid. The SDCLK and the SYNC signals can be inverted, if desired, using the INVSCLK and INVSYNC inputs, respectively. Depending on the input, RDC, the data can be read during the following conversion or after each conversion. Figure 40 and Figure 41 show detailed timing diagrams of these two modes.

Read During Convert (RDC = High)

Setting RDC = high allows the master read (previous conversion result) during conversion mode. Usually, because the AD7952 is used with a fast throughput, this mode is the most recommended serial mode. In this mode, the serial clock and data toggle at appropriate instances, minimizing potential feedthrough between digital activity and critical conversion decisions. In this mode, the SDCLK period changes because the LSBs require more time to settle and the SDCLK is derived from the SAR conversion cycle. In this mode, the AD7952 generates a discontinuous SDCLK of two different periods and the host should use an SPI interface.

Read After Convert (RDC = Low, DIVSCLK[1:0] = [0 to 3])

Setting RDC = low allows the read after conversion mode. Unlike the other serial modes, the BUSY signal returns low after the 14 data bits are pulsed out and not at the end of the conversion phase, resulting in a longer BUSY width (refer to Table 4 for BUSY timing specifications). The DIVSCLK[1:0] inputs control the SDCLK period and SDOUT data rate. As a result, the maximum throughput cannot be achieved in this mode. In this mode, the AD7952 also generates a discontinuous SDCLK; however, a fixed period and hosts supporting both SPI and serial ports can also be used.

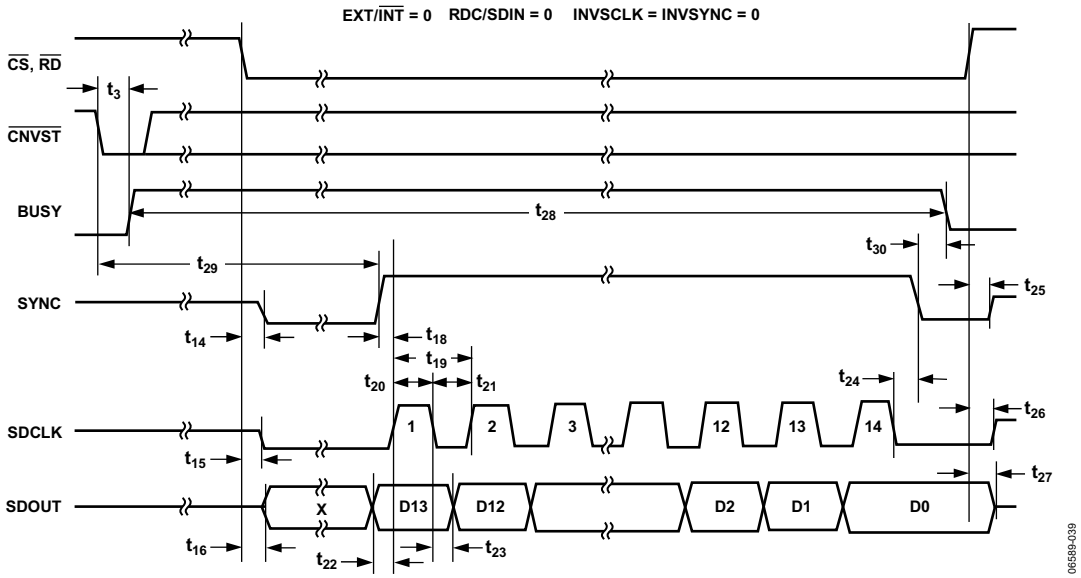


Figure 40. Master Serial Data Timing for Reading (Read After Convert)

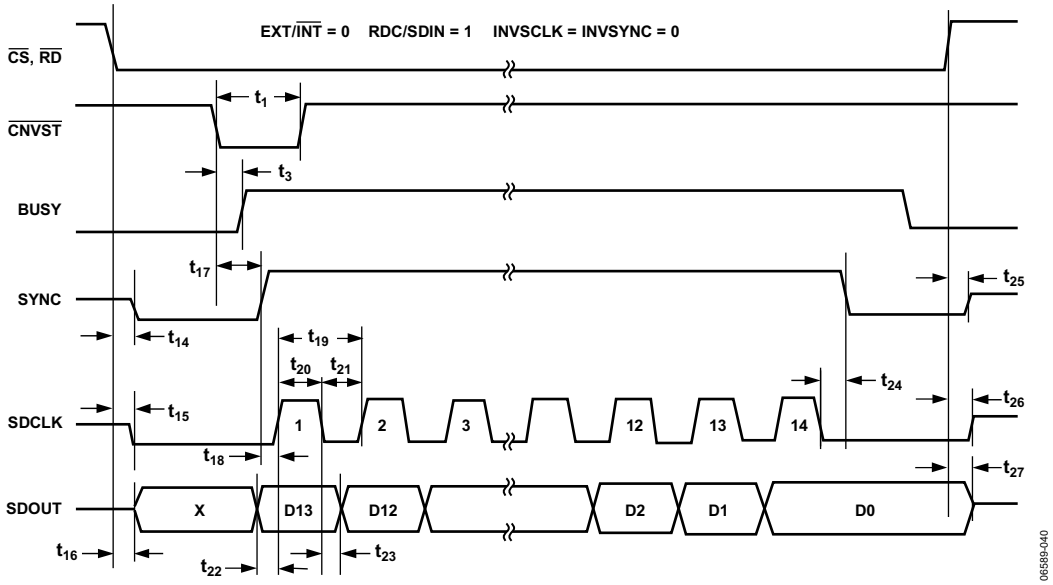


Figure 41. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

SLAVE SERIAL INTERFACE

The pins multiplexed on D[19:2] used for slave serial interface are: EXT/$\overline{\text{INT}}$, INVSCLK, SDIN, SDOUT, SDCLK, and RDERROR.

External Clock (SER/$\overline{\text{PAR}}$ = High, EXT/$\overline{\text{INT}}$ = High)

Setting the EXT/$\overline{\text{INT}}$ = high allows the AD7952 to accept an externally supplied serial data clock on the SDCLK pin. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{\text{CS}}$. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the data can be read after each conversion or during the following conversion. A clock can be either normally high or normally low when inactive. For detailed timing diagrams, see Figure 43 and Figure 44.

While the AD7952 is performing a bit decision, it is important that voltage transients be avoided on digital input/output pins or degradation of the conversion result may occur. This is particularly important during the last 450 ns of the conversion phase because the AD7952 provides error correction circuitry that can correct for an improper bit decision made during the first part of the conversion phase. For this reason, it is recommended that any external clock provided is a discontinuous clock that transitions only when BUSY is low or, more importantly, that it does not transition during the last 450 ns of BUSY high.

External Discontinuous Clock Data Read After Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 43 shows the detailed timing diagrams for this method. After a conversion is complete, indicated by BUSY returning low, the conversion result can be read while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low. Data is shifted out MSB first with 14 clock pulses and, depending on the SDCLK frequency, can be valid on the falling and rising edges of the clock.

One advantage of this method is that conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Another advantage is the ability to read the data at any speed up to 40 MHz, which accommodates both the slow digital host interface and the fastest serial reading.

Daisy-Chain Feature

Also in the read after convert mode, the AD7952 provides a daisy-chain feature for cascading multiple converters together using the serial data input pin, SDIN. This feature is useful for reducing component count and wiring connections when desired, for instance, in isolated multiconverter applications. See Figure 43 for the timing details.

An example of the concatenation of two devices is shown in Figure 42.

Simultaneous sampling is possible by using a common $\overline{\text{CNVST}}$ signal. Note that the SDIN input is latched on the opposite edge of SDCLK used to shift out the data on SDOUT (SDCLK falling edge when INVSCLK = low). Therefore, the MSB of the upstream converter follows the LSB of the downstream converter on the next SDCLK cycle. In this mode, the 40 MHz SDCLK rate cannot be used because the SDIN-to-SDCLK setup time, t_{33}, is less than the minimum time specified. (SDCLK-to-SDOUT delay, t_{32}, is the same for all converters when simultaneously sampled). For proper operation, the SDCLK edge for latching SDIN (or ½ period of SDCLK) needs to be

$$t_{1/2SDCLK} = t_{32} + t_{33}$$

or the maximum SDCLK frequency needs to be

$$f_{SDCLK} = \frac{1}{2(t_{32} + t_{33})}$$

If not using the daisy-chain feature, the SDIN input should always be tied either high or low.

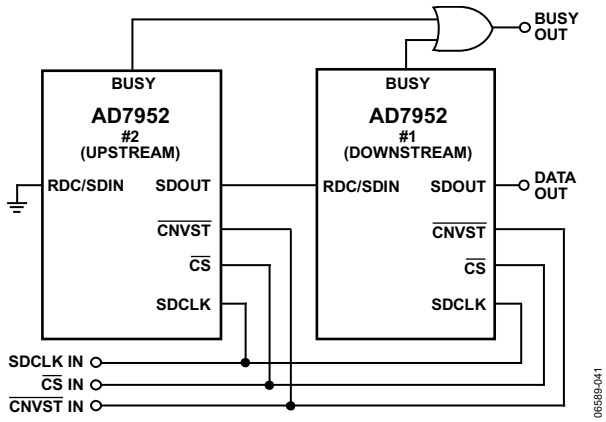


Figure 42. Two AD7952 Devices in a Daisy-Chain Configuration

External Clock Data Read During Previous Conversion

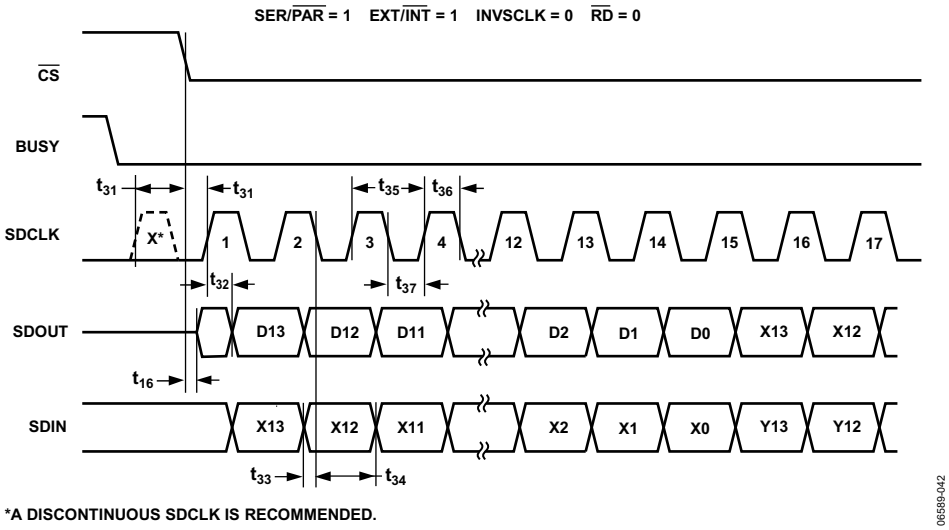
Figure 44 shows the detailed timing diagrams for this method. During a conversion, while both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 14 clock pulses, and depending on the SDCLK frequency, can be valid on both the falling and rising edges of the clock. The 14 bits have to be read before the current conversion is completed; otherwise, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading.

To reduce performance degradation due to digital activity, a fast discontinuous clock of at least 40 MHz is recommended to ensure that all the bits are read during the first half of the SAR conversion phase.

The daisy-chain feature should not be used in this mode because digital activity occurs during the second half of the SAR conversion phase, likely resulting in performance degradation.

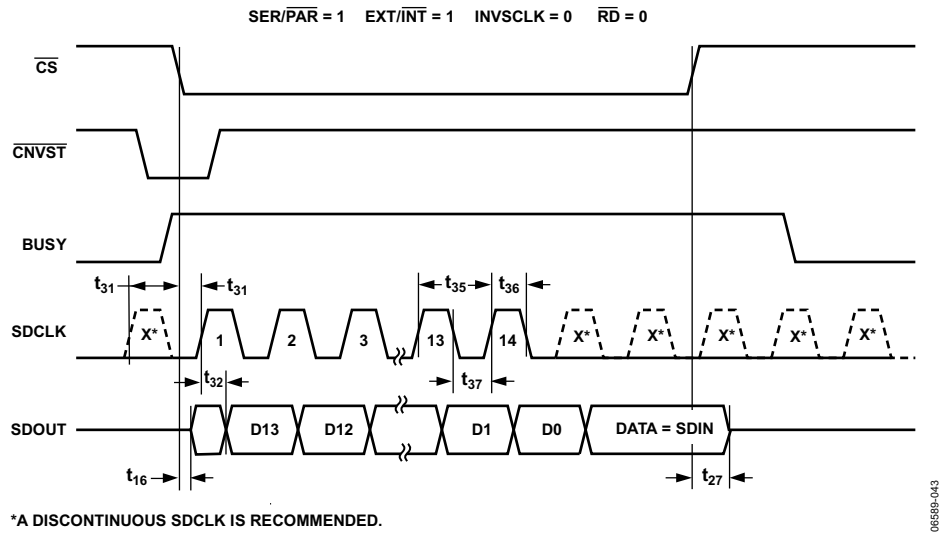
External Clock Data Read After/During Conversion

It is also possible to begin to read data after conversion and continue to read the last bits after a new conversion is initiated. This method allows the full throughput and the use of a slower SDCLK frequency. Again, it is recommended to use a discontinuous SDCLK whenever possible to minimize potential incorrect bit decisions. For the different modes, the use of a slower SDCLK, such as 20 MHz in warp mode, 15 MHz in normal mode, and 13 MHz in impulse mode can be used.



*A DISCONTINUOUS SDCLK IS RECOMMENDED.

Figure 43. Slave Serial Data Timing for Reading (Read After Convert)



*A DISCONTINUOUS SDCLK IS RECOMMENDED.

Figure 44. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

HARDWARE CONFIGURATION

The AD7952 can be configured at any time with the dedicated hardware pins WARP, IMPULSE, BIPOLAR, TEN, OB/$\overline{2C}$, and PD for parallel mode (SER/$\overline{PAR}$ = low) or serial hardware mode (SER/ $\overline{PAR}$ = high, HW/$\overline{SW}$ = high). Programming the AD7952 for mode selection and input range configuration can be done before or during conversion. Like the RESET input, the ADC requires at least one acquisition time to settle, as shown in Figure 45. See Table 6 for pin descriptions. Note that these inputs are high impedance when using the software configuration mode.

SOFTWARE CONFIGURATION

The pins multiplexed on D[13:10] used for software configuration are: HW/$\overline{SW}$, SCIN, SCCLK, and $\overline{SCCS}$. The AD7952 is programmed using the dedicated write-only serial configurable port (SCP) for conversion mode, input range selection, output coding, and power-down using the serial configuration register. See Table 10 for details of each bit in the configuration register. The SCP can only be used in serial software mode selected with SER/$\overline{PAR}$ = high and HW/$\overline{SW}$ = low because the port is multiplexed on the parallel interface.

The SCP is accessed by asserting the port's chip select, $\overline{SCCS}$, and then writing SCIN synchronized with SCCLK, which (like SDCLK) is edge sensitive depending on the state of INVSCLK. See Figure 46 for timing details. SCIN is clocked into the configuration register MSB first. The configuration register is an internal shift register that begins with Bit 8, the START bit. The 9th SPPCLK edge updates the register and allows the new settings to be used. As indicated in the timing diagram, at least one acquisition time is required from the 9th SCCLK edge. Bits [1:0] are reserved bits and are not written to while the SCP is being updated.

The SCP can be written to at any time, up to 40 MHz, and it is recommended to write to while the AD7952 is not busy converting, as detailed in Figure 46. In this mode, the full 1 MSPS is not attainable because the time required for SCP access is (t_{31} + 9 × 1/SCCLK + t_8) minimum. If the full throughput is required, the SCP can be written to during conversion; however, it is not recommended to write to the SCP during the last 450 ns of conversion (BUSY = high), or performance degradation can result. In addition, the SCP can be accessed in both serial master and serial slave read during and read after convert modes.

Note that at power-up, the configuration register is undefined. The RESET input clears the configuration register (sets all bits to 0), thus placing the configuration to 0 V to 5 V input, normal mode, and twos complemented output.

Table 10. Configuration Register Description

Bit	Name	Description		
8	START	START bit. With the SCP enabled ($\overline{SCCS}$ = low), when START is high, the first rising edge of SCCLK (INVSCLK = low) begins to load the register with the new configuration.		
7	BIPOLAR	Input Range Select. Used in conjunction with Bit 6, TEN, per the following.		
		Input Range (V)	**BIPOLAR**	**TEN**
		0 to 5	Low	Low
		0 to 10	Low	High
		±5	High	Low
		±10	High	High
6	TEN	Input Range Select. See Bit 7, BIPOLAR.		
5	PD	Power Down. PD = low, normal operation. PD = high, power down the ADC. The SCP is accessible while in power-down. To power-up the ADC, write PD = low on the next configuration setting.		
4	IMPULSE	Mode Select. Used in conjunction with Bit 3, WARP, per the following.		
		Mode	**WARP**	**IMPULSE**
		Normal	Low	Low
		Impulse	Low	High
		Warp	High	Low
		Normal	High	High
3	WARP	Mode Select. See Bit 4, IMPULSE.		
2	OB/$\overline{2C}$	Output Coding. OB/$\overline{2C}$ = low, use twos complement output. OB/$\overline{2C}$ = high, use straight binary output.		
1	RSV	Reserved.		
0	RSV	Reserved.		

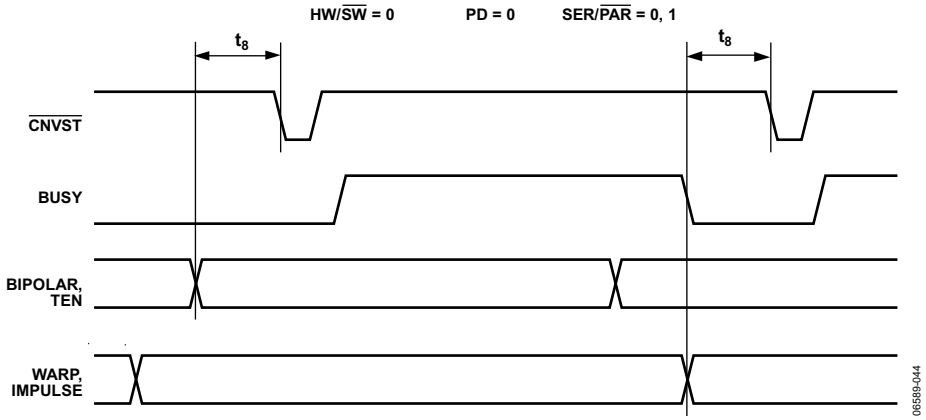


Figure 45. Hardware Configuration Timing

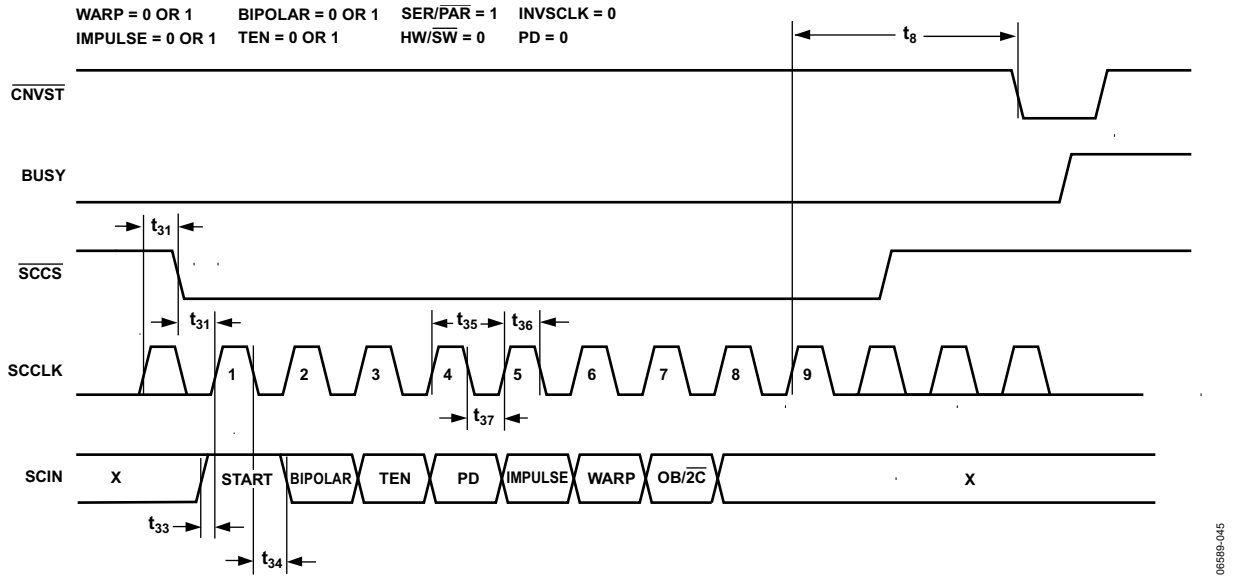


Figure 46. Serial Configuration Port Timing

MICROPROCESSOR INTERFACING

The AD7952 is ideally suited for traditional dc measurement applications supporting a microprocessor and ac signal processing applications interfacing to a digital signal processor. The AD7952 is designed to interface with a parallel 8-bit or 14-bit wide interface, or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7952 to prevent digital noise from coupling into the ADC.

SPI Interface

The AD7952 is compatible with SPI and QSPI digital hosts and DSPs, such as Blackfin® ADSP-BF53x and ADSP-218x/ADSP-219x. Figure 47 shows an interface diagram between the AD7952 and the SPI-equipped ADSP-219x. To accommodate the slower speed of the DSP, the AD7952 acts as a slave device, and data must be read after conversion. This mode also allows the daisy-chain feature. The convert command could be initiated in response to an internal timer interrupt.

The reading process can be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the DSP. The serial peripheral interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, clock polarity bit (CPOL) = 0, clock phase bit (CPHA) = 1, and SPI interrupt enable (TIMOD) = 0 by writing to the SPI control register (SPICLTx).

It should be noted that to meet all timing requirements, the SPI clock should be limited to 17 Mbps, allowing it to read an ADC result in less than 1 µs. When a higher sampling rate is desired, use one of the parallel interface modes.

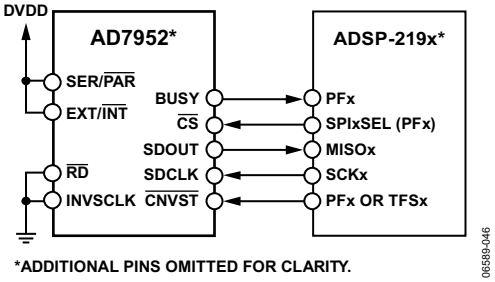


Figure 47. Interfacing the AD7952 to SPI Interface

APPLICATION INFORMATION

LAYOUT GUIDELINES

While the AD7952 has very good immunity to noise on the power supplies, exercise care with the grounding layout. To facilitate the use of ground planes that can be easily separated, design the printed circuit board that houses the AD7952 so that the analog and digital sections are separated and confined to certain areas of the board. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7952, or as close as possible to the AD7952. If the AD7952 is in a system where multiple devices require analog-to-digital ground connections, the connections should still be made at one point only, a star ground point, established as close as possible to the AD7952.

To prevent coupling noise onto the die, to avoid radiating noise, and to reduce feedthrough:

- Do not run digital lines under the device.
- Do run the analog ground plane under the AD7952.
- Shield fast switching signals, like $\overline{\text{CNVST}}$ or clocks, with digital ground to avoid radiating noise to other sections of the board, and never run them near analog signal paths.
- Avoid crossover of digital and analog signals.
- Run traces on different but close layers of the board, at right angles to each other, to reduce the effect of feedthrough through the board.

The power supply lines to the AD7952 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the impedance of the supplies presented to the AD7952, and to reduce the magnitude of the supply spikes. Decoupled ceramic capacitors, typically 100 nF, should be placed on each of the power supplies pins, AVDD, DVDD, OVDD, VCC, and VEE. The capacitors should be placed close to, and ideally right up against, these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7952 can either be a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, and no separate supply is available, it is recommended to connect the DVDD digital supply to the analog supply AVDD through an RC filter, and to connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. See Figure 27 for an example of this configuration. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

The AD7952 has four different ground pins: REFGND, AGND, DGND, and OGND.

- REFGND senses the reference voltage and, because it carries pulsed currents, should be a low impedance return to the reference.
- AGND is the ground to which most internal ADC analog signals are referenced; it must be connected with the least resistance to the analog ground plane.
- DGND must be tied to the analog or digital ground plane depending on the configuration.
- OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. To minimize parasitic inductances, place the decoupling capacitor close to the ADC and connect it with short, thick traces.

OUTLINE DIMENSIONS

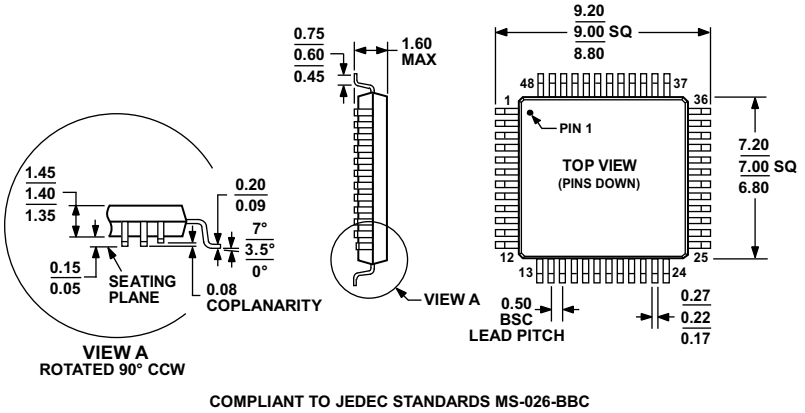


Figure 48. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

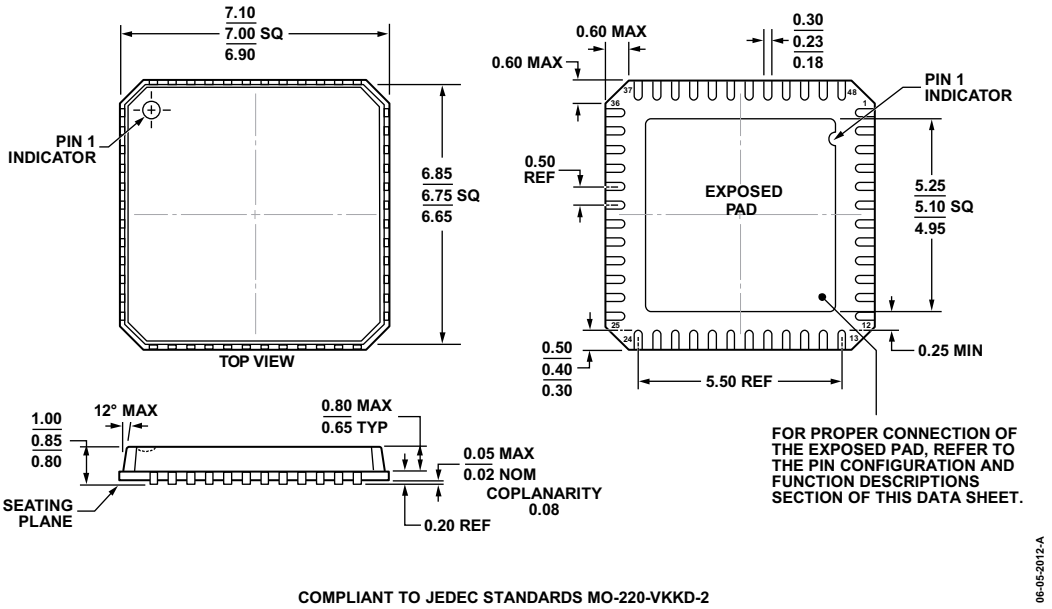


Figure 49. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7952BCPZ	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
AD7952BCPZRL	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
AD7952BSTZ	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD7952BSTZRL	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48

[1] Z = RoHS Compliant Part.

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