Low Noise, High Speed Amplifier for 16-Bit Systems

AD8021

FEATURES

Low Noise
- 2.1 nV/√Hz Input Voltage Noise
- 2.1 pA/√Hz Input Current Noise

Custom Compensation
- Constant Bandwidth from G = –1 to G = –10

High Speed
- 200 MHz (G = –1)
- 190 MHz (G = –10)

Low Power
- 34 mW or 6.7 mA Typ for 5 V Supply

Output Disable Feature, 1.3 mA

Low Distortion
- –93 dB Second Harmonic, f_C = 1 MHz
- –108 dB Third Harmonic, f_C = 1 MHz

DC Precision
- 1 mV Max Input Offset Voltage
- 0.5 μV/°C Input Offset Voltage Drift

Wide Supply Range, 5 V to 24 V

Low Price

Small Packaging
- Available in SOIC-8 and MSOP-8

APPLICATIONS

ADC Preamp and Driver

Instrumentation Preamp
- Active Filters

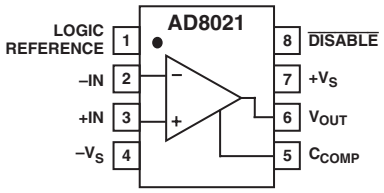
Portable Instrumentation

Line Receivers
- Precision Instruments
- Ultrasound Signal Processing

High Gain Circuits

CONNECTION DIAGRAM

SOIC-8 (R-8)
MSOP-8 (RM-8)



PRODUCT DESCRIPTION

The AD8021 is a very high performance, high speed voltage feedback amplifier that can be used in 16-bit resolution systems. It is designed to have low voltage and current noise (2.1 nV/√Hz typ and 2.1 pA/√Hz typ) while operating at the lowest quiescent supply current (7 mA @ ±5 V) among today's high speed, low noise op amps. The AD8021 operates over a wide range of supply voltages from ±2.5 V to ±12 V, as well as from single 5 V supplies, making it ideal for high speed, low power instruments. An output disable pin allows further reduction of the quiescent supply current to 1.3 mA.

The AD8021 allows the user to choose the gain bandwidth product that best suits the application. With a single capacitor, the user can compensate the AD8021 for the desired gain with little trade-off in bandwidth. The AD8021 is a very well behaved amplifier that settles to 0.01% in 23 ns for a 1 V step. It has a fast overload recovery of 50 ns.

The AD8021 is stable over temperature with low input offset voltage drift and input bias current drift, 0.5 μV/°C and 10 nA/°C, respectively. The AD8021 is also capable of driving a 75 Ω line with ±3 V video signals.

The AD8021 is not only technically superior, but also priced considerably less than comparable amps drawing much higher quiescent current. The AD8021 is a high speed, general-purpose amplifier, ideal for a wide variety of gain configurations, and can be used throughout a signal processing chain and in control loops.

The AD8021 is available in both standard 8-lead SOIC and MSOP packages in the industrial temperature range of –40°C to +85°C.

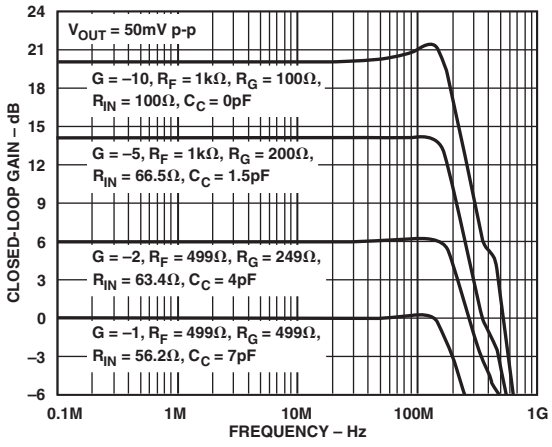


Figure 1. Small Signal Frequency Response

REV. D

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Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD8021–SPECIFICATIONS

$V_S = \pm 5$ V (@ T_A = 25°C, V_S = 5 V, R_L = 1 kΩ, Gain = +2, unless otherwise noted.)

Parameter	Conditions	AD8021AR/AD8021ARM Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = +1, C_C = 10 pF, V_O = 0.05 V p-p	355	490		MHz
	G = +2, C_C = 7 pF, V_O = 0.05 V p-p	160	205		MHz
	G = +5, C_C = 2 pF, V_O = 0.05 V p-p	150	185		MHz
	G = +10, C_C = 0 pF, V_O = 0.05 V p-p	110	150		MHz
Slew Rate, 1 V Step	G = +1, C_C = 10 pF	95	120		V/µs
	G = +2, C_C = 7 pF	120	150		V/µs
	G = +5, C_C = 2 pF	250	300		V/µs
	G = +10, C_C = 0 pF	380	420		V/µs
Settling Time to 0.01%	V_O = 1 V Step, R_L = 500 Ω		23		ns
Overload Recovery (50%)	±2.5 V Input Step, G = +2		50		ns
DISTORTION/NOISE PERFORMANCE					
f = 1 MHz					
HD2	V_O = 2 V p-p		–93		dBc
HD3	V_O = 2 V p-p		–108		dBc
f = 5 MHz					
HD2	V_O = 2 V p-p		–70		dBc
HD3	V_O = 2 V p-p		–80		dBc
Input Voltage Noise	f = 50 kHz		2.1	2.6	nV/√Hz
Input Current Noise	f = 50 kHz		2.1		pA/√Hz
Differential Gain Error	NTSC, R_L = 150 Ω		0.03		%
Differential Phase Error	NTSC, R_L = 150 Ω		0.04		Degrees
DC PERFORMANCE					
Input Offset Voltage			0.4	1.0	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		0.5		µV/°C
Input Bias Current	+Input or –Input		7.5	10.5	µA
Input Bias Current Drift			10		nA/°C
Input Offset Current			0.1	0.5	±µA
Open-Loop Gain		82	86		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Common-Mode Input Capacitance			1		pF
Input Common-Mode Voltage Range			–4.1 to +4.6		V
Common-Mode Rejection Ratio	V_{CM} = ±4 V	–86	–98		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		–3.5 to +3.2	–3.8 to +3.4		V
Linear Output Current			60		mA
Short-Circuit Current			75		mA
Capacitive Load Drive for 30% Overshoot	V_O = 50 mV p-p/1 V p-p		15/120		pF
DISABLE CHARACTERISTICS					
Off Isolation	f = 10 MHz		–40		dB
Turn-On Time	V_O = 0 V to 2 V, 50% Logic to 50% Output		45		ns
Turn-Off Time	V_O = 0 V to 2 V, 50% Logic to 50% Output		50		ns
$\overline{\text{DISABLE}}$ Voltage—Off/On	$V_{DISABLE} - V_{LOGIC\ REFERENCE}$		1.75/1.90		V
Enabled Leakage Current	$\underline{\text{Logic Ref}}$ = 0.4 V		70		µA
	$\overline{\text{DISABLE}}$ = 4.0 V		2		µA
Disabled Leakage Current	$\underline{\text{Logic Ref}}$ = 0.4 V		30		µA
	$\overline{\text{DISABLE}}$ = 0.4 V		33		µA
POWER SUPPLY					
Operating Range		±2.25	±5	±12.0	V
Quiescent Current	Output Enabled		7.0	7.7	mA
	Output Disabled		1.3	1.6	mA
+Power Supply Rejection Ratio	V_{CC} = +4 V to +6 V, V_{EE} = –5 V	–86	–95		dB
–Power Supply Rejection Ratio	V_{CC} = +5 V, V_{EE} = –6 V to –4 V	–86	–95		dB

Specifications subject to change without notice.

$V_S = \pm 12$ V (@ T_A = 25°C, R_L = 1 kΩ, Gain = +2, unless otherwise noted.)

Parameter	Conditions	AD8021AR/AD8021ARM Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = +1, C_C = 10 pF, V_O = 0.05 V p-p	520	560		MHz
	G = +2, C_C = 7 pF, V_O = 0.05 V p-p	175	220		MHz
	G = +5, C_C = 2 pF, V_O = 0.05 V p-p	170	200		MHz
	G = +10, C_C = 0 pF, V_O = 0.05 V p-p	125	165		MHz
Slew Rate, 1 V Step	G = +1, C_C = 10 pF	105	130		V/µs
	G = +2, C_C = 7 pF	140	170		V/µs
	G = +5, C_C = 2 pF	265	340		V/µs
	G = +10, C_C = 0 pF	400	460		V/µs
Settling Time to 0.01%	V_O = 1 V Step, R_L = 500 Ω		21		ns
Overload Recovery (50%)	±6 V Input Step, G = +2		90		ns
DISTORTION/NOISE PERFORMANCE					
f = 1 MHz					
HD2	V_O = 2 V p-p		–95		dBc
HD3	V_O = 2 V p-p		–116		dBc
f = 5 MHz					
HD2	V_O = 2 V p-p		–71		dBc
HD3	V_O = 2 V p-p		–83		dBc
Input Voltage Noise	f = 50 kHz		2.1	2.6	$nV/\sqrt{Hz}$
Input Current Noise	f = 50 kHz		2.1		$pA/\sqrt{Hz}$
Differential Gain Error	NTSC, R_L = 150 Ω		0.03		%
Differential Phase Error	NTSC, R_L = 150 Ω		0.04		Degrees
DC PERFORMANCE					
Input Offset Voltage			0.4	1.0	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		0.2		µV/°C
Input Bias Current	+Input or –Input		8	11.3	µA
Input Bias Current Drift			10		nA/°C
Input Offset Current			0.1	0.5	±µA
Open-Loop Gain		84	88		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Common-Mode Input Capacitance			1		pF
Input Common-Mode Voltage Range			–11.1 to +11.6		V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	–86	–96		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		–10.2 to +9.8	–10.6 to +10.2		V
Linear Output Current			70		mA
Short-Circuit Current			115		mA
Capacitive Load Drive for 30% Overshoot	V_O = 50 mV p-p/1 V p-p		15/120		pF
DISABLE CHARACTERISTICS					
Off Isolation	f = 10 MHz		–40		dB
Turn-On Time	V_O = 0 V to 2 V, 50% Logic to 50% Output		45		ns
Turn-Off Time	V_O = 0 V to 2 V, 50% Logic to 50% Output		50		ns
$\overline{\text{DISABLE}}$ Voltage—Off/On	$V_{DISABLE} - V_{LOGIC\ REFERENCE}$		1.80/1.95		V
Enabled Leakage Current	$\overline{\text{Logic Ref}}$ = 0.4 V		70		µA
	$\overline{\text{DISABLE}}$ = 4.0 V		2		µA
Disabled Leakage Current	$\overline{\text{Logic Ref}}$ = 0.4 V		30		µA
	$\overline{\text{DISABLE}}$= 0.4 V		33		µA
POWER SUPPLY					
Operating Range		±2.25	±5	±12.0	V
Quiescent Current	Output Enabled		7.8	8.6	mA
	Output Disabled		1.7	2.0	mA
+Power Supply Rejection Ratio	V_{CC} = +11 V to +13 V, V_{EE} = –12 V	–86	–96		dB
–Power Supply Rejection Ratio	V_{CC} = +12 V, V_{EE} = –13 V to –11 V	–86	–100		dB

Specifications subject to change without notice.

$V_S = 5$ V (@ T_A = 25°C, R_L = 1 kΩ, Gain = +2, unless otherwise noted.)

Parameter	Conditions	AD8021AR/AD8021ARM Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = +1, C_C = 10 pF, V_O = 0.05 V p-p	270	305		MHz
	G = +2, C_C = 7 pF, V_O = 0.05 V p-p	155	190		MHz
	G = +5, C_C = 2 pF, V_O = 0.05 V p-p	135	165		MHz
	G = +10, C_C = 0 pF, V_O = 0.05 V p-p	95	130		MHz
Slew Rate, 1 V Step	G = +1, C_C = 10 pF	80	110		V/µs
	G = +2, C_C = 7 pF	110	140		V/µs
	G = +5, C_C = 2 pF	210	280		V/µs
	G = +10, C_C = 0 pF	290	390		V/µs
Settling Time to 0.01%	V_O = 1 V Step, R_L = 500 Ω		28		ns
Overload Recovery (50%)	0 V to 2.5 V Input Step, G = +2		40		ns
DISTORTION/NOISE PERFORMANCE					
f = 1 MHz					
HD2	V_O = 2 V p-p		–84		dBc
HD3	V_O = 2 V p-p		–91		dBc
f = 5 MHz					
HD2	V_O = 2 V p-p		–68		dBc
HD3	V_O = 2 V p-p		–81		dBc
Input Voltage Noise	f = 50 kHz		2.1	2.6	nV/√Hz
Input Current Noise	f = 50 kHz		2.1		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.4	1.0	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		0.8		µV/°C
Input Bias Current	+Input or –Input		7.5	10.3	µA
Input Bias Current Drift			10		nA/°C
Input Offset Current			0.1	0.5	±µA
Open-Loop Gain		72	76		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Common-Mode Input Capacitance			1		pF
Input Common-Mode Voltage Range			0.9 to 4.6		V
Common-Mode Rejection Ratio	1.5 V to 3.5 V	–84	–98		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		1.25 to 3.38	1.10 to 3.60		V
Linear Output Current			30		mA
Short-Circuit Current			50		mA
Capacitive Load Drive for 30% Overshoot	V_O = 50 mV p-p/1 V p-p		10/120		pF
DISABLE CHARACTERISTICS					
Off Isolation	f = 10 MHz		–40		dB
Turn-On Time	V_O = 0 V to 1 V, 50% Logic to 50% Output		45		ns
Turn-Off Time	V_O = 0 V to 1 V, 50% Logic to 50% Output		50		ns
$\overline{\text{DISABLE}}$ Voltage—Off/On	$V_{DISABLE} - V_{LOGIC\ REFERENCE}$		1.55/1.70		V
Enabled Leakage Current	$\overline{\text{Logic Ref}}$ = 0.4 V		70		µA
	$\overline{\text{DISABLE}}$ = 4.0 V		2		µA
Disabled Leakage Current	$\overline{\text{Logic Ref}}$ = 0.4 V		30		µA
	$\overline{\text{DISABLE}}$ = 0.4 V		33		µA
POWER SUPPLY					
Operating Range		±2.25	±5	±12.0	V
Quiescent Current	Output Enabled		6.7	7.5	mA
	Output Disabled		1.2	1.5	mA
+Power Supply Rejection Ratio	V_{CC} = 4.5 V to 5.5 V, V_{EE} = 0 V	–74	–82		dB
–Power Supply Rejection Ratio	V_{CC} = +5 V, V_{EE} = –0.5 V to +0.5 V	–76	–84		dB

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 26.4 V
Power Dissipation . . . . . Observed Power Derating Curves
Input Voltage (Common-Mode) . . . . . $\pm V_S \pm 1$ V
Differential Input Voltage[2] . . . . . ±0.8 V
Differential Input Current . . . . . ±10 mA
Output Short-Circuit Duration
. . . . . Observed Power Derating Curves
Storage Temperature . . . . . –65°C to +125°C
Operating Temperature Range . . . . . –40°C to +85°C
Lead Temperature Range (Soldering, 10 sec) . . . . . 300°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

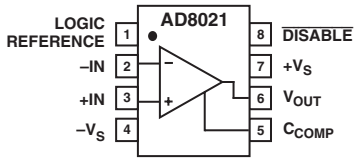
[2] The AD8021 inputs are protected by diodes. Current-limiting resistors are not used in order to preserve the low noise. If a differential input exceeds ±0.8 V, the input current should be limited to ±10 mA.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8021 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8021 is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

PIN CONFIGURATION



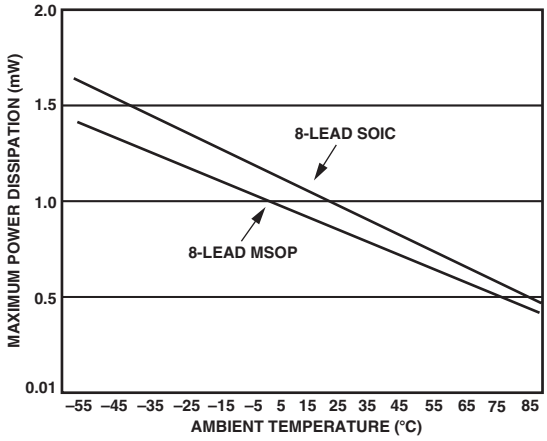


*Figure 2. Maximum Power Dissipation vs. Temperature**

*Specification is for device in free air:
8-Lead SOIC: θ_{JA} = 125°C/W
8-Lead MSOP: θ_{JA} = 145°C/W

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	LOGIC REFERENCE	Reference for Pin 8* Voltage Level. Connect to logic low supply.
2	–IN	Inverting Input
3	+IN	Noninverting Input
4	$-V_S$	Negative Supply Voltage
5	C_{COMP}	Compensation Capacitor. Tie to $-V_S$. (See the Applications section for value.)
6	V_{OUT}	Output
7	$+V_S$	Positive Supply Voltage
8	$\overline{\text{DISABLE}}$	Disable, Active Low*

*When Pin 8 ($\overline{\text{DISABLE}}$) is about 2 V or more higher than Pin 1 (LOGIC REFERENCE), the part is enabled. When Pin 8 is brought down to within about 1.5 V of Pin 1, the part is disabled. (See the Specification tables for exact disable and enable voltage levels.) If the disable feature is not going to be used, Pin 8 can be tied to $+V_S$ or a logic high source, and Pin 1 can be tied to ground or logic low. Alternatively, if Pin 1 and Pin 8 are not connected, the part will be in an enabled state.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline	Branding
AD8021AR	–40°C to +85°C	8-Lead SOIC	R-8	
AD8021AR-REEL	–40°C to +85°C	8-Lead SOIC	R-8	
AD8021AR-REEL7	–40°C to +85°C	8-Lead SOIC	R-8	
AD8021ARM	–40°C to +85°C	8-Lead MSOP	RM-8	HNA
AD8021ARM-REEL	–40°C to +85°C	8-Lead MSOP	RM-8	HNA
AD8021ARM-REEL7	–40°C to +85°C	8-Lead MSOP	RM-8	HNA
AD8021ARZ*	–40°C to +85°C	8-Lead SOIC	R-8	
AD8021ARZ-REEL*	–40°C to +85°C	8-Lead SOIC	R-8	
AD8021ARZ-REEL7*	–40°C to +85°C	8-Lead SOIC	R-8	

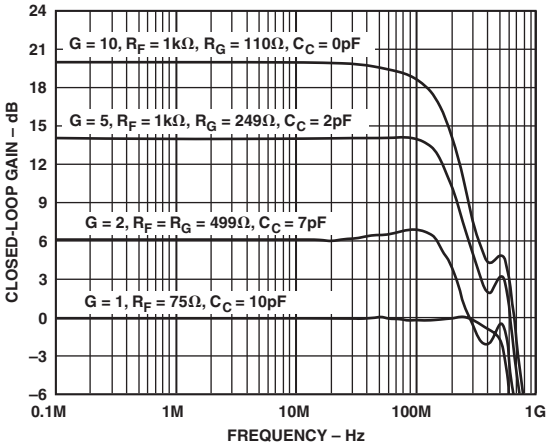
*Z = Lead Free

CAUTION

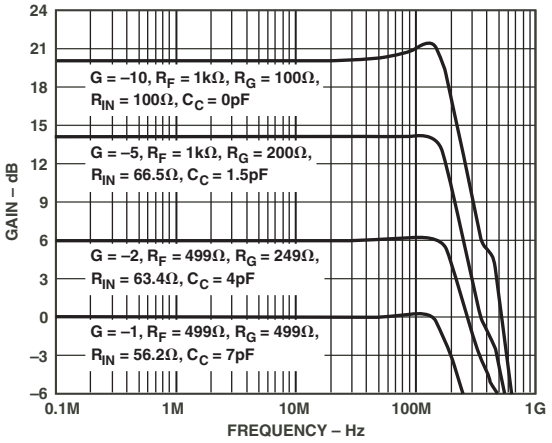
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8021 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD8021–Typical Performance Characteristics

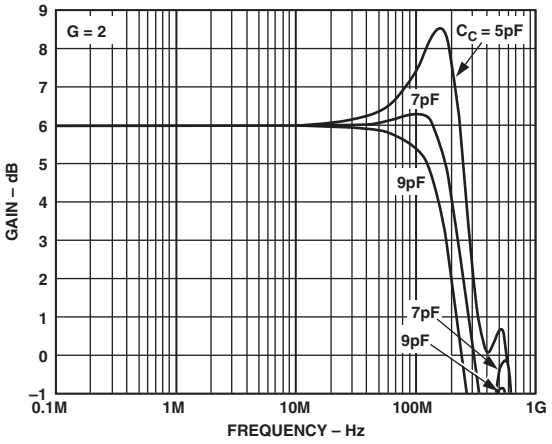
(T_A = 25°C, V_S = ±5 V, R_L = 1 kΩ, G = +2, R_F = R_G = 499 Ω, R_S = 49.9 Ω, R_O = 976 Ω, R_D = 53.6 Ω, C_C = 7 pF, C_L = 0, C_F = 0, V_{OUT} = 2 V p-p, Freq = 1 MHz, unless otherwise noted.)



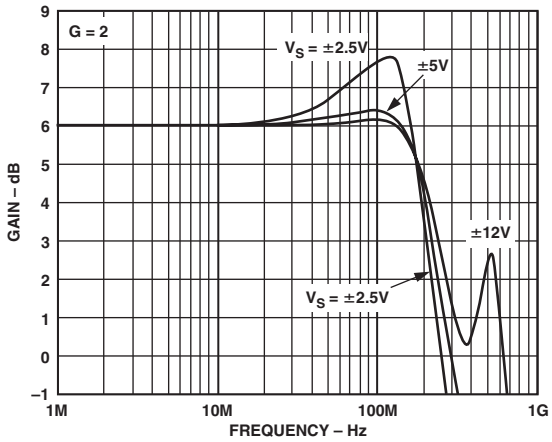
TPC 1. Small Signal Frequency Response vs. Frequency and Gain, V_{OUT} = 50 mV p-p, Noninverting. See Test Circuit 1.



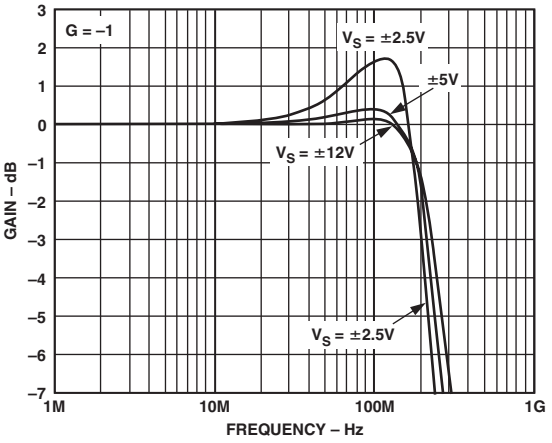
TPC 2. Small Signal Frequency Response vs. Frequency and Gain, V_{OUT} = 50 mV p-p, Inverting. See Test Circuit 1.



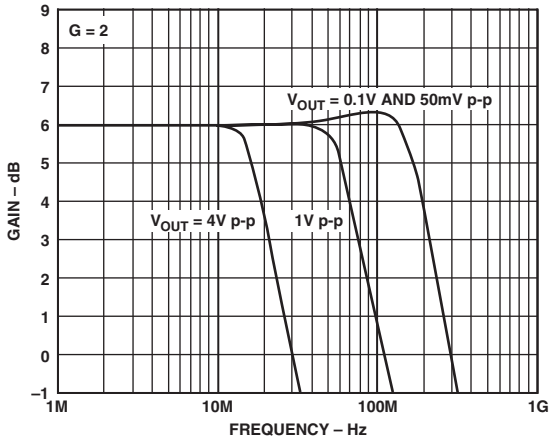
TPC 3. Small Signal Frequency Response vs. Frequency and Compensation Capacitor, V_{OUT} = 50 mV p-p. See Test Circuit 1.



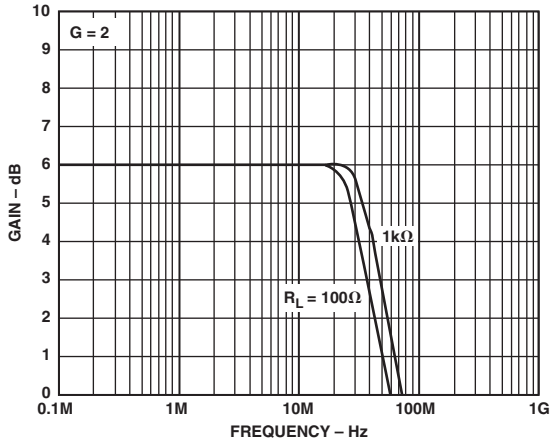
TPC 4. Small Signal Frequency Response vs. Frequency and Supply, V_{OUT} = 50 mV p-p, Noninverting. See Test Circuit 1.



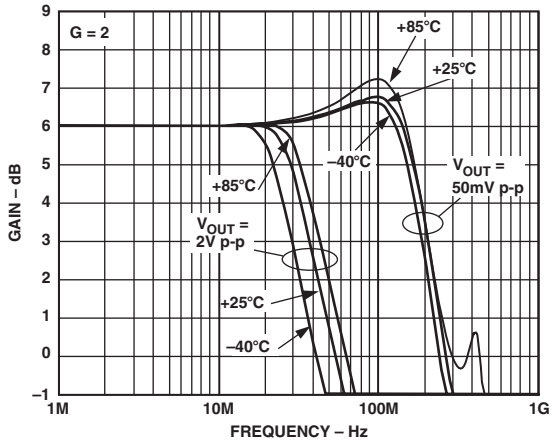
TPC 5. Small Signal Frequency Response vs. Frequency and Supply, V_{OUT} = 50 mV p-p, Inverting. See Test Circuit 3.



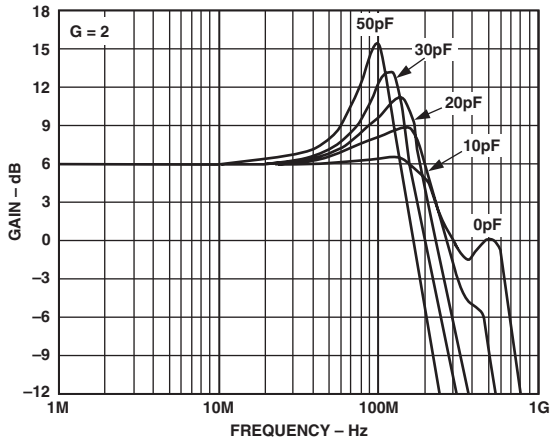
TPC 6. Frequency Response vs. Frequency and V_{OUT}, Noninverting. See Test Circuit 1.



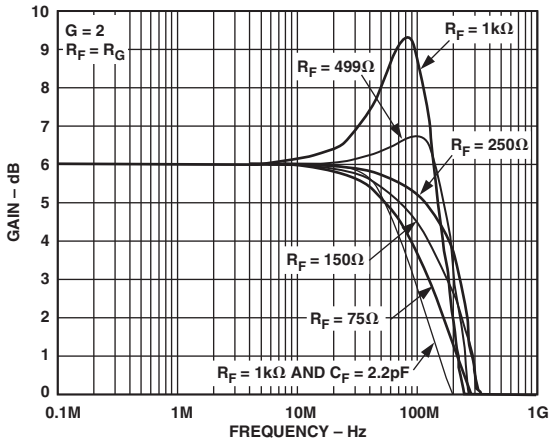
TPC 7. Large Signal Frequency Response vs. Frequency and Load, Noninverting. See Test Circuit 2.



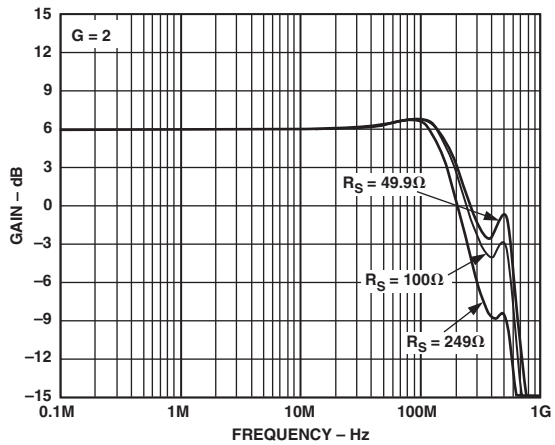
TPC 8. Frequency Response vs. Frequency, Temperature and V_{OUT}, Noninverting. See Test Circuit 1.



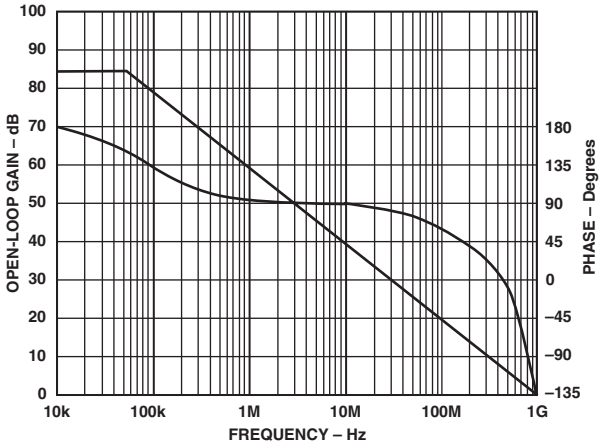
TPC 9. Small Signal Frequency Response vs. Frequency and Capacitive Load, Noninverting, V_{OUT} = 50 mV p-p. See Test Circuit 2 and Figure 16.



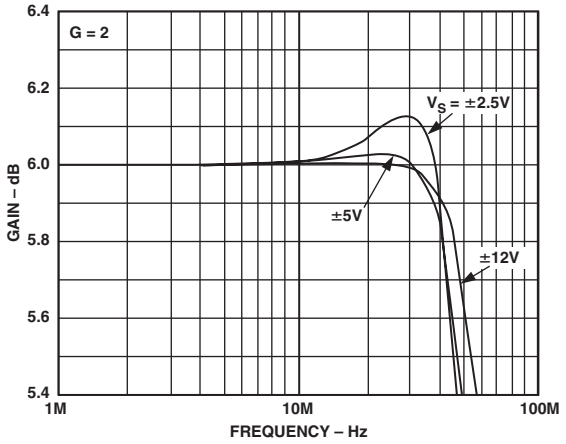
TPC 10. Small Signal Frequency Response vs. Frequency and R_F, Noninverting, V_{OUT} = 50 mV p-p. See Test Circuit 1.



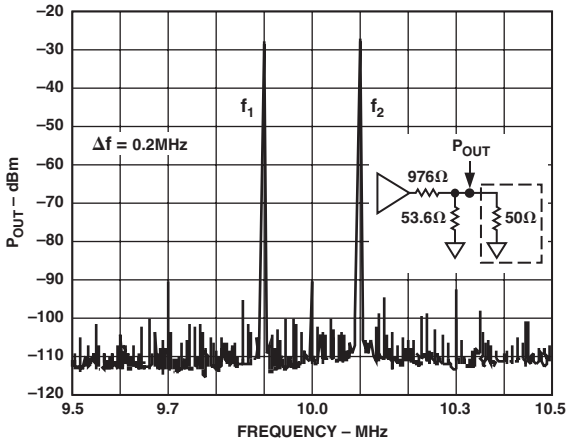
TPC 11. Small Signal Frequency Response vs. Frequency and R_S, Noninverting, V_{OUT} = 50 mV p-p. See Test Circuit 1.



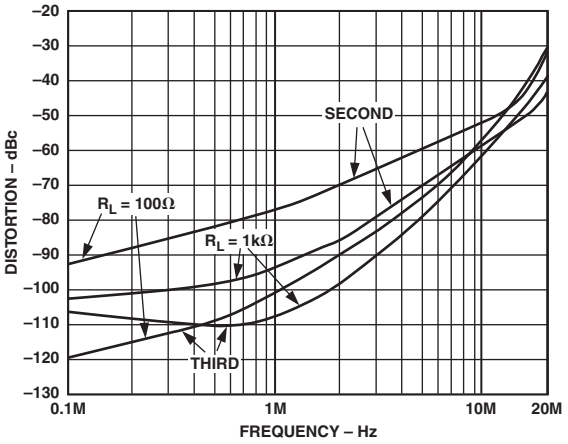
TPC 12. Open-Loop Gain and Phase vs. Frequency, R_G =100 Ω, R_F = 1 kΩ, R_O = 976 Ω, R_D = 53.6 Ω, C_C = 0 pF. See Test Circuit 3.



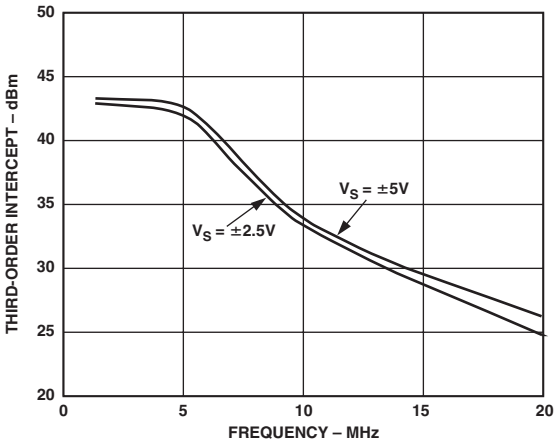
TPC 13. 0.1 dB Flatness vs. Frequency and Supply, V_{OUT} = 1 V p-p, R_L = 150 Ω, Noninverting. See Test Circuit 2.



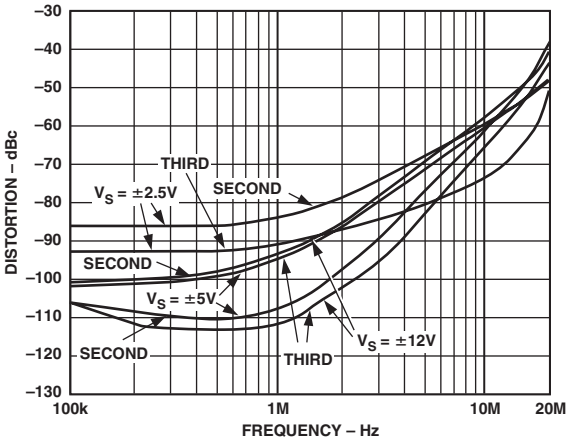
TPC 16. Intermodulation Distortion vs. Frequency



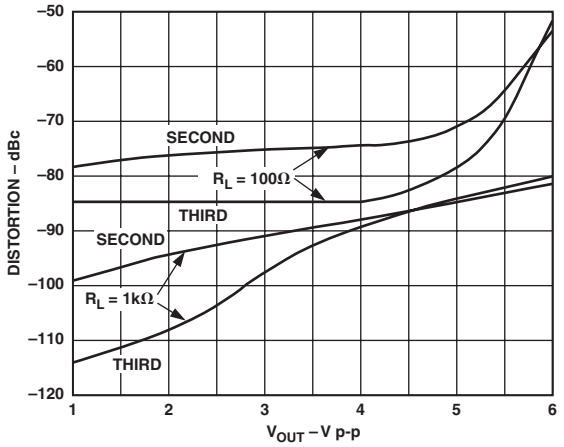
TPC 14. Second and Third Harmonic Distortion vs. Frequency and R_L



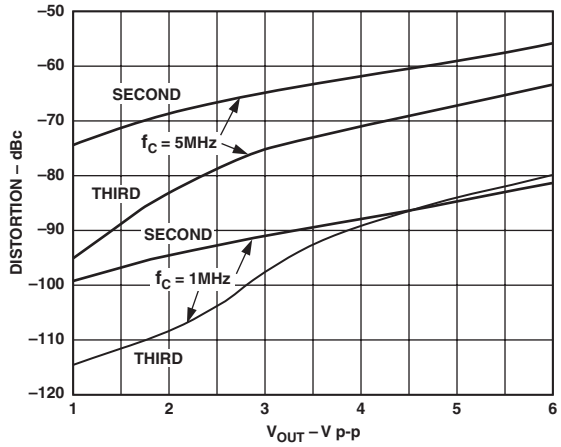
TPC 17. Third-Order Intercept vs. Frequency and Supply Voltage



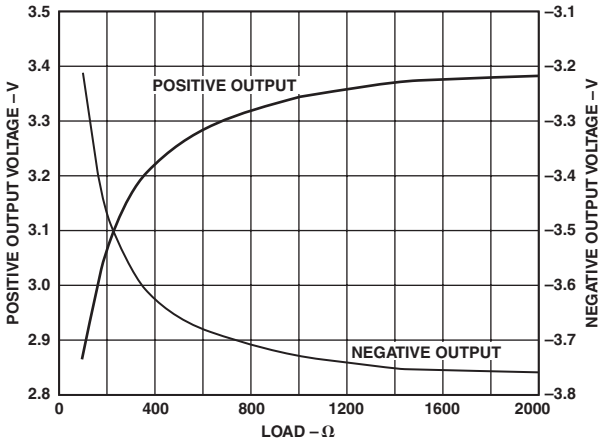
TPC 15. Second and Third Harmonic Distortion vs. Frequency and V_S



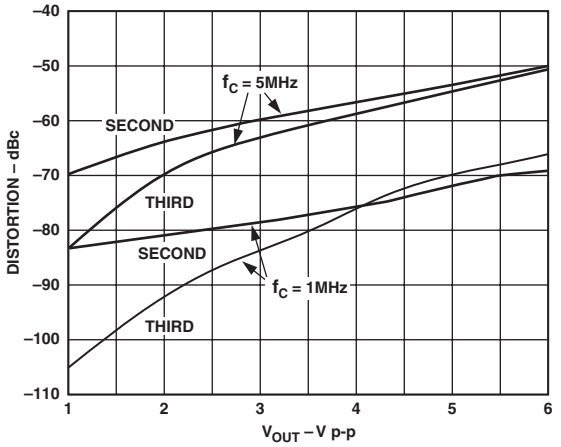
TPC 18. Second and Third Harmonic Distortion vs. V_{OUT} and R_L



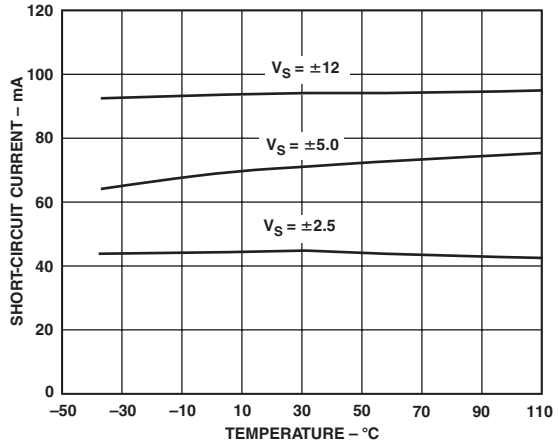
TPC 19. Second and Third Harmonic Distortion vs. V_{OUT} and Fundamental Frequency (f_C), G = +2



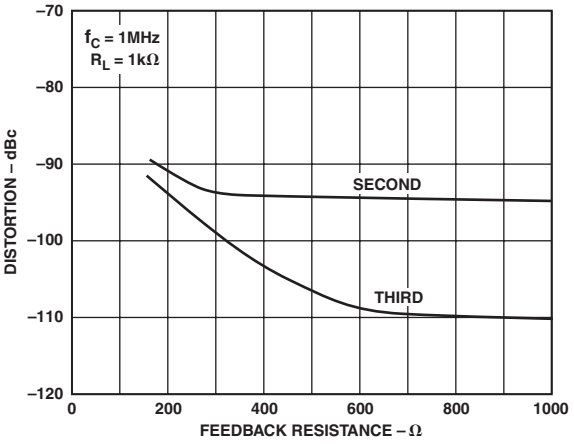
TPC 22. DC Output Voltage vs. Load. See Test Circuit 1.



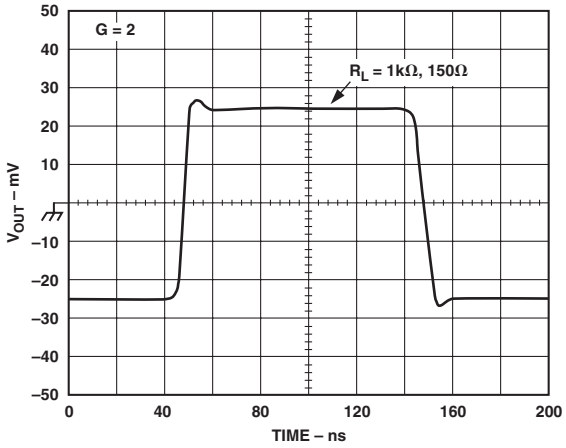
TPC 20. Second and Third Harmonic Distortion vs. V_{OUT} and Fundamental Frequency (f_C), G = +10



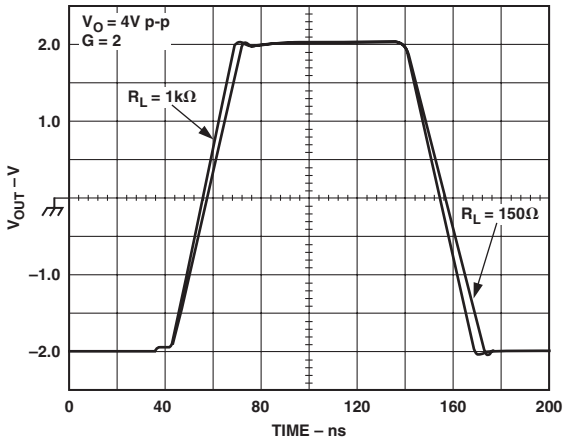
TPC 23. Short-Circuit Current to Ground vs. Temperature



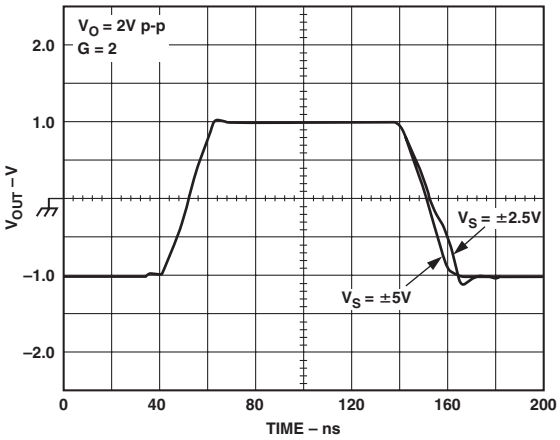
TPC 21. Second and Third Harmonic Distortion vs. Feedback Resistor (R_F)



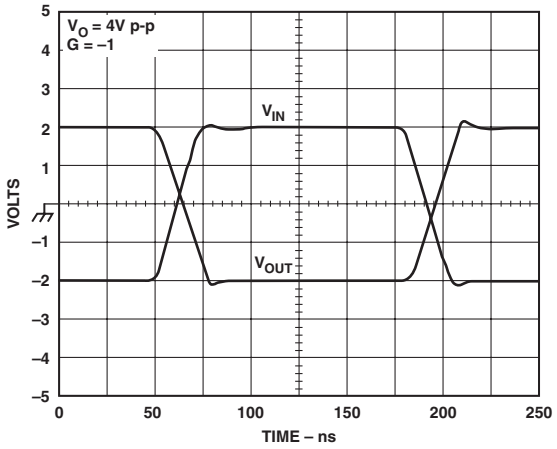
TPC 24. Small Signal Transient Response vs. R_L, V_O = 50 mV p-p. See Test Circuit 2, Noninverting.



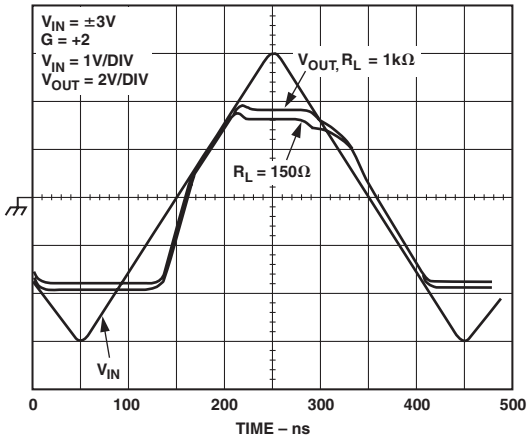
TPC 25. Large Signal Transient Response vs. R_L. See Test Circuit 2, Noninverting.



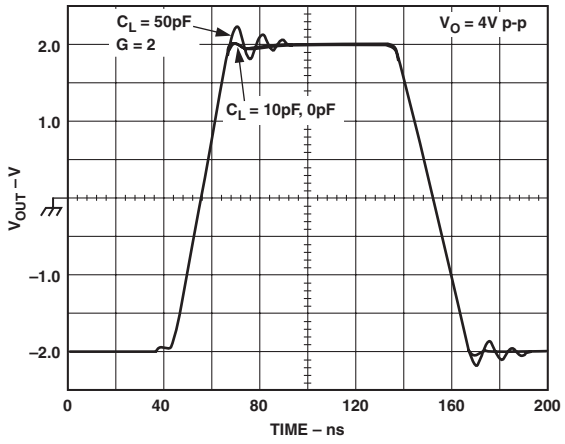
TPC 28. Large Signal Transient Response vs. V_S. See Test Circuit 1.



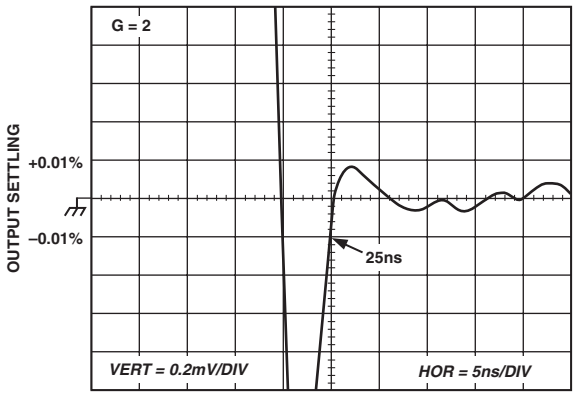
TPC 26. Large Signal Transient Response. See Test Circuit 3, Inverting.



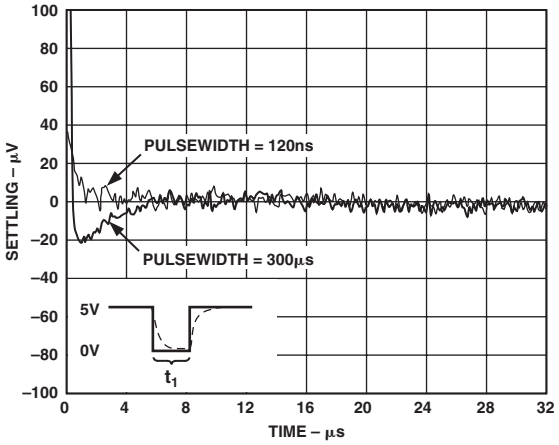
TPC 29. Overdrive Recovery vs. R_L. See Test Circuit 2.



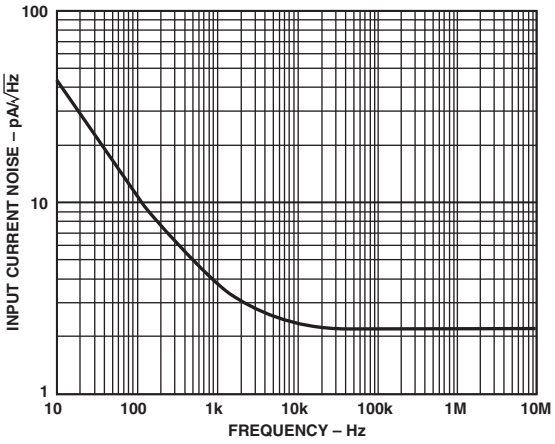
TPC 27. Large Signal Transient Response vs. C_L. See Test Circuit 1.



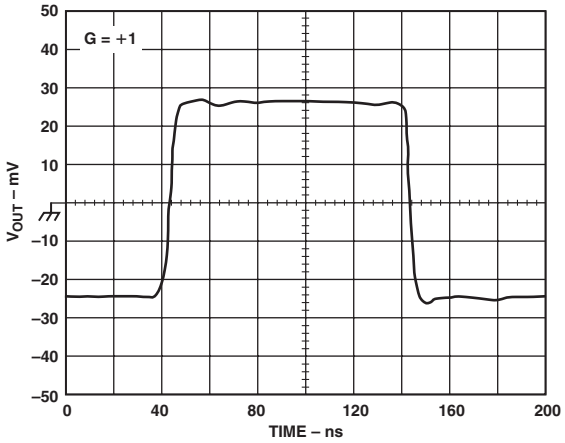
TPC 30. 0.01% Settling Time, 2 V Step



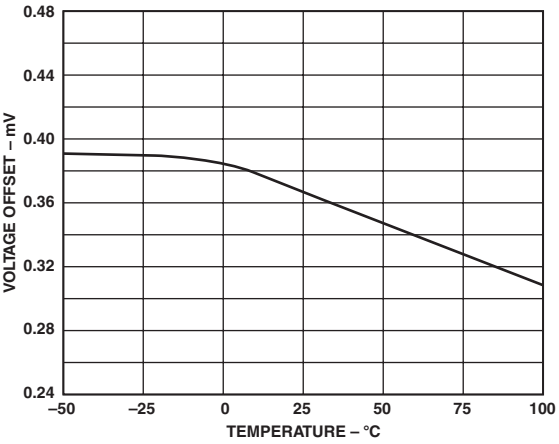
TPC 31. Long-Term Settling, 0 V to 5 V, $V_S = \pm 12$ V, G = +13



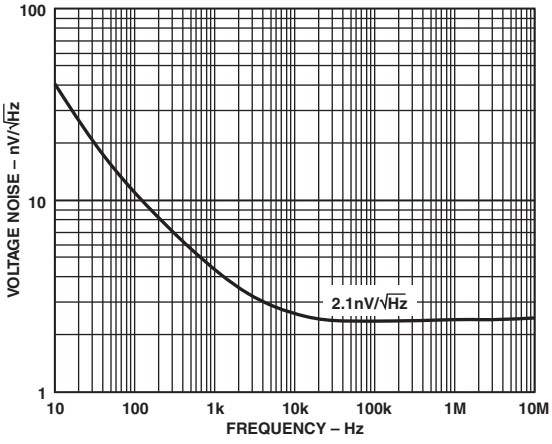
TPC 34. Input Current Noise vs. Frequency



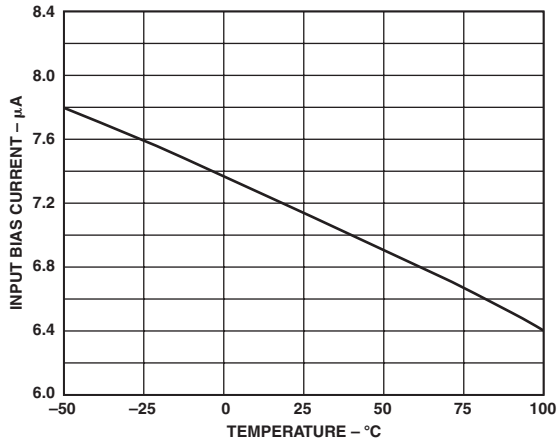
TPC 32. Small Signal Transient Response, V_O = 50 mV p-p. G = +1. See Test Circuit 1.



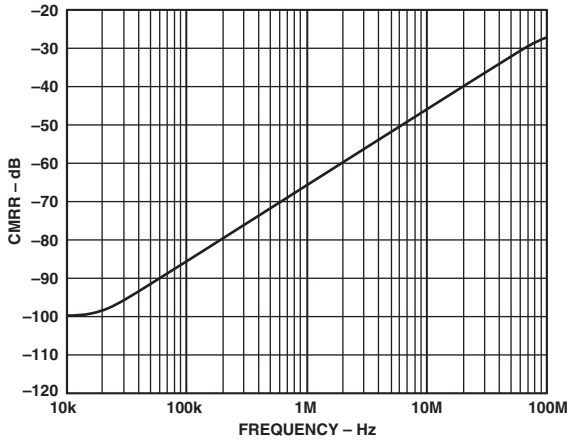
TPC 35. V_{OS} vs. Temperature



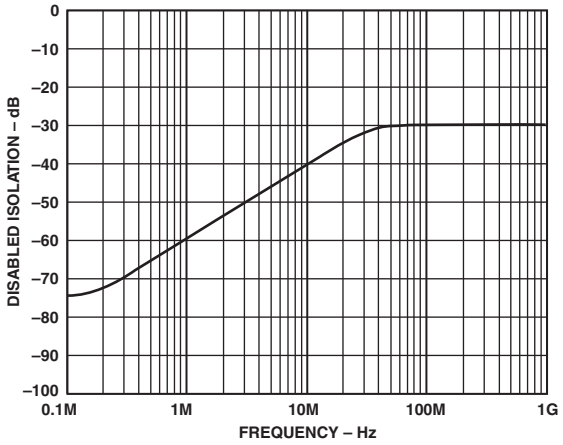
TPC 33. Input Voltage Noise vs. Frequency



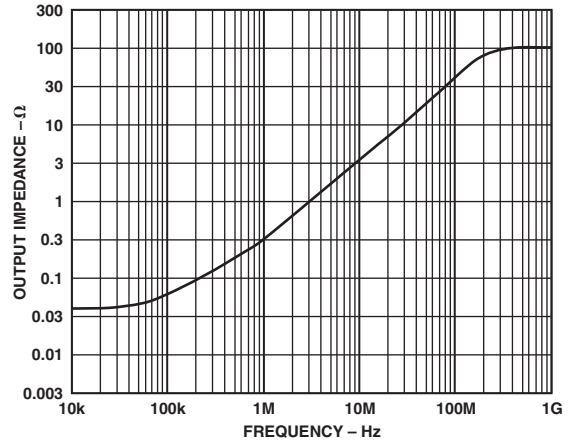
TPC 36. Input Bias Current vs. Temperature



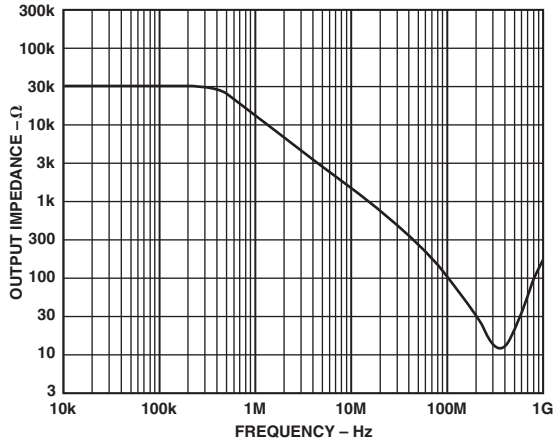
TPC 37. CMRR vs. Frequency. See Test Circuit 4.



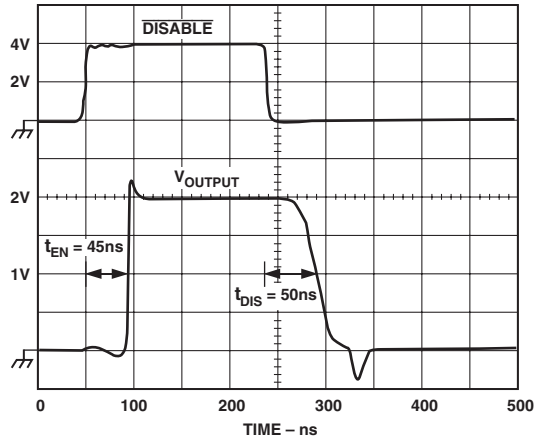
TPC 40. Input to Output Isolation, Chip Disabled. See Test Circuit 7.



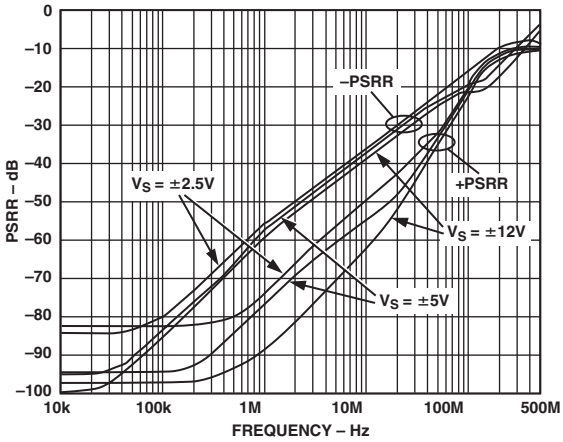
TPC 38. Output Impedance vs. Frequency, Chip Enabled. See Test Circuit 5.



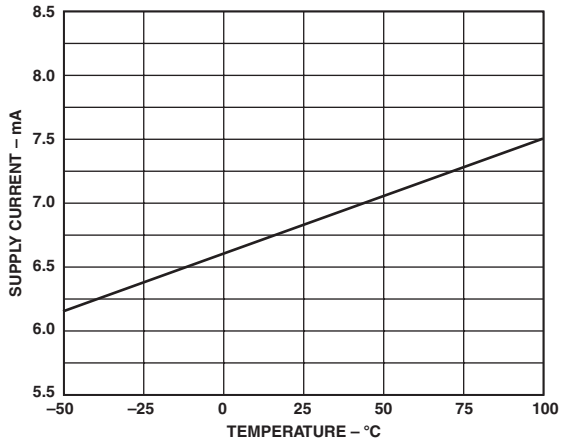
TPC 41. Output Impedance vs. Frequency, Chip Disabled. See Test Circuit 8.



TPC 39. Enable (t_{EN})/Disable (t_{DIS}) Time vs. V_{OUT}. See Test Circuit 6.

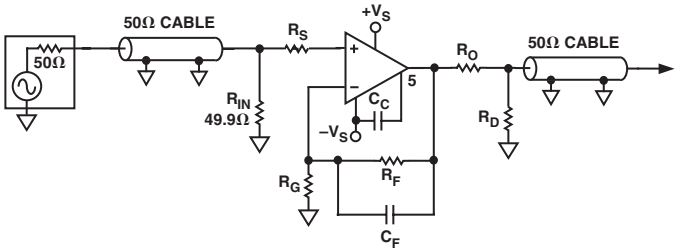


TPC 42. PSRR vs. Frequency and Supply Voltage. See Test Circuits 9 and 10.

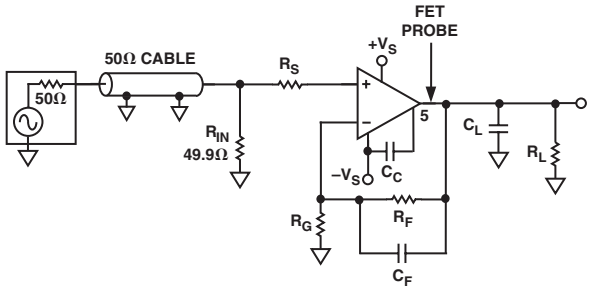


TPC 43. Quiescent Supply Current vs. Temperature

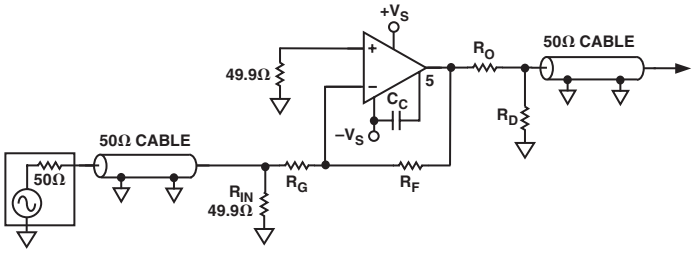
Test Circuits



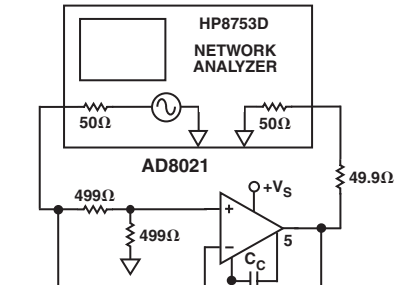
Test Circuit 1. Noninverting Gain



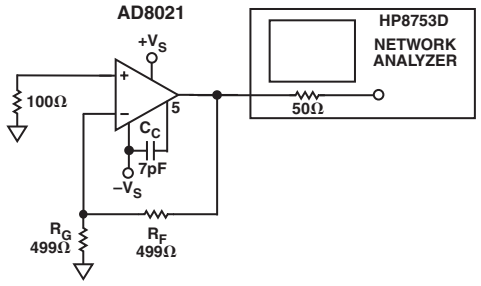
Test Circuit 2. Noninverting Gain with FET Probe



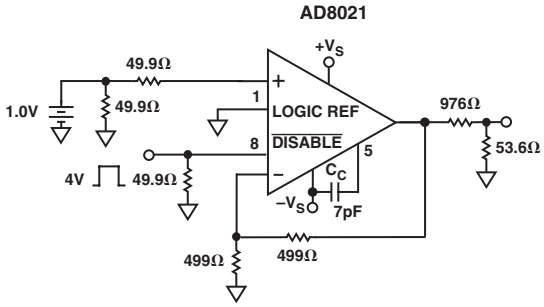
Test Circuit 3. Inverting Gain



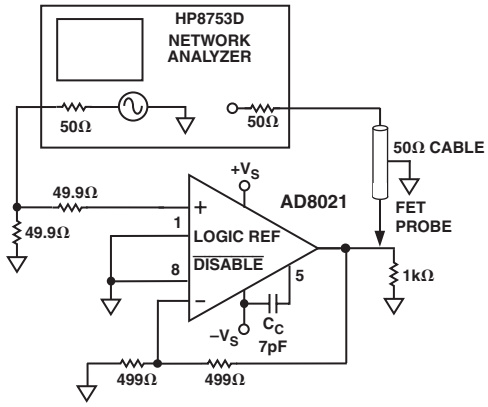
Test Circuit 4. CMRR



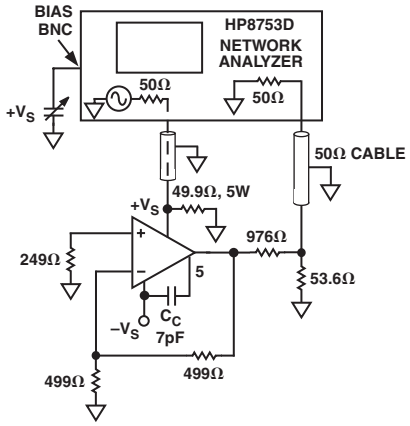
Test Circuit 5. Output Impedance, Chip Enabled



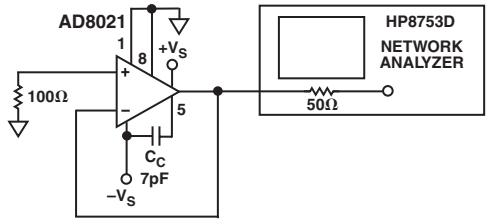
Test Circuit 6. Enable/Disable



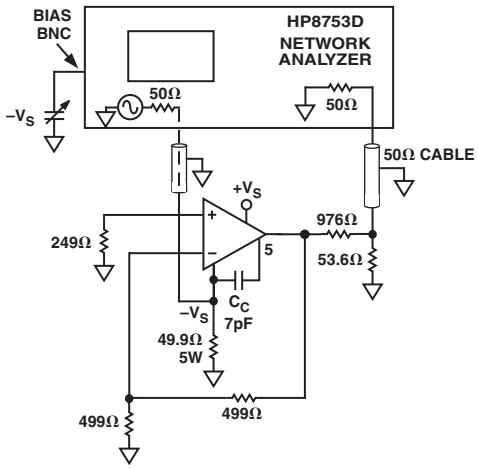
Test Circuit 7. Input to Output Isolation, Chip Disabled



Test Circuit 9. Positive PSRR



Test Circuit 8. Output Impedance, Chip Disabled



Test Circuit 10. Negative PSRR

APPLICATIONS

The typical voltage feedback op amp is frequency stabilized with a fixed internal capacitor, $C_{INTERNAL}$, using dominant pole compensation. To a first-order approximation, voltage feedback op amps have a fixed gain bandwidth product. For example, if its –3 dB bandwidth for G = +1 is 200 MHz, at a gain of G = +10 its bandwidth will be only about 20 MHz. The AD8021 is a voltage feedback op amp with a minimal $C_{INTERNAL}$ of about 1.5 pF. By adding an external compensation capacitor, C_C, the user can circumvent the fixed gain bandwidth limitation of other voltage feedback op amps.

Unlike the typical op amp with fixed compensation, the AD8021 allows the user to

1. Maximize the amplifier bandwidth for closed-loop gains between 1 and 10, avoiding the usual loss of bandwidth and slew rate.
2. Optimize the trade-off between bandwidth and phase margin for a particular application.
3. Match bandwidth in gain blocks with different noise gains, such as when designing differential amplifiers (as shown in Figure 10).

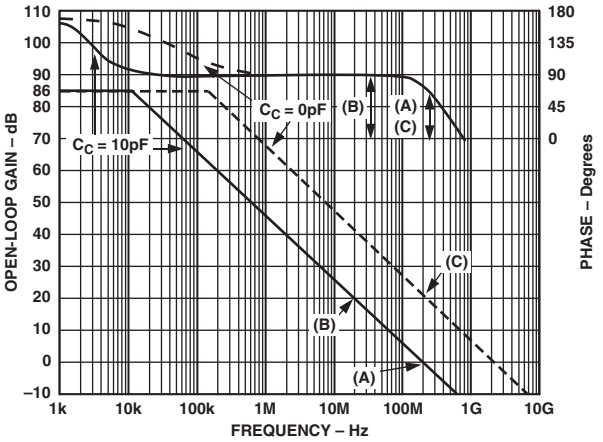


Figure 3. Simplified Diagram of Open-Loop Gain and Phase Response

Figure 3 is the AD8021 gain and phase plot that has been simplified for instructional purposes. If the desired closed-loop gain is G = +1 and C_C = 10 pF is chosen, Arrow A of the figure shows that the bandwidth is about 200 MHz and the phase margin is about 60°. If the gain is changed to G = +10 and C_C is fixed at 10 pF, then (as expected for a typical op amp) the bandwidth is degraded to about 20 MHz and the phase margin increases to 90° (Arrow B). However, by reducing C_C to zero, the bandwidth and phase margin return to about 200 MHz and 60° (Arrow C), respectively. In addition, the slew rate is dramatically increased, as it roughly varies with the inverse of C_C.

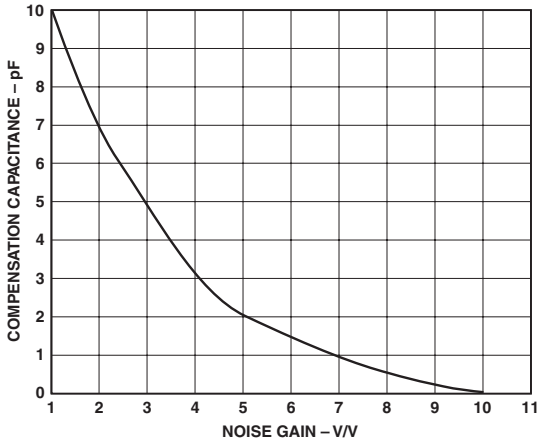


Figure 4. Suggested Compensation Capacitance vs. Gain for Maintaining 1 dB Peaking

Table I and Figure 4 provide recommended values of compensation capacitance at various gains and the corresponding slew rate, bandwidth, and noise. Note that the value of the compensation capacitor depends on the circuit noise gain, not the voltage gain. As shown in Figure 5, the noise gain, G_N, of an op amp gain block is equal to its noninverting voltage gain, regardless of whether it is actually used for inverting or noninverting gain. Thus,

$$Noninverting\ G_N = R_F / R_G + 1$$
$$Inverting\ G_N = R_F / R_G + 1$$

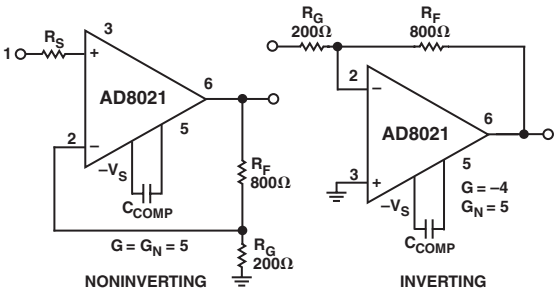


Figure 5. The Noise Gain of Both Is 5

Table I. Recommended Component Values. See Test Circuit 2. C_F = C_L = 0, R_L = 1 kΩ, R_{IN} = 49.9 Ω

Noise Gain (Noninverting Gain)	R_S (Ω)	R_F (Ω)	R_G (Ω)	C_{COMP} (pF)	Slew Rate (V/μs)	–3 dB SS BW (MHz)	Output Noise (AD8021 Only) (nV/√Hz)	Output Noise (AD8021 with Resistors) (nV/√Hz)
1	75	75	NA	10	120	490	2.1	2.8
2	49.9	499	499	7	150	205	4.3	8.2
5	49.9	1 k	249	2	300	185	10.7	15.5
10	49.9	1 k	110	0	420	150	21.2	27.9
20	49.9	1 k	52.3	0	200	42	42.2	52.7
100	49.9	1 k	10	0	34	6	211.1	264.1

With the AD8021, a variety of trade-offs can be made to fine-tune its dynamic performance. Sometimes more bandwidth or slew rate is needed at a particular gain. Reducing the compensation capacitance, as illustrated in TPC 3, will increase the bandwidth and peaking due to a decrease in phase margin. On the other hand, if more stability is needed, increasing the compensation cap will decrease the bandwidth while increasing the phase margin.

As with all high speed amplifiers, parasitic capacitance and inductance around the amplifier can affect its dynamic response. Often, the input capacitance (due to the op amp itself, as well as the PC board) could have a significant effect. The feedback resistance, together with the input capacitance, may contribute to a loss of phase margin, thereby affecting the high frequency response, as shown in TPC 10. Furthermore, a capacitor (C_F) in parallel with the feedback resistor can compensate for this phase loss.

Additionally, any resistance in series with the source will create a pole with the input capacitance (as well as dampen high frequency resonance due to package and board inductance and capacitance), the effect of which is shown in TPC 11.

It must also be noted that increasing resistor values will increase the overall noise of the amplifier, and that reducing the feedback resistor value will increase the load on the output stage, thus increasing distortion (TPC 18).

Using the Disable Feature

When Pin 8 ($\overline{\text{DISABLE}}$) is approximately 2 V or more higher than Pin 1 (LOGIC REFERENCE), the part is enabled. When Pin 8 is brought down to within about 1.5 V of Pin 1, the part is disabled. See the Specification tables for exact disable and enable voltage levels. If the disable feature is not going to be used, Pin 8 can be tied to V_S or a logic high source, and Pin 1 can be tied to ground or logic low. Alternatively, if Pin 1 and Pin 8 are not connected, the part will be in an enabled state.

THEORY OF OPERATION

The AD8021 is fabricated on the second generation of Analog Devices' proprietary High Voltage eXtra-Fast Complementary Bipolar (XFCB) process, which enables the construction of PNP and NPN transistors with similar f_Ts in the 3 GHz region. The transistors are dielectrically isolated from the substrate (and each other), eliminating the parasitic and latch-up problems caused by junction isolation. It also reduces nonlinear capacitance (a source of distortion) and allows a higher transistor f_T for a given quiescent current. The supply current is trimmed, which results in less part-to-part variation of bandwidth, slew rate, distortion, and settling time.

As shown in Figure 6, the AD8021 input stage consists of an NPN differential pair in which each transistor operates at 0.8 mA collector current. This allows the input devices a high transconductance; thus, the AD8021 has a low input noise of 2.1 nV/$\sqrt{\text{Hz}}$ @ 50 kHz. The input stage drives a folded cascode that consists of a pair of PNP transistors. The folded cascode and current mirror provide a differential to single-ended conversion of signal current. This current then drives the high impedance node (Pin 5), where the C_C external capacitor is connected. The output stage preserves this high impedance with a current gain of 5,000, so that the AD8021 can maintain a high open-loop gain even when driving heavy loads.

Two internal diode clamps across the inputs (Pins 2 and 3) protect the input transistors from large voltages that could otherwise cause emitter-base breakdown, which would result in degradation of offset voltage and input bias current.

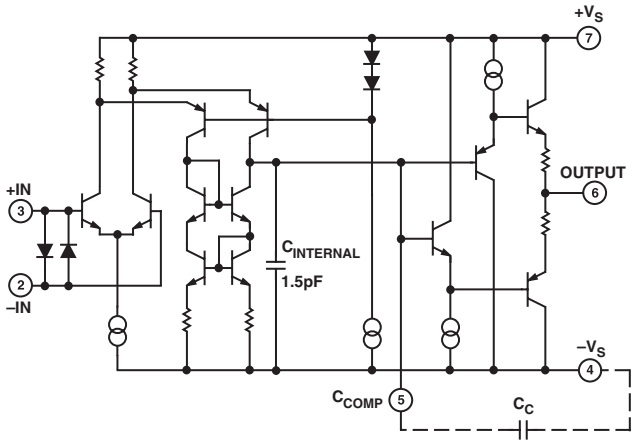


Figure 6. Simplified Schematic

PCB LAYOUT CONSIDERATIONS

As with all high speed op amps, achieving optimum performance from the AD8021 requires careful attention to PC board layout. Particular care must be exercised to minimize lead lengths between the ground leads of the bypass capacitors and between the compensation capacitor and the negative supply. Otherwise, lead inductance can influence the frequency response and even cause high frequency oscillations. Use of a multilayer printed circuit board, with an internal ground plane, will reduce ground noise and enable a compact component arrangement.

Due to the relatively high impedance of Pin 5 and low values of the compensation capacitor, a guard ring is recommended. The guard ring is simply a PC trace that encircles Pin 5 and is connected to the output, Pin 6, which is at the same potential as Pin 5. This serves two functions. It shields Pin 5 from any local circuit noise generated by surrounding circuitry. It also minimizes stray capacitance, which would tend to otherwise reduce the bandwidth. An example of a guard ring layout may be seen in Figure 7.

Also shown in Figure 7, the compensation capacitor is located immediately adjacent to the edge of the AD8021 package, spanning Pin 4 and Pin 5. This capacitor must be a high quality surface-mount COG or NPO ceramic. The use of leaded capacitors is not recommended. The high frequency bypass capacitor(s) should be located immediately adjacent to the supplies, Pins 4 and 7.

To achieve the shortest possible lead length at the inverting input, the feedback resistor R_F is located beneath the board and just spans the distance from the output, Pin 6, to inverting input Pin 2. The return node of resistor R_G should be situated as closely as possible to the return node of the negative supply bypass capacitor connected to Pin 4.

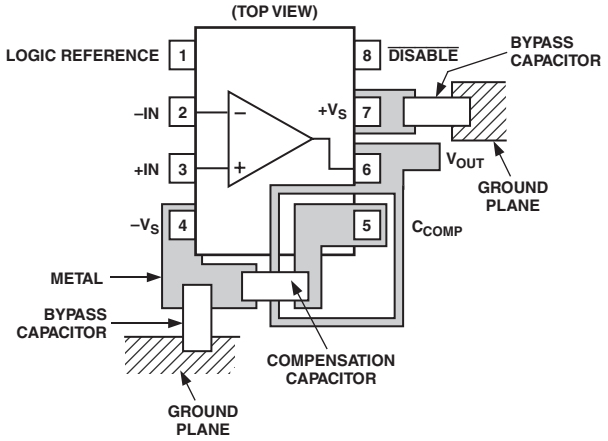


Figure 7. Recommended Location of Critical Components and Guard Ring

DRIVING 16-BIT ADCS

Low noise and adjustable compensation make the AD8021 especially suitable as a buffer/driver for high resolution analog-to-digital converters.

As seen in TPC 15, the harmonic distortion is better than 90 dB at frequencies between 100 kHz and 1 MHz. This is a real advantage for complex waveforms that contain high frequency information, as the phase and gain integrity of the sampled waveform can be preserved throughout the conversion process. The increase in loop gain results in improved output regulation and lower noise when the converter input changes state during a sample. This advantage is particularly apparent when using 16-bit high resolution ADCs with high sampling rates.

Figure 8 shows a typical ADC driver configuration. The AD8021 is in an inverting gain of –7.5, f_C is 65 kHz, and its output voltage is 10 V p-p. The results are listed in Table II.

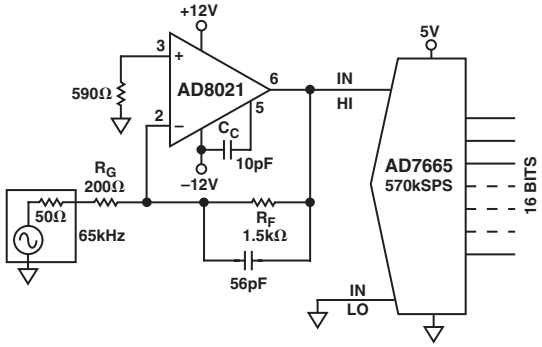


Figure 8. Inverting ADC Driver, Gain = –7.5, f_C = 65 kHz

Table II. Summary of ADC Driver Performance, f_C = 65 kHz, V_{OUT} = 10 V p-p

Parameter	Measurement	Unit
Second Harmonic Distortion	–101.3	dB
Third Harmonic Distortion	–109.5	dB
THD	–100.0	dB
SFDR	100.3	dB

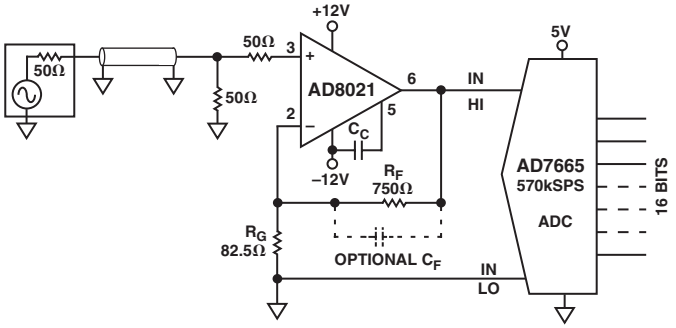


Figure 9. Noninverting ADC Driver, Gain = 10, f_C = 100 kHz

Table III. Summary of ADC Driver Performance, f_C = 100 kHz, V_{OUT} = 20 V p-p

Parameter	Measurement	Unit
Second Harmonic Distortion	–92.6	dB
Third Harmonic Distortion	–86.4	dB
THD	–84.4	dB
SFDR	5.4	dB

Figure 9 shows another ADC driver connection. The circuit was tested with a noninverting gain of 10.1 and an output voltage of approximately 20 V p-p for optimum resolution and noise performance. No filtering was used. An FFT was performed using Analog Devices' evaluation software for the AD7665 16-bit converter. The results are listed in Table III.

DIFFERENTIAL DRIVER

The AD8021 is uniquely suited as a low noise differential driver for many ADCs, balanced lines, and other applications requiring differential drive. If pairs of internally compensated op amps are configured as inverter and follower, the noise gain of the inverter will be higher than that of the follower section, resulting in an imbalance in the frequency response (see Figure 11).

A better solution takes advantage of the external compensation feature of the AD8021. By reducing the C_{COMP} value of the inverter, its bandwidth may be increased to match that of the follower, avoiding compromises in gain bandwidth and phase delay. The inverting and noninverting bandwidths can be closely matched using the compensation feature, thus minimizing distortion.

Figure 10 illustrates an inverter-follower driver circuit operating at a gain of 2, using individually compensated AD8021s. The values of feedback and load resistors were selected to provide a total load of less than 1 kΩ, and the equivalent resistances seen at each op amp's inputs were matched to minimize offset voltage and drift. Figure 12 is a plot of the resulting ac responses of driver halves.

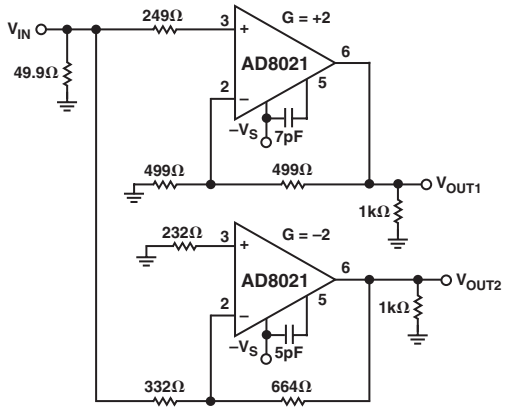


Figure 10. Differential Amplifier

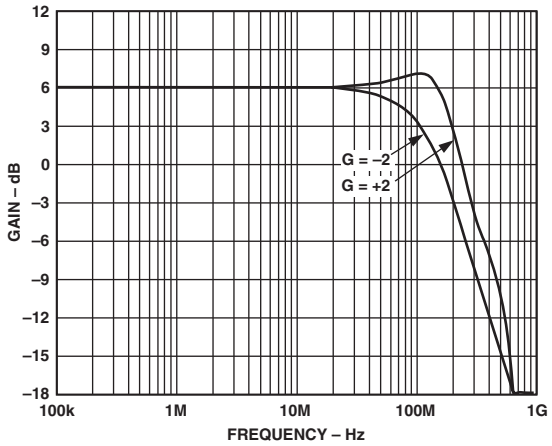


Figure 11. AC Response of Two Identically Compensated High Speed Op Amps Configured for Gains of +2 and –2

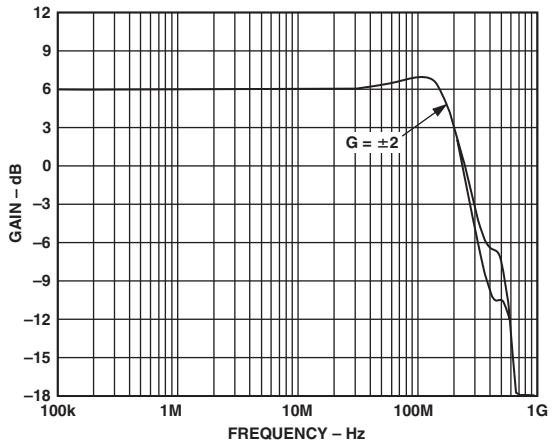


Figure12. AC Response of Two Dissimilarly Compensated AD8021 Op Amps (Figure 11) Configured for Gains of +2 and –2. Note the Close Gain Match.

USING THE AD8021 IN ACTIVE FILTERS

The low noise and high gain bandwidth of the AD8021 make it an excellent choice in active filter circuits. Most active filter literature provides resistor and capacitor values for various filters but neglects the effect of the op amp's finite bandwidth on filter performance; ideal filter response with infinite loop gain is implied. Unfortunately, real filters do not behave in this manner. Instead, they exhibit finite limits of attenuation, depending on the gain bandwidth of the active device. Good low-pass filter performance requires an op amp with high gain bandwidth for attenuation at high frequencies, and low noise and high dc gain for low frequency, pass-band performance.

Figure 13 shows the schematic of a 2-pole, low-pass active filter, and Table IV lists typical component values for filters having a Bessel-type response with gains of 2 and 5. Figure 14 is a network analyzer plot of this filter's performance.

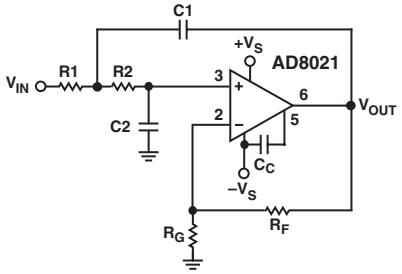


Figure 13. Schematic of a Second-Order Low-Pass Active Filter

Table IV. Typical Component Values for Second-Order Low-Pass Filter of Figure 13

Gain	R1 (Ω)	R2 (Ω)	R_F (Ω)	R_S (Ω)	C1	C2	C_C
2	71.5	215	499	499	10 nF	10 nF	7 pF
5	44.2	365	90.9	365	10 nF	10 nF	2 pF

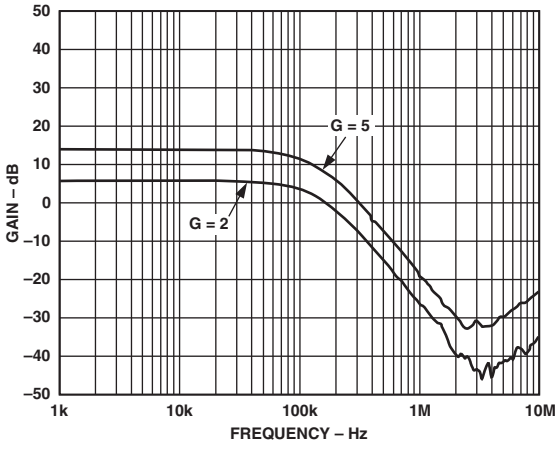


Figure 14. Frequency Response of the Filter Circuit of Figure 13 for Two Different Gains

Driving Capacitive Loads

When the AD8021 drives a capacitive load, the high frequency response may show excessive peaking before it rolls off. Two techniques can be used to improve stability at high frequency and reduce peaking. The first technique is to increase the compensation capacitor, C_C, which reduces the peaking while maintaining gain flatness at low frequencies. The second technique is to add a resistor, R_{SNUB}, in series between the output pin of the AD8021 and the capacitive load, C_L. Figure 15 shows the response of the AD8021 when both C_C and R_{SNUB} are used to reduce peaking. For a given C_L, Figure 16 can be used to determine the value of R_{SNUB} that maintains 2 dB of peaking in the frequency response. Note, however, that using R_{SNUB} attenuates the low frequency output by a factor of $R_{LOAD}/(R_{SNUB} + R_{LOAD})$.

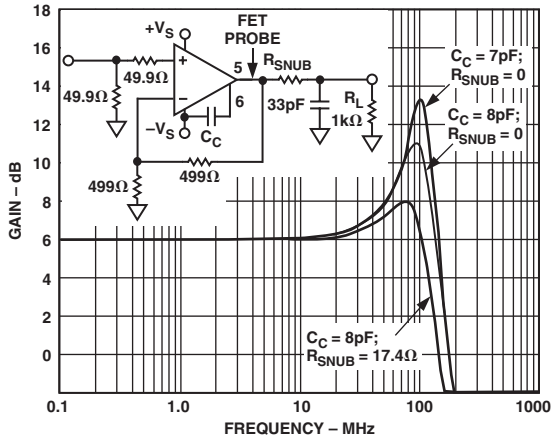


Figure 15. Peaking vs. R_{SNUB} and C_C for C_L = 33 pF

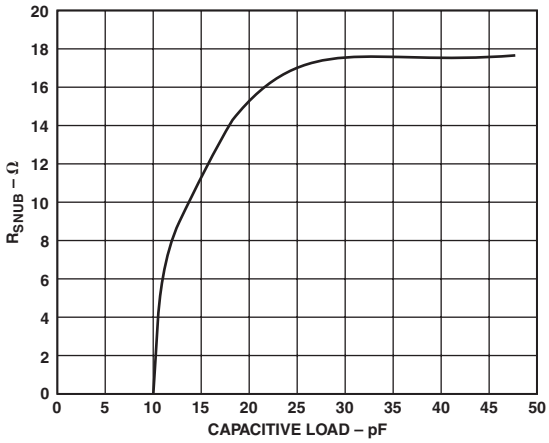
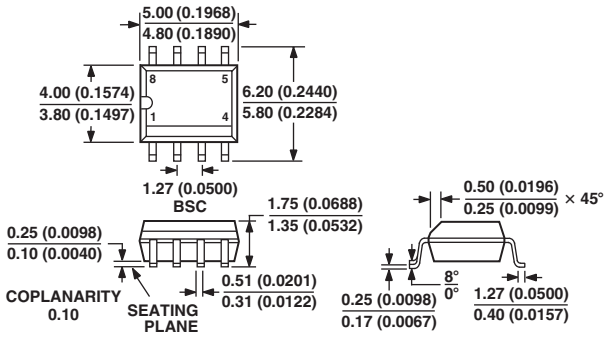


Figure 16. Relationship of R_{SNUB} vs. C_L for 2 dB Peaking at a Gain of +2

OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC]
(R-8)

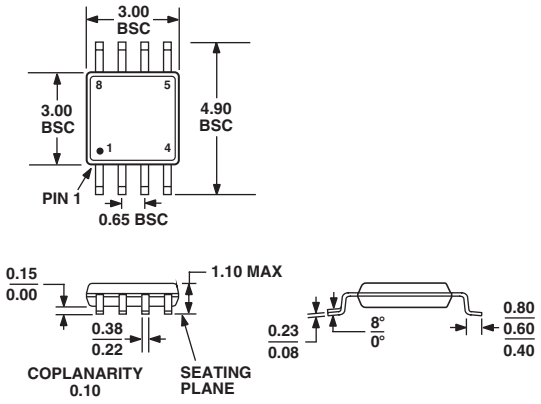
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

Revision History

Location	Page
10/03—Data Sheet changed from REV. C to REV. D.	
Edits to SPECIFICATIONS heading	3
Changes to ORDERING GUIDE	5
7/03—Data Sheet changed from REV. B to REV. C.	
Deleted all references to evaluation board	Universal
Replaced Figure 2	5
Updated OUTLINE DIMENSIONS	20
2/03—Data Sheet changed from REV. A to REV. B.	
Edits to Evaluation Board Applications	20
Edits to Figure 17	20
6/02—Data Sheet changed from REV. 0 to REV. A.	
Edits to SPECIFICATIONS	2

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