Dual High Speed Low Noise Op Amps

AD8022

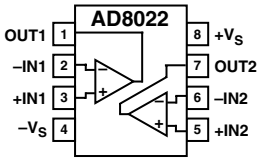
FEATURES

- Low Power Amplifiers Provide Low Noise and Low Distortion, Ideal for xDSL Modem Receiver
- Wide Supply Range: +5 V, ±2.5 V to ±12 V Voltage Supply
- Low Power Consumption
  - 4.0 mA/Amp
- Voltage Feedback
  - Ease of Use
  - Lower Total Noise (Insignificant Input Current Noise Contribution Compared to Current Feedback Amps)
- Low Noise and Distortion
  - 2.5 nV/$\sqrt{Hz}$ Voltage Noise @ 100 kHz
  - 1.2 pA/$\sqrt{Hz}$ Current Noise
  - MTPR < –66 dBc (G = +7)
  - SFDR 110 dB @ 200 kHz
- High Speed
  - 130 MHz Bandwidth (–3 dB), G = +1
  - Settling Time to 0.1%, 68 ns
  - 50 V/μs Slew Rate
- High Output Swing
  - ±10.1 V on ±12 V Supply
- Low Offset Voltage, 1.5 mV Typical

APPLICATIONS

- Receiver for ADSL, VDSL, HDSL, and Proprietary xDSL Systems
- Low Noise Instrumentation Front End
- Ultrasound Preamp
- Active Filters
- 16-Bit ADC Buffer

FUNCTIONAL BLOCK DIAGRAM
SOIC, MSOP



PRODUCT DESCRIPTION

The AD8022 consists of two low noise, high speed, voltage feedback amplifiers. Each amplifier consumes only 4.0 mA of quiescent current yet has only 2.5 nV/$\sqrt{Hz}$ of voltage noise. These dual amplifiers provide wideband, low distortion performance, with high output current optimized for stability when driving capacitive loads. Manufactured on ADI's high voltage generation of XFCB bipolar process, the AD8022 operates on a wide range of supply voltages. The AD8022 is available in both an 8-lead MSOP and an 8-lead SOIC package. Fast overvoltage recovery and wide bandwidth make the AD8022 ideal as the receive channel front end to an ADSL, VDSL or proprietary xDSL transceiver design.

In an xDSL line interface circuit, the AD8022's op amps can be configured as the differential receiver from the line transformer or as independent active filters.

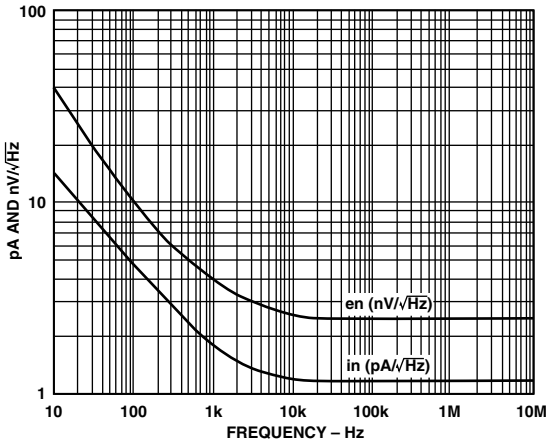


Figure 1. Current and Voltage Noise vs. Frequency

REV. A

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AD8022–SPECIFICATIONS (@ 25°C, V_S = ±12 V, R_L = 500 Ω, G = +1, T_{MIN} = –40°C, T_{MAX} = +85°C, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	V_{OUT} = 50 mV p-p	110	130		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 50 mV p-p		25		MHz
Large Signal Bandwidth[1]	V_{OUT} = 4 V p-p		4		MHz
Slew Rate	V_{OUT} = 2 V p-p, G = +2	40	50		V/µs
Rise and Fall Time	V_{OUT} = 2 V p-p, G = +2		30		ns
Settling Time 0.1%	V_{OUT} = 2 V p-p		62		ns
Overdrive Recovery Time	V_{OUT} = 150% of Max Output Voltage, G = +2		200		ns
NOISE/DISTORTION PERFORMANCE					
Distortion	V_{OUT} = 2 V p-p				
Second Harmonic	f_C = 1 MHz		–95		dBc
Third Harmonic	f_C = 1 MHz		–100		dBc
Multitone Input Power Ratio[2]	G = +7 Differential				
	26 kHz to 132 kHz		–67.2		dBc
	144 kHz to 1.1 MHz		–66		dBc
Voltage Noise (RTI)	f = 100 kHz		2.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.2		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			–1.5	±6	mV
	T_{MIN} to T_{MAX}			±7.25	mV
Input Offset Current			±120		nA
Input Bias Current			2.5	5.0	µA
	T_{MIN} to T_{MAX}			±7.5	µA
Open-Loop Gain			72		dB
INPUT CHARACTERISTICS					
Input Resistance (Differential)			20		kΩ
Input Capacitance			0.7		pF
Input Common-Mode Voltage Range			–11.25 to +11.75		V
Common-Mode Rejection Ratio	V_{CM} = ±3 V		98		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 500 Ω		±10.1		V
	R_L = 2 kΩ		±10.6		V
Linear Output Current	G = +1, R_L = 150, DC Error = 1%		±55		mA
Short Circuit Output Current			100		mA
Capacitive Load Drive	R_S = 0 Ω, <3 dB of Peaking		75		pF
POWER SUPPLY					
Operating Range		+4.5		±13.0	V
Quiescent Current			4.0	5.5	mA/Amp
	T_{MIN} to T_{MAX}			6.1	mA/Amp
Power Supply Rejection Ratio	V_S = ±5 V to ±12 V		80		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTES

[1]FPBW = Slew Rate/(2 πV_{PEAK}).

[2]Multitone testing performed with 800 mV rms across a 500 Ω load at Points A and B on TPC 20.

Specifications subject to change without notice.

SPECIFICATIONS (@ 25°C, V_S = ±2.5 V, R_L = 500 Ω, G = +1, T_{MIN} = –40°C, T_{MAX} = +85°C, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	V_{OUT} = 50 mV p-p	100	120		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 50 mV p-p		22		MHz
Large Signal Bandwidth[1]	V_{OUT} = 3 V p-p		4		MHz
Slew Rate	V_{OUT} = 2 V p-p, G = +2	30	42		V/µs
Rise and Fall Time	V_{OUT} = 2 V p-p, G = +2		40		ns
Settling Time 0.1%	V_{OUT} = 2 V p-p		75		ns
Overdrive Recovery Time	V_{OUT} = 150% of Max Output Voltage, G = +2		225		ns
NOISE/DISTORTION PERFORMANCE					
Distortion	V_{OUT} = 2 V p-p				
Second Harmonic	f_C = 1 MHz		–77.5		dBc
Third Harmonic	f_C = 1 MHz		–94		dBc
Multitone Input Power Ratio[2]	G = +7 Differential, V_S = ±6 V				
	26 kHz to 132 kHz		–69		dBc
	144 kHz to 1.1 MHz		–66.7		dBc
Voltage Noise (RTI)	f = 100 kHz		2.3		nV/√Hz
Input Current Noise	f = 100 kHz		1		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			–0.8	±5.0	mV
	T_{MIN} to T_{MAX}			±6.25	mV
Input Offset Current			±65		nA
Input Bias Current			2.0	5.0	µA
	T_{MIN} to T_{MAX}			7.5	µA
Open-Loop Gain			64		dB
INPUT CHARACTERISTICS					
Input Resistance (Differential)			20		kΩ
Input Capacitance			0.7		pF
Input Common-Mode Voltage Range			–1.83 to +2.0		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V V_S = ±5.0 V		98		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 500 Ω		–1.38 to +1.48		V
Linear Output Current	G = +1, R_L = 100, DC Error = 1%		±32		mA
Short Circuit Output Current			80		mA
Capacitive Load Drive	R_S = 0 Ω, <3 dB of Peaking		75		pF
POWER SUPPLY					
Operating Range		+4.5		±13.0	V
Quiescent Current			3.5	4.25	mA/Amp
	T_{MIN} to T_{MAX}			4.4	mA/Amp
Power Supply Rejection Ratio	ΔV_S = ±1 V		86		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTES

[1]FPBW = Slew Rate/(2 π V_{PEAK}).

[2]Multitone testing performed with 800 mV rms across a 500 Ω load at Points A and B on TPC 20.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 26.4 V
Internal Power Dissipation[2]
Small Outline Package (R) . . . . . 1.6 W
MSOP Package (RM) . . . . . 1.2 W
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±0.8 V
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range RM, R . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for the device in free air:
8-Lead SOIC Package: θ_{JA} = 160°C/W.
8-Lead MSOP Package: θ_{JA} = 200°C/W.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8022 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8022 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8022AR	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD8022ARM	–40°C to +85°C	8-Lead MSOP	RM-8
AD8022AR-EVAL		Evaluation Board	SO-8

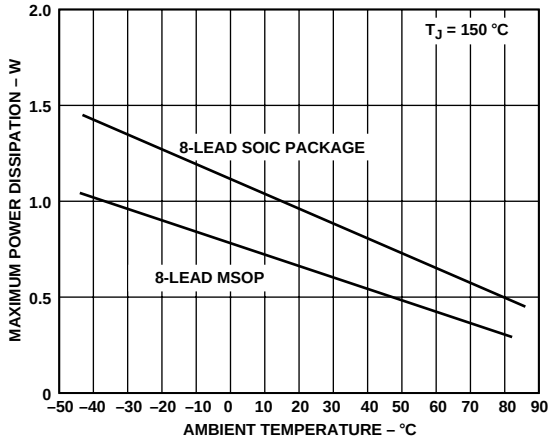
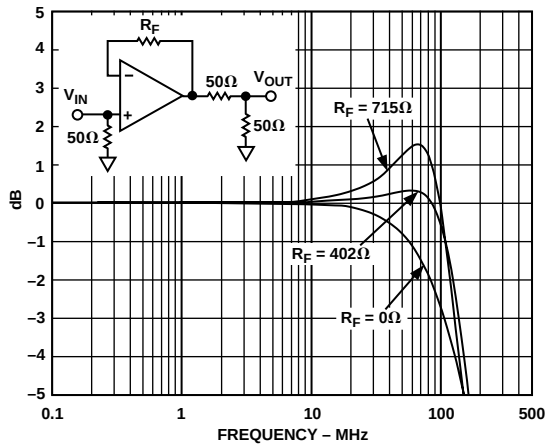


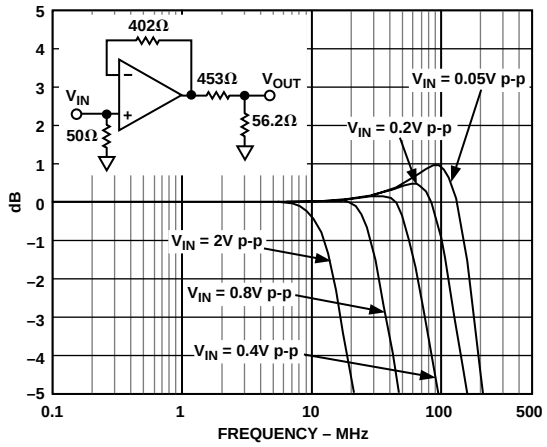
Figure 2. Plot of Maximum Power Dissipation vs. Temperature

CAUTION

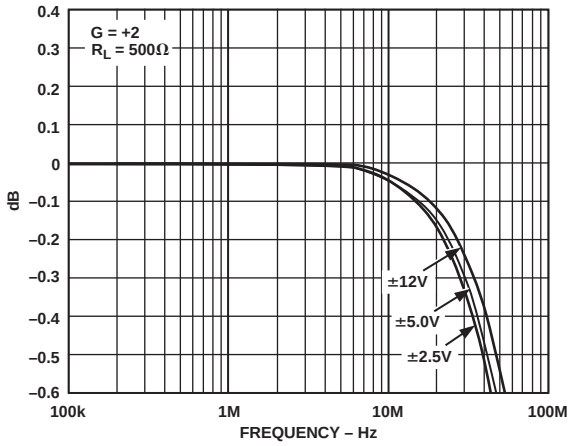
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8022 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



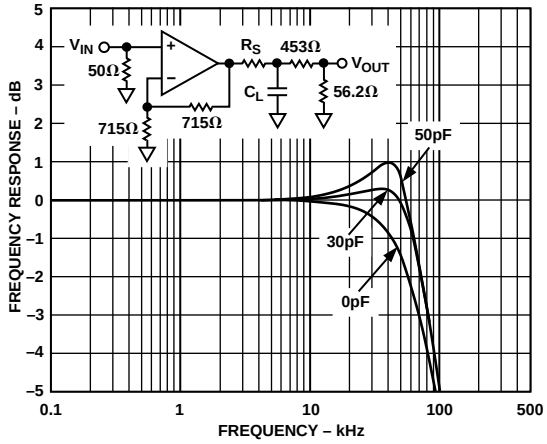
TPC 1. Frequency Response vs. R_F, G = +1, V_S = ±12 V, V_{IN} = 63 mV p-p



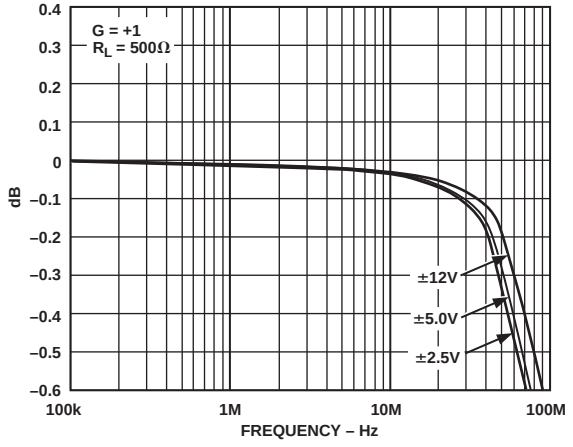
TPC 4. Frequency Response vs. Signal Level, V_S = ±12 V, G = +1



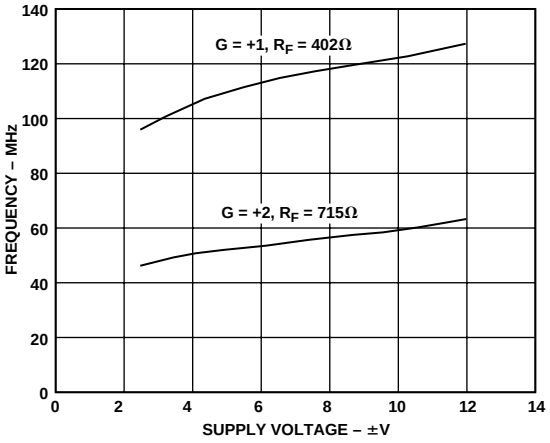
TPC 2. Fine-Scale Gain Flatness vs. Frequency, G = +2



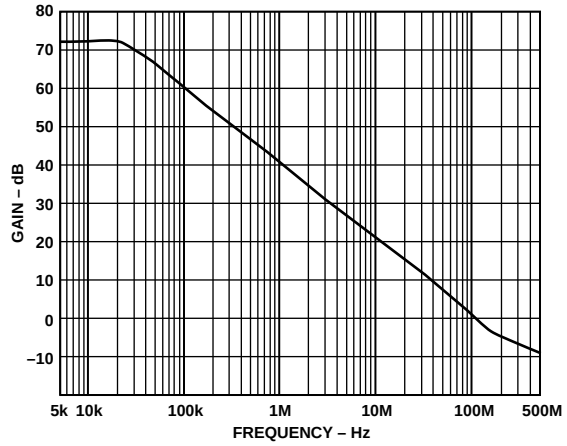
TPC 5. Frequency Response vs. Capacitive Load, C_L = 0 pF, 30 pF, and 50 pF, R_S = 0 Ω



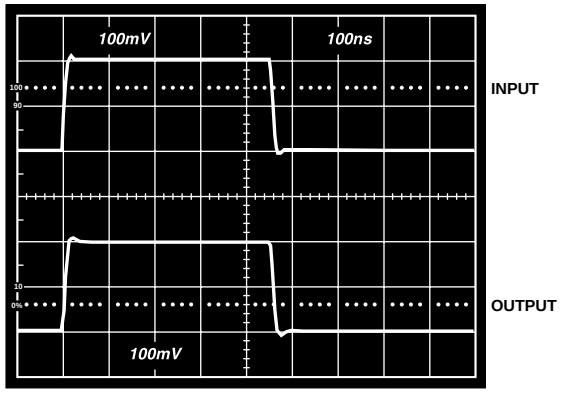
TPC 3. Fine-Scale Gain Flatness vs. Frequency, G = +1



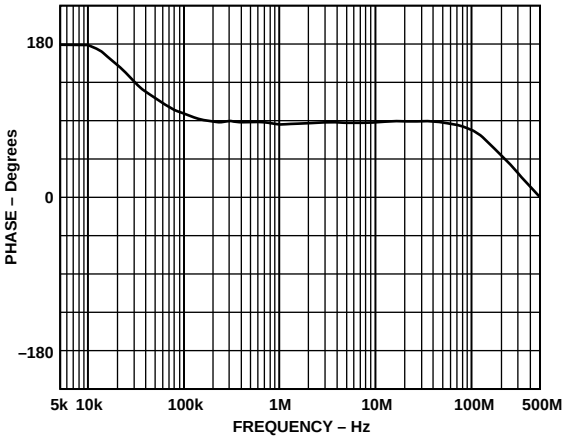
TPC 6. Bandwidth vs. Supply, R_L = 500 Ω, V_{IN} = 200 mV p-p



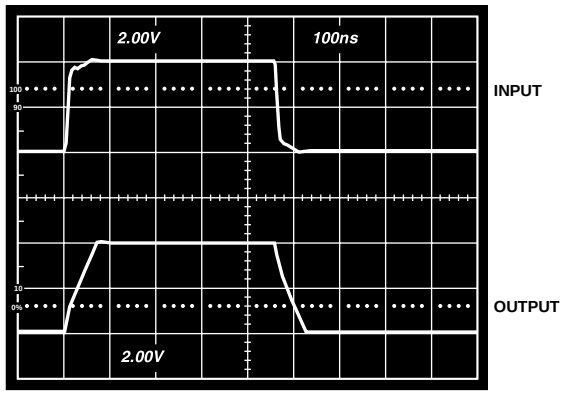
TPC 7. Open-Loop Gain



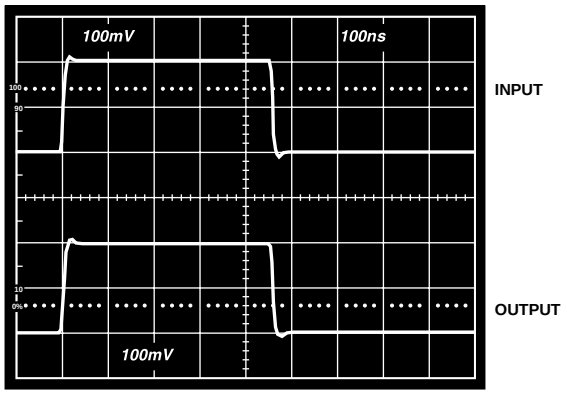
TPC 10. Noninverting Small Signal Pulse Response, R_L = 500 Ω, V_S = ±2.5 V, G = +1, R_F = 0



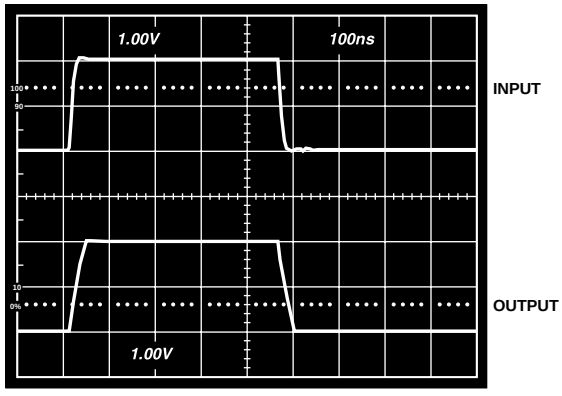
TPC 8. Open-Loop Phase



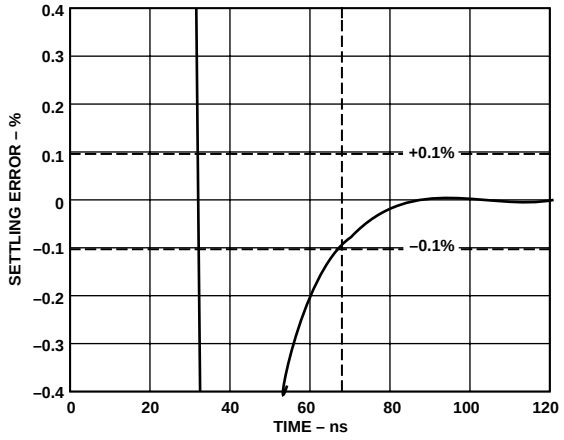
TPC 11. Noninverting Large Signal Pulse Response, R_L = 500 Ω, V_S = ±12 V, G = +1, R_F = 0



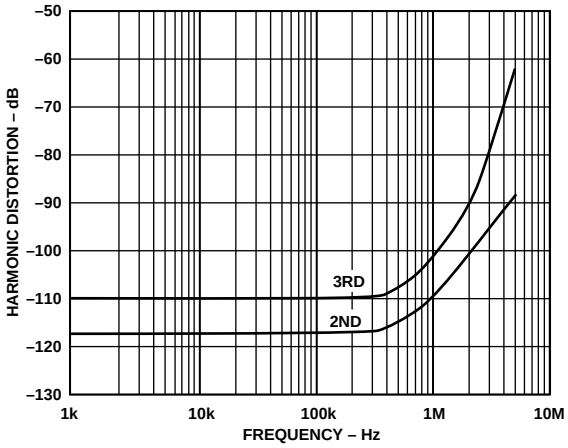
TPC 9. Noninverting Small Signal Pulse Response, R_L = 500 Ω, V_S = ±12 V, G = +1, R_F = 0



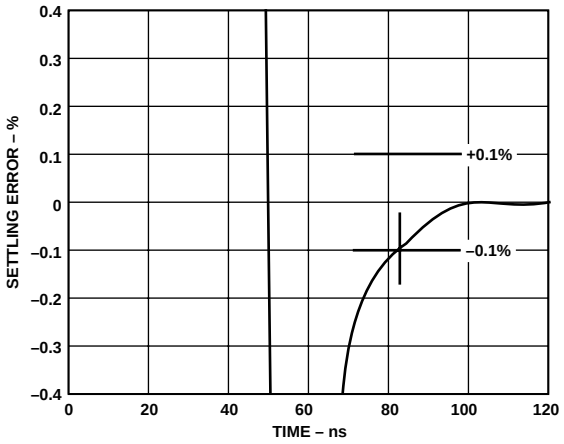
TPC 12. Noninverting Large Signal Pulse Response, R_L = 500 Ω, V_S = ±2.5V, G = +1, R_F = 0



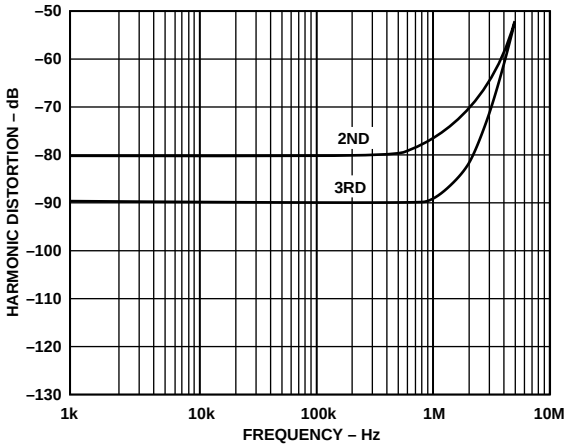
TPC 13. Settling Time to 0.1%, $V_S = \pm 12$ V, Step Size = 2 V p-p, G = +2, $R_L = 500\ \Omega$



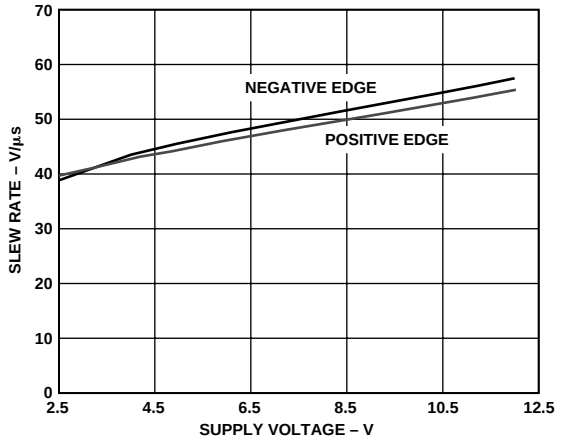
TPC 16. Distortion vs. Frequency, $V_S = \pm 12$ V, $R_L = 500\ \Omega$, $R_F = 0\ \Omega$, $V_{OUT} = 2$ V p-p, G = +1



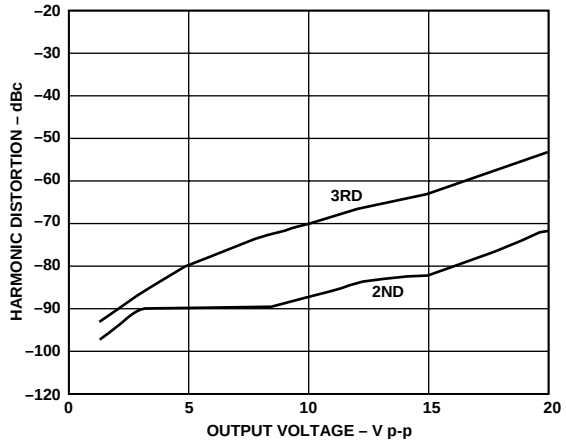
TPC 14. Settling Time to 0.1%, $V_S = \pm 2.5$ V, Step Size = 2 V p-p, G = +2, $R_L = 500\ \Omega$



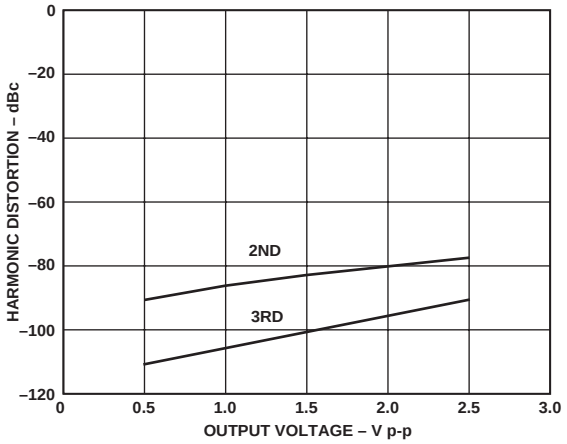
TPC 17. Distortion vs. Frequency, $V_S = \pm 2.5$ V, $R_L = 500\ \Omega$, $R_F = 0\ \Omega$, $V_{OUT} = 2$ V p-p, G = +1



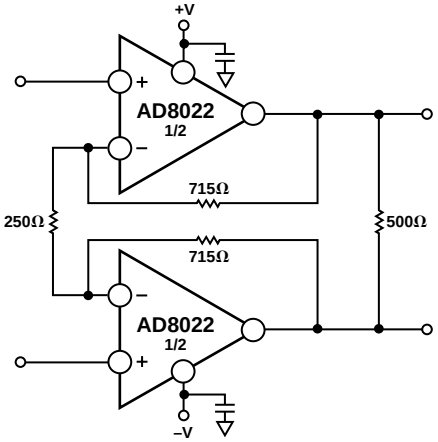
TPC 15. Slew Rate vs. Supply Voltage, G = +2



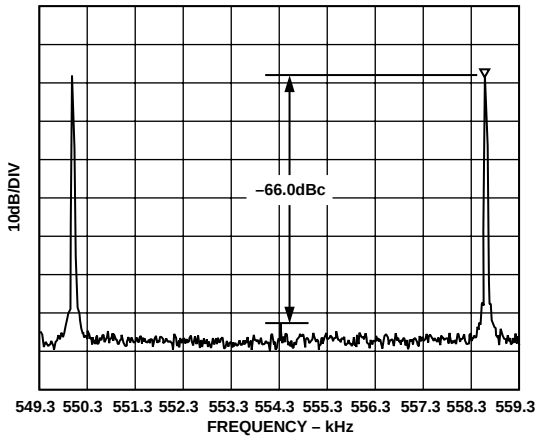
TPC 18. Distortion vs. Output Voltage, $V_S = \pm 12$ V, G = +2, f = 1 MHz, $R_L = 500\ \Omega$, $R_F = 715\ \Omega$



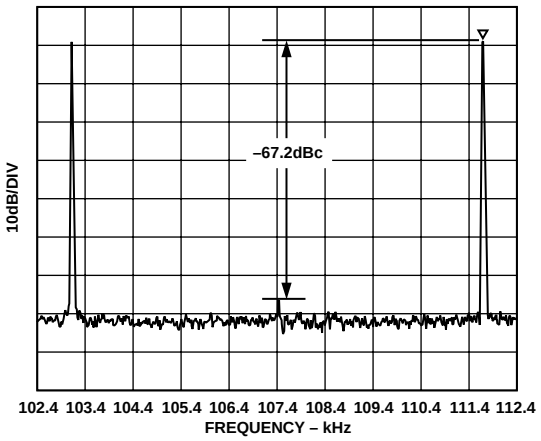
TPC 19. Distortion vs. Output Voltage, $V_S = \pm 2.5$ V, G = +1, f = 1 MHz, $R_L = 500\ \Omega$, $R_F = 0\ \Omega$



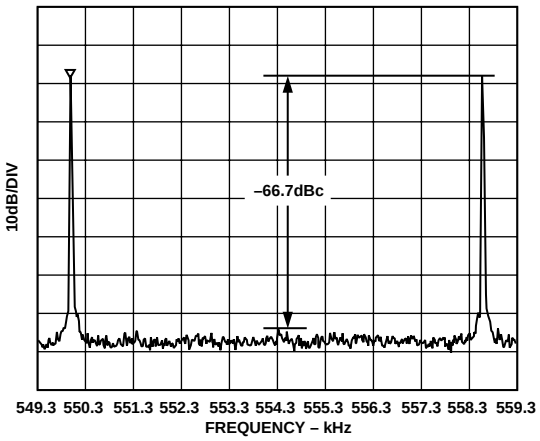
TPC 20. Multitone Power Ratio Test Circuit



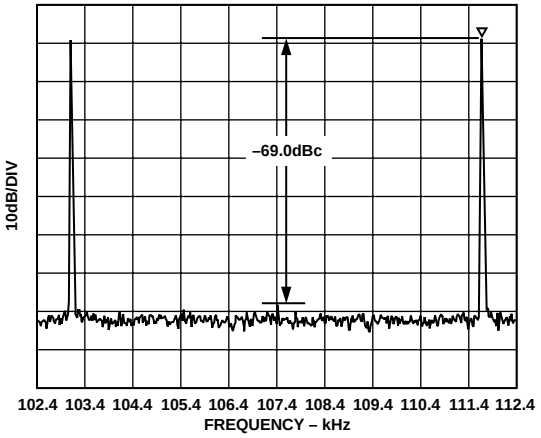
TPC 21. Multitone Power Ratio: $V_S = \pm 12$ V, $R_L = 500\ \Omega$, Full Rate ADSL (DMT), Downstream



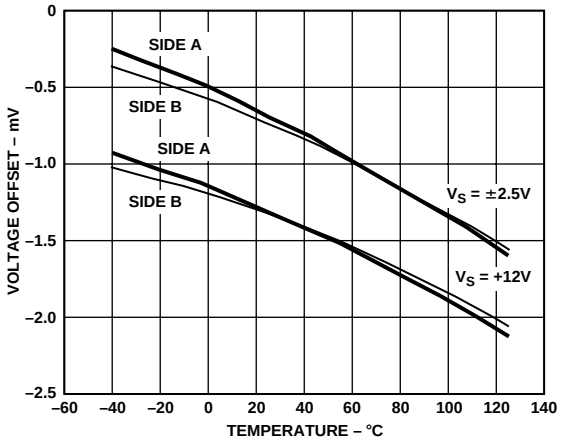
TPC 22. Multitone Power Ratio: $V_S = \pm 12$ V, $R_L = 500\ \Omega$, Full Rate ADSL (DMT), Upstream



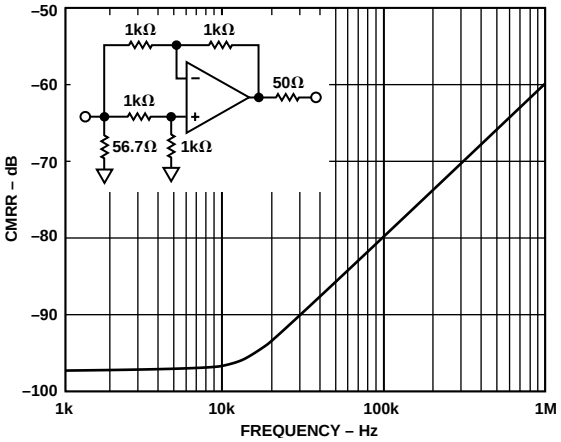
TPC 23. Multitone Power Ratio: $V_S = \pm 6$ V, $R_L = 500\ \Omega$, Full Rate ADSL (DMT), Downstream



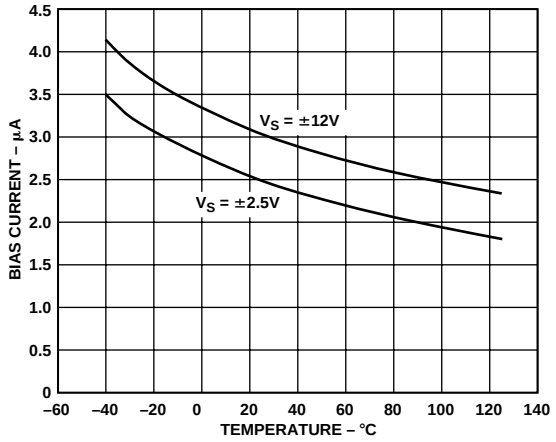
TPC 24. Multitone Power Ratio: $V_S = \pm 6$ V, $R_L = 500\ \Omega$, Full Rate ADSL (DMT), Upstream



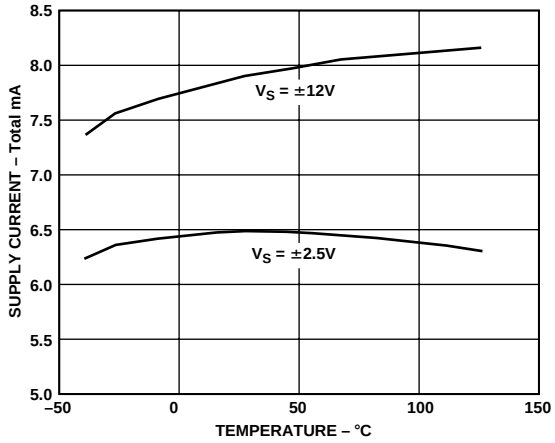
TPC 25. Voltage Offset vs. Temperature



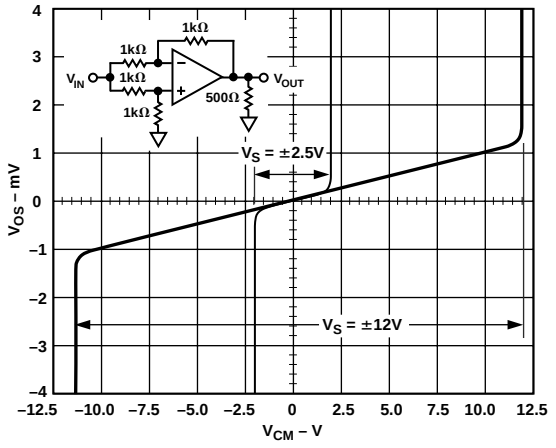
TPC 28. CMRR vs. Frequency



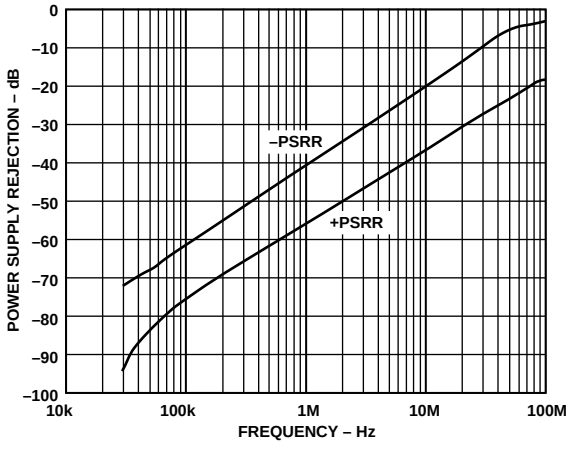
TPC 26. Bias Current vs. Temperature



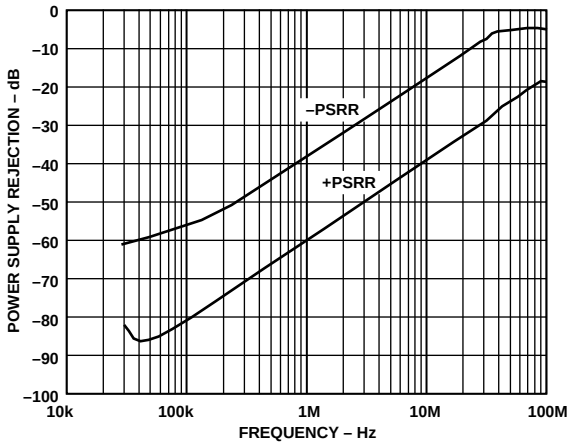
TPC 29. Total Supply Current vs. Temperature



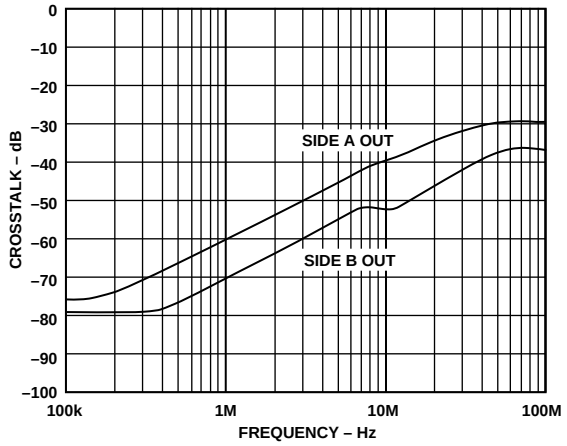
TPC 27. Voltage Offset vs. Input Common-Mode Voltage



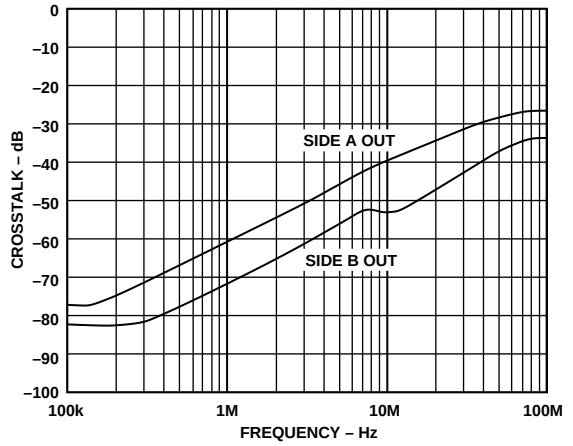
TPC 30. Power Supply Rejection vs. Frequency, V_S = ±12 V



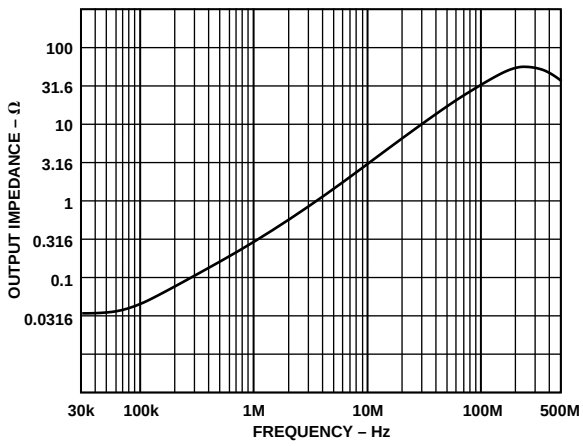
TPC 31. Power Supply Rejection vs. Frequency, $V_S = \pm 2.5$ V



TPC 33. Output-to-Output Crosstalk vs. Frequency, $V_S = \pm 2.5$ V



TPC 32. Output-to-Output Crosstalk vs. Frequency, $V_S = \pm 12$ V



TPC 34. Output Impedance vs. Frequency, $V_S = \pm 12$ V

THEORY OF OPERATION

The AD8022 is a voltage-feedback op amp designed especially for ADSL or other applications requiring very low voltage and current noise along with low supply current, low distortion, and ease of use.

The AD8022 is fabricated on Analog Devices' proprietary eXtra-Fast Complementary Bipolar (XFCB) process, which enables the construction of PNP and NPN transistors with similar fTs in the 4 GHz region. The process is dielectrically isolated to eliminate the parasitic and latch-up problems caused by junction isolation. These features enable the construction of high frequency, low distortion amplifiers with low supply currents.

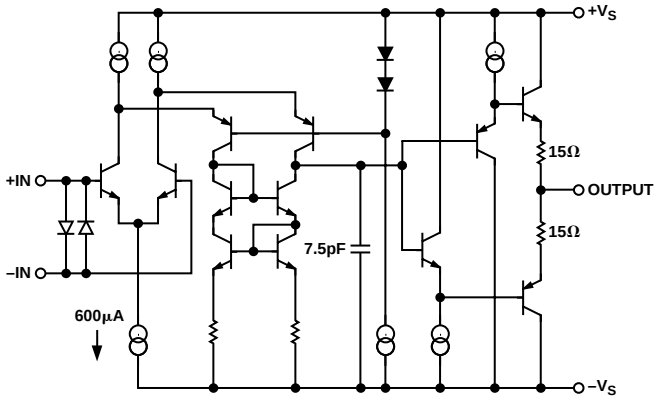


Figure 3. Simplified Schematic

As shown in Figure 3, the AD8022 input stage consists of an NPN differential pair in which each transistor operates a 300 µA collector current. This gives the input devices a high transconductance and hence gives the AD8022 low-input noise of 2.5 nV/√Hz @ 100 kHz. The input stage drives a folded cascode that consists of a pair of PNP transistors. These PNP's then drive a current mirror that provides a differential input to single-ended-output conversion. The output stage provides a high current gain of 10,000, so that the AD8022 can maintain a high dc open-loop gain, even into low load impedances.

APPLICATIONS

The low noise AD8022 dual xDSL receiver amplifier is specifically designed for the dual differential receiver amplifier function within xDSL transceiver hybrids, as well as other low noise amplifier applications. The AD8022 may be used in receiving modulated signals including discrete multitone (DMT) on either end of the subscriber loop. Communication systems designers can be challenged when designing an xDSL modem transceiver hybrid capable of receiving the smallest signals embedded in noise that inherently exists on twisted pair phone lines. Noise sources include near end crosstalk (NEXT), far end crosstalk (FEXT), background, and impulse noise, all of which are fed, to some degree, into the receiver front end. Based on a Bellcore noise survey, the background noise level for typical twisted pair telephone loops is said to be –140 dBm/√Hz or 31 nV/√Hz. It is therefore important to minimize the noise added by the receiver amplifiers in order to preserve as much signal-to-noise ratio (SNR) as possible. With careful transceiver hybrid design using the AD8022 dual low noise receiver amplifier, maintaining power density levels lower than –140 dBm/√Hz in ADSL modems is easily achieved.

DMT Modulation and Multitone Power Ratio (MTPR)

ADSL systems rely on discrete multitone DMT modulation to carry digital data over phone lines. DMT modulation appears in the frequency domain as power contained in several individual frequency subbands, sometimes referred to as tones or bins, each of which is uniformly separated in frequency. (See TPCs 21, 22, 23, and 24 for MTPR results while the AD8022 receives DMT driving 800 mV rms across 500 Ω differential load.) A uniquely encoded quadrature amplitude modulation (QAM) signal occurs at the center frequency of each subband or tone. Difficulties will exist when decoding these subbands if a QAM signal from one subband is corrupted by the QAM signal(s) from other subbands, regardless of whether the corruption comes from an adjacent subband or harmonics of other subbands. Conventional methods of expressing the output signal integrity of line receivers, such as spurious-free dynamic range (SFDR), single tone harmonic distortion or THD, two-tone intermodulation distortion (IMD), and third order intercept (IP3), become significantly less meaningful when amplifiers are required to process DMT and other heavily modulated waveforms. A typical xDSL downstream DMT signal may contain as many as 256 carriers (subbands or tones) of QAM signals. MTPR is the relative difference between the measured power in a typical subband (at one tone or carrier) versus the power at another subband specifically selected to contain no QAM data. In other words, a selected subband (or tone) remains open or void of intentional power (without a QAM signal) yielding an empty frequency bin. MTPR, sometimes referred to as the "empty bin test," is typically expressed in dBc, similar to expressing the relative difference between single tone fundamentals and second or third harmonic distortion components. Measurements of MTPR are typically made at the output of the receiver directly across the differential load. Other components aside, the receiver function of an ADSL transceiver hybrid will be affected by the turns ratio of the selected transformers within the hybrid design. Since a transformer reflects the secondary voltage back to the primary side by the inverse of the turns ratio, 1/N, increasing the turns ratio on the secondary side reduces the voltage across the primary side inputs of the differential receiver. Increasing the turns ratio of the transformers may inadvertently cause a reduction of the SNR by reducing the received signal strength.

Channel Capacity and SNR

The efficiency of an ADSL system in delivering the digital data embedded in the DMT signals can be compromised when the noise power of the transmission system increases. The graph below shows the relationship between SNR and the relative maximum number of bits per tone or subband while maintaining a bit error rate at 1E-7 errors per second.

Figure 4. ADSL DMT SNR vs. Bits/Tone

Generating DMT

At this time, DMT modulated waveforms are not typically menu selectable items contained within arbitrary waveform generators (AWG). AWGs that are available today may not deliver DMT signals sufficient in performance with regard to MTPR due to limitations in the D/A converters and output amplifiers used by AWG manufacturers. Similar to evaluating single tone distortion performance of an amplifier, MTPR evaluation requires a DMT signal generator capable of delivering MTPR performance better than that of the driver under evaluation. Generating DMT signals can be accomplished using a Tektronics AWG 2021 equipped with Opt 4, (12-bit/24-bit, TTL digital data out), digitally coupled to Analog Devices' AD9754, a 14-bit TxDAC, buffered by an AD8002 amplifier configured as a differential driver. See Figure 5 for schematics of a circuit used to generate DMT signals that can achieve down to –80 dBc of MTPR performance, sufficient for use in evaluating xDSL receivers. WFM files are needed to produce the necessary digital data required to drive the TxDAC from the optional TTL digital data output of the TEK AWG2021. Copies of .WFM files for upstream and downstream DMT waveforms with a peak-to-average ratio (crest factor) of ~5.3 can be obtained through the Analog Devices website:
http://products.analog.com/products/info.asp?product=AD8022.

Upstream data is contained in the ...24.wfm files and downstream data in the ...128.wfm files. These DMT modulated signals are used to evaluate xDSL products for multitone power ratio or MTPR performance. The data files are used in pairs (e.g., adslu24.wfm and adsll24.wfm go together) and are loaded into Tektronics AWG2021 arbitrary waveform generator. The adslu24.wfm is loaded via the TEK AWG2021 floppy drive into Channel 1, while the adsll24.wfm is simultaneously loaded into Channel 2. The number in the file name, prefixed with 'u,' goes into CH1 or upper channel and the 'l' goes into CH2 or the lower channel. Twelve bits from channel CH1 are combined with two bits from CH2 to achieve 14-bit digital data at the digital outputs of the TEK 2021. The resulting waveforms produced at the AD9754-EB outputs are then buffered and amplified by the AD8002 differential driver to achieve 14-bit performance from this DMT signal source.

Power Supply and Decoupling

The AD8022 should be powered with a good quality (i.e., low noise) dual supply of ±12 V for the best overall performance. The AD8022 circuit will also function at voltages lower than ±12 V. Careful attention must be paid to decoupling the power supply pins. A pair of 10 µF capacitors located in near proximity to the AD8022 is required to provide good decoupling for lower frequency signals. In addition, 0.1 µF decoupling capacitors should be located as close to each of the power supply pins as is physically possible.

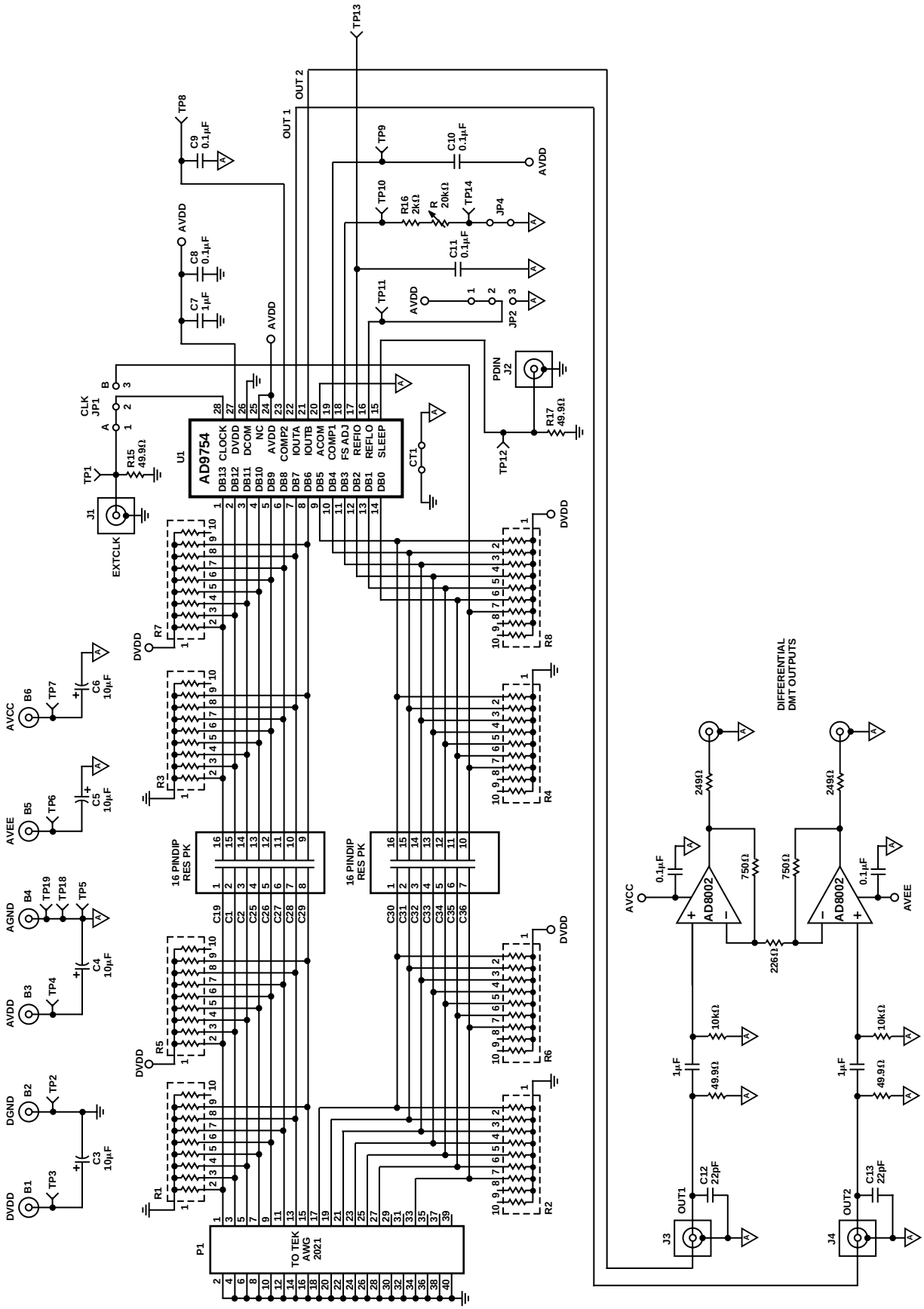


Figure 5. DMT Signal Generator Schematic

EVALUATION BOARDS

The evaluation board schematic of Figure 8 is our standard dual SOIC noninverting evaluation circuit, offering the ability to evaluate the AD8022 in typical op amp circuits, available from Analog Devices Inc. In addition, the AD8022 receiver function may be added to on our ADSL EVAL boards. The AD8016ARB-EVAL, the AD8016ARP-EVAL, AD8017AR-EVAL, and AD8018ARU-EVAL boards are available through Analog Devices. These platforms provide the capability to fully evaluate the Analog Devices ADSL transceiver hybrid. All of the ADSL evaluation boards mentioned above can accommodate the evaluation of the AD8022 as a receiver amplifier when installed in the U2 location. The receiver circuit on these boards is typically unpopulated. Requesting samples of the AD8022 along with the EVAL board of your choice will provide the capability to evaluate the AD8022 along with many other Analog Devices ADSL line driver products in a typical transceiver circuit. The evaluation circuits have been designed to replicate the CPE or CO side analog transceiver hybrid circuits.

The ADSL EVAL circuits mentioned above are designed using a two transformer transceiver topology, including a line receiver, line driver, line matching network, an RJ11 jack for interfacing to line simulators, and transformer-coupled inputs for single-to-differential input conversion.

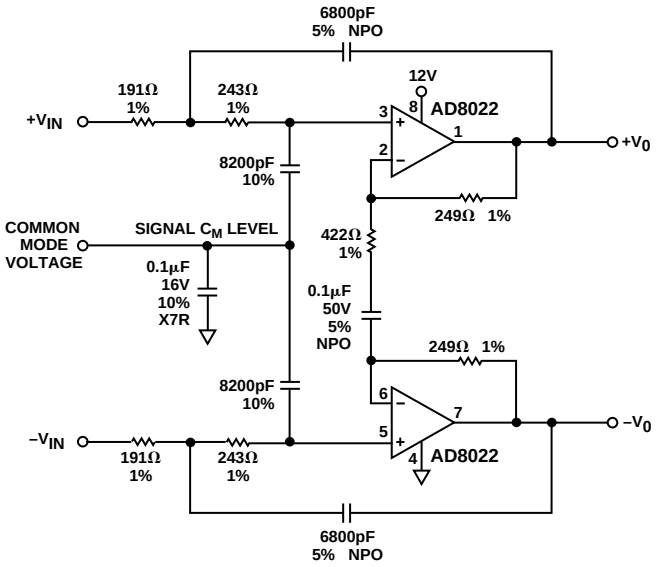


Figure 6. Differential Input Sallen-Key Filter Using AD8022 on Single Supply, +12 V

Layout Considerations

As is the case with all "high speed" amplifiers, careful attention to printed circuit board layout details will prevent associated board parasitics from becoming problematic. Proper RF design technique is mandatory. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low-impedance return path. Removing the ground plane from the area near the input signal lines will reduce stray capacitance. Chip capacitors should be used for the supply bypassing. One end of the capacitor should be connected to the ground plane and the other no more than 1/8 inch away from each supply pin. An additional large (0.47 μF to 10 μF) tantalum capacitor should be connected in parallel, although not necessarily as close, in order to supply current for fast, large signal changes at the AD8022 output. Signal lines connecting the feedback and gain resistors should be as short as possible, minimizing the inductance and stray capacitance associated with these traces. Locate termination resistors and loads as close as possible to the input(s) and output respectively. Adhere to stripline design techniques for long signal traces (greater than about 1 inch). Following these generic guidelines will improve the performance of the AD8022 in all applications.

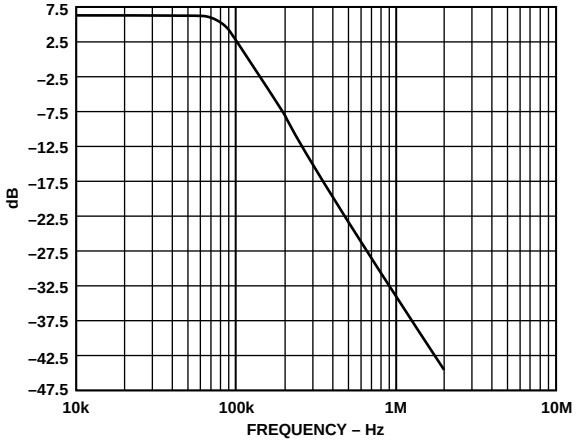


Figure 7. Frequency Response of Sallen-Key Filter

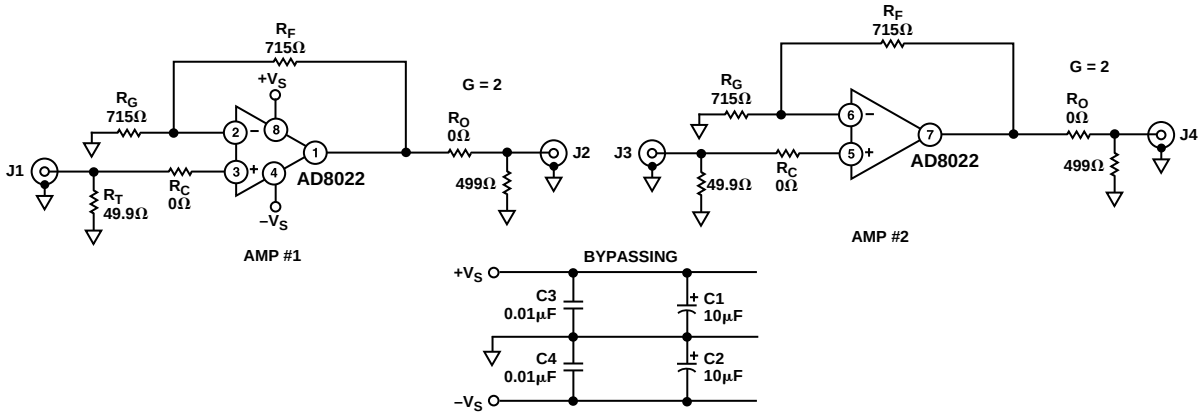
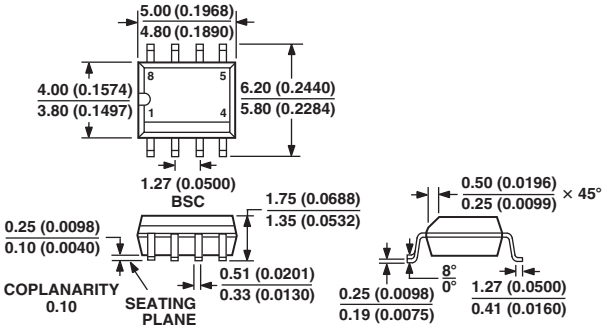


Figure 8. Evaluation Board Schematic

OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

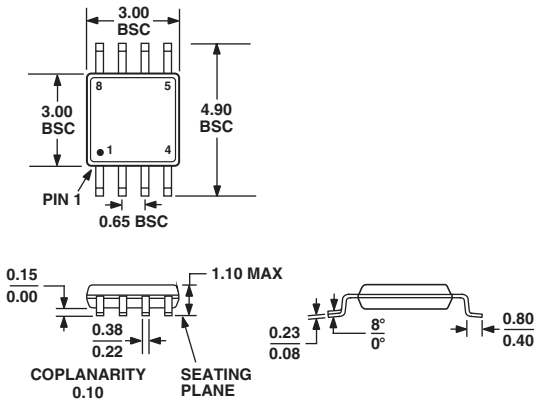


CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

COMPLIANT TO JEDEC STANDARDS MS-012AA

8-Lead MSOP Package [MSOP]
(RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

C01053–0–9/02(A)

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