

FEATURES

Voltage Feedback, Rail-to-Rail Output
Rated Settling Time to Within 0.5 V of Supply Rail
Quad High Speed Amplifier
 Settling Time to 0.1% of 55 ns (4 V Swing, $C_L = 100$ pF)
 Slew Rate 135 V/ μ s (4 V Swing)
 -3 dB Bandwidth 60 MHz
 Fixed Gain Resistors for High DC Accuracy
 Low Voltage Offset 0.5 mV RTO Typical
 Gain Error Less than 0.05%
 Low Supply Current 3.4 mA
 Nominal +12 V Supply
 14-Lead SOIC Package

APPLICATIONS

LCD Source Drivers
 CD DVD
 CDR

PRODUCT DESCRIPTION

The AD8026 is a complete low cost, closed loop, voltage feedback, quad amplifier. Precision trimmed resistors set a fixed R_F/R_G ratio of 5/3 to a typical gain accuracy of 0.02%. Manufactured on ADI's proprietary XFCB high speed bipolar process, which enables the output drivers to settle to within 0.1% within 55 ns into a 100 pF load (4 V swing) and drive output voltages to rated settling time to within 0.5 V from the rail. The typical 3 dB bandwidth is 60 MHz, at $G = +2.67$. The AD8026 is laser trimmed to produce both exceptional offset and gain performance.

The low settling time, high slew rate, low offset and rail-to-rail output voltage drive capability makes the AD8026 ideal for driving LCD displays.

The AD8026 is available in a 14-lead SOIC package.

FUNCTIONAL BLOCK DIAGRAM

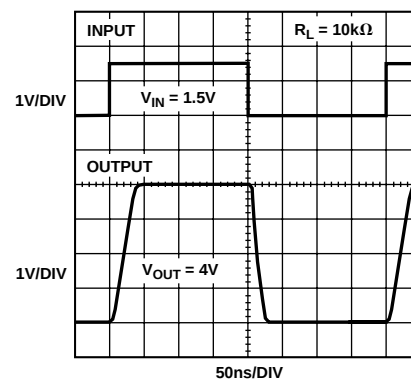
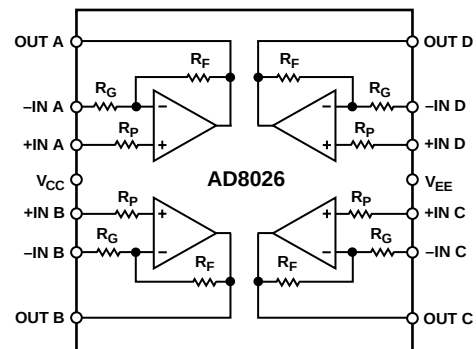


Figure 1. 4 V Step Response

REV. 0

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AD8026—SPECIFICATIONS

(@ +25°C, $V_S = \pm 6\text{ V}$, $R_I = 500\ \Omega$, $R_L = 10\text{ k}\Omega$, $R_F = 5\text{ k}\Omega$, $R_G = 3\text{ k}\Omega$ Noninverting Configuration, $T_{\text{MIN}} = 0^\circ\text{C}$, $T_{\text{MAX}} = +70^\circ\text{C}$, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	$V_{\text{IN}} = 50\text{ mV rms}$ $R_L = 1\text{ k}\Omega$	20	60		MHz
Bandwidth for 0.1 dB Flatness	$V_{\text{IN}} = 50\text{ mV rms}$ $R_L = 1\text{ k}\Omega$		12		MHz
Slew Rate	$V_O = 4\text{ V Step}$		135		V/ μs
Full Power Response	$V_O = 2\text{ V p-p}$		10		MHz
Settling Time to 0.1%	$V_O = 4\text{ V Step}$, $C_L = 100\text{ pF}$, $R_S = 50\ \Omega$		55		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	$f_C = 5\text{ MHz}$, $V_O = 2\text{ V p-p}$, $R_L = 1\text{ k}\Omega$		–60		dBc
Voltage Noise (RTO) ¹	$f = 10\text{ kHz}$		67		nV/ $\sqrt{\text{Hz}}$
Crosstalk, Output to Output	$f = 5\text{ MHz}$, $V_O = 2\text{ V p-p}$, $R_L = 1\text{ k}\Omega$		–80		dB
Differential Gain Error	NTSC $R_L = 1\text{ k}\Omega$		0.02		%
Differential Phase Error	NTSC $R_L = 1\text{ k}\Omega$		0.02		Degrees
DC PERFORMANCE					
RTO Offset Voltage ²	$V_{\text{IN}} = 0\text{ V}$ T_{MIN} to T_{MAX}		0.5	5.5	mV
RTO Offset Drift			10	6	mV/ $^\circ\text{C}$
+Input Bias Current			0.6	1.6	μA
Closed-Loop Gain Error ³	$R_L = 10\text{ k}\Omega$, $-2.67 < V_O < +2.67$ T_{MIN} to T_{MAX}		–0.02	0.05	%
Gain Matching	Channel-to-Channel, $R_L = 10\text{ k}\Omega$			0.05	%
				0.03	%
INPUT CHARACTERISTICS					
+Input Resistance			170		k Ω
+Input Capacitance			2.5		pF
OUTPUT CHARACTERISTICS					
Output Voltage Swing	$R_L = 10\text{ k}\Omega$, $V_{\text{CC}} - V_{\text{OH}}$, $V_{\text{EE}} + V_{\text{OL}}$		0.2	0.25	V
Short Circuit Output Current			175		mA
POWER SUPPLY					
Operating Range ⁴				13	V
Quiescent Current/Amp			3.2	3.4	mA/Amp
Power Supply Rejection Ratio (RTO)	$+V_S = 5.5\text{ V to }6.5\text{ V}$, $-V_S = -6\text{ V}$	48	60		dB
	$-V_S = -5.5\text{ V to }-6.5\text{ V}$, $+V_S = 6\text{ V}$	48	65		dB
OPERATING TEMPERATURE RANGE		0		+70	$^\circ\text{C}$

NOTES

¹Includes gain resistor thermal noise.

²RTO offset includes effects of input voltage offset, input current, and input offset current.

³Measured in the inverting mode.

⁴Observe Absolute Maximum Ratings.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage $V_{CC}-V_{EE}$ 14.0 V
 Internal Power Dissipation²

Small Outline Package (R) 0.9 W
 +Input Voltage $V_{CC}-V_{IN+}$ < 12 V
 -Input Voltage < $V_{EE} + 12$ V
 > $V_{EE} - 12$ V

Output Short Circuit Duration

..... Observe Power Derating Curves
 Storage Temperature Range -65°C to +125°C
 Operating Temperature Range (A Grade) 0°C to +70°C
 Lead Temperature Range (Soldering 10 sec) +300°C

NOTES

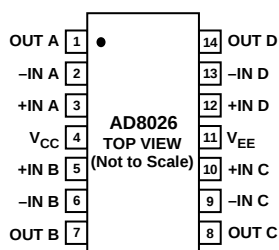
¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Specification is for device in free air:

14-Lead SOIC Package: $\theta_{JA} = 120^{\circ}\text{C}/\text{W}$, where $P_D = (T_J - T_A)/\theta_{JA}$.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8026AR	0°C to +70°C	14-Lead Plastic SOIC	SO-14
AD8026AR-REEL	0°C to +70°C	REEL SOIC	SO-14
AD8026AR-REEL7	0°C to +70°C	REEL 7 SOIC	SO-14

PIN CONFIGURATION**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8026 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8026 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8026 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

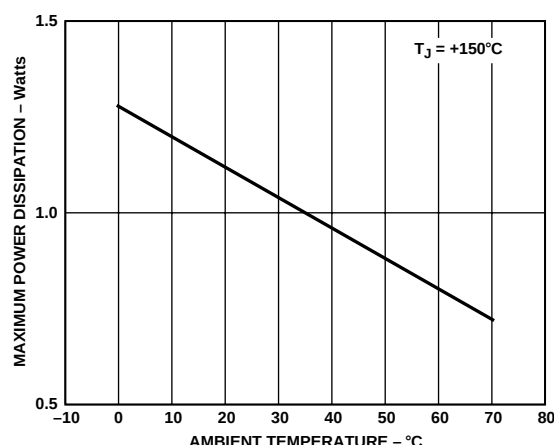


Figure 2. Maximum Power Dissipation vs. Temperature



AD8026—Typical Performance Characteristics

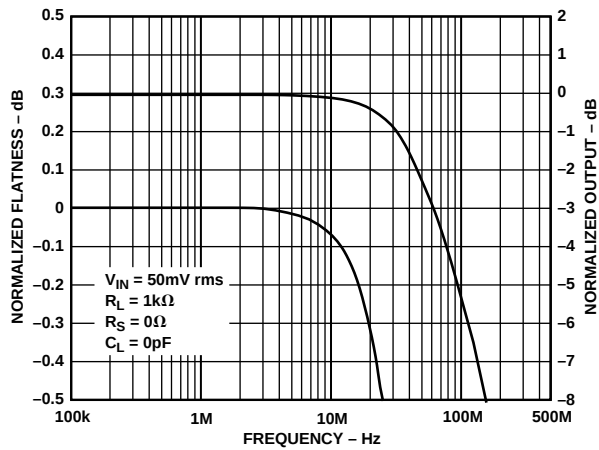


Figure 3. Small Signal Bandwidth and 0.1 dB Flatness

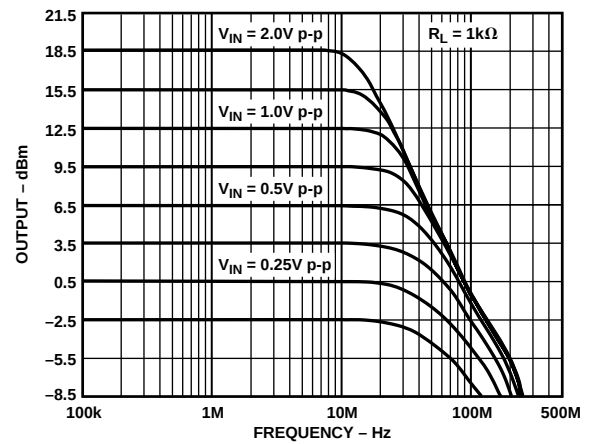


Figure 6. Large Signal Bandwidth

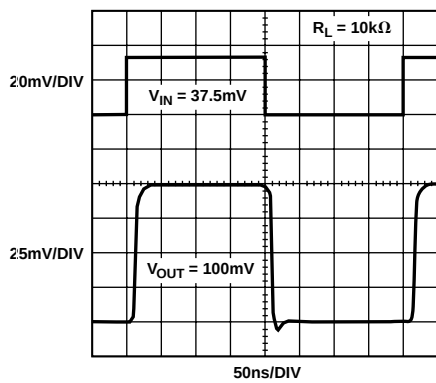


Figure 4. 100 mV Step Response

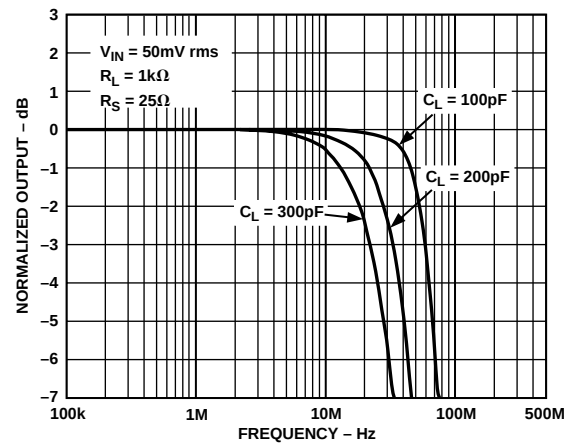


Figure 7. Cap Load vs. Frequency

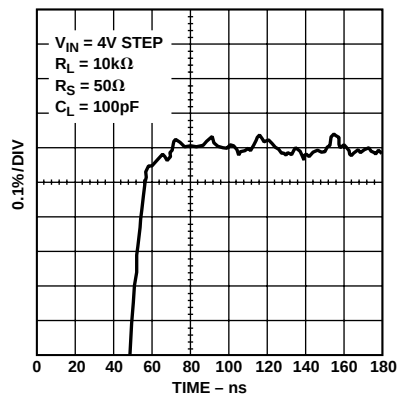


Figure 5. Short-Term Settling Time

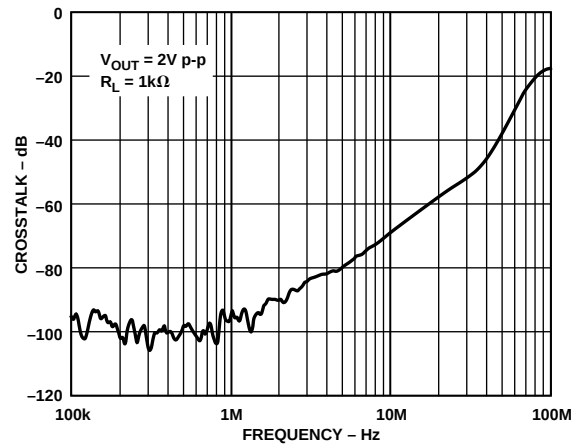


Figure 8. Crosstalk (Output-to-Output) vs. Frequency

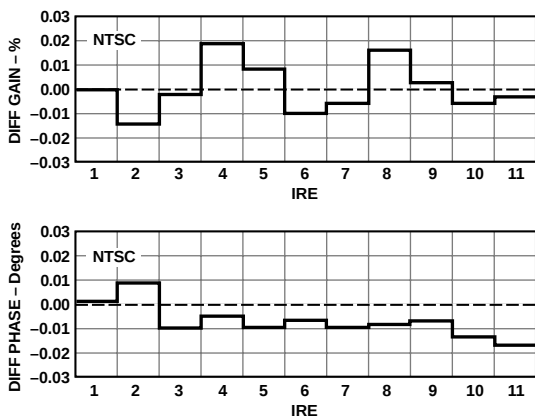


Figure 9. Differential Gain and Differential Phase

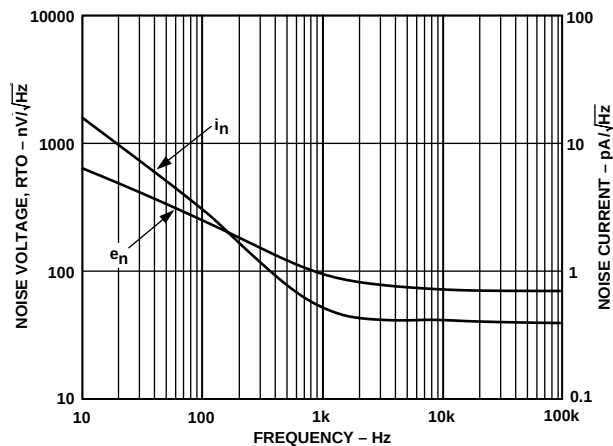


Figure 12. Noise (RTO) vs. Frequency

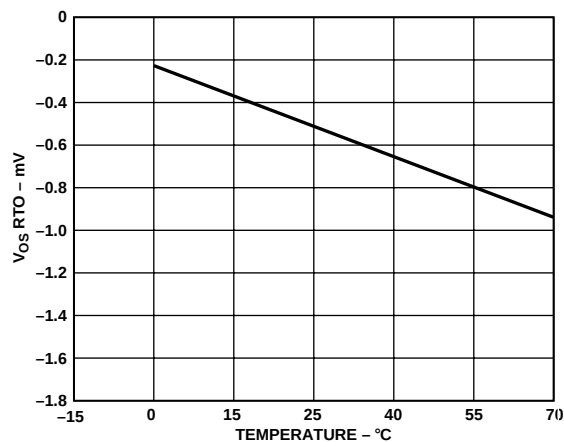


Figure 10. V_{OS} RTO vs. Temperature

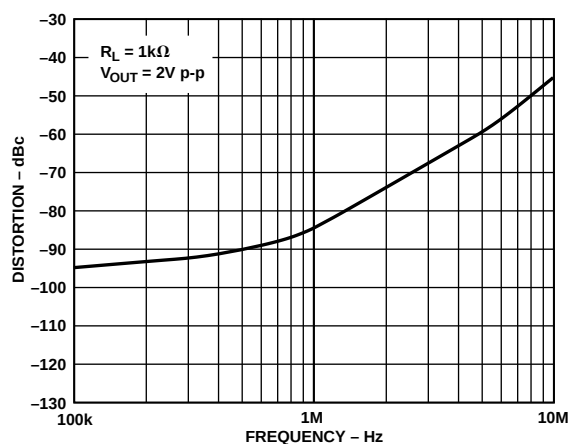


Figure 13. Total Harmonic Distortion

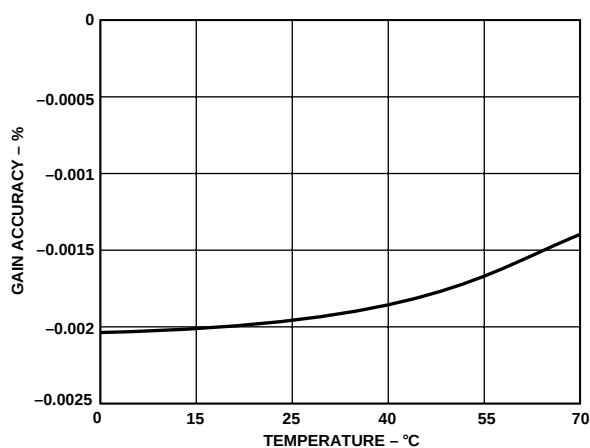


Figure 11. Gain Accuracy vs. Temperature

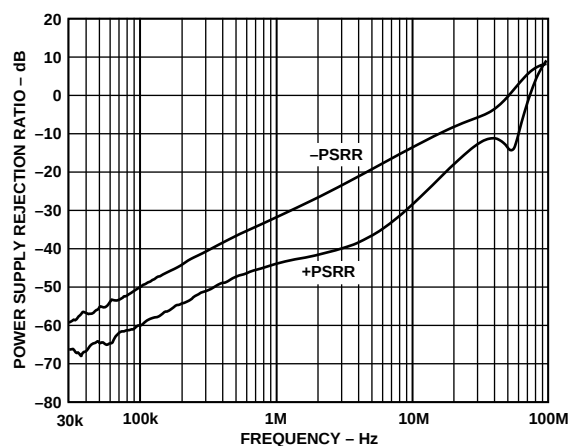


Figure 14. PSRR vs. Frequency

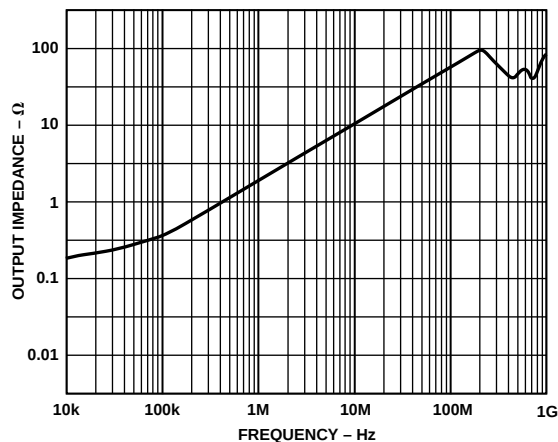


Figure 15. Output Impedance vs. Frequency

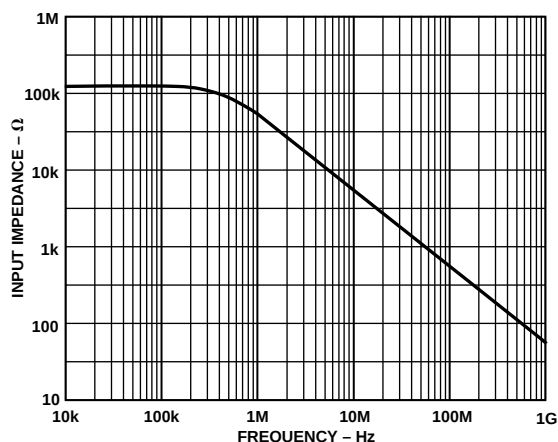


Figure 16. Input Impedance vs. Frequency

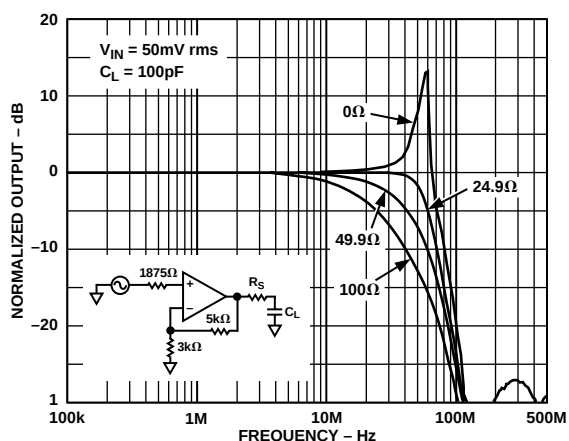


Figure 17. Bandwidth and Flatness vs. Series Resistance into 100 pF

THEORY OF OPERATION

The AD8026, a quad voltage feedback amplifier with rail-to-rail output swing, is internally configured for a gain of either $-5/3$ or $+8/3$. The gain-setting resistors are laser trimmed for precise control of their ratio. In addition, the amplifier's frequency response has been adjusted to compensate for the parasitic capacitances associated with the gain resistors and with the amplifier's inverting input. The result is an amplifier with very tight control of closed-loop gain and settling time.

The amplifier's input stage will operate with voltages from about -0.2 V below the negative supply voltage to within about 1 V of the positive supply. Exceeding these values will not cause phase reversal at the output; however, the input ESD protection devices will begin to conduct if the input voltages exceed the supply rails by greater than 0.5 V. The gain resistors that connect to Pins 2, 6, 9, and 13 are protected from ESD in such a way that the voltages applied to these pins may exceed the negative supply by as much as -7 V.

The rail-to-rail output range of the AD8026 is provided by a complementary common-emitter output stage. The chosen circuit topology allows the outputs to source and sink 50 mA of output current and, with the use of an external series resistor, to achieve rapid settling time while driving capacitive loads within 0.5 V of the supply rails.

Output Referred Offset Voltage

The output referred offset voltage for a voltage feedback amplifier can be estimated with the following equation:

$$V_{OOS} = V_{IOS} \times \left(1 + R_F/R_G\right) + I_{OS} \times \left(R_F \parallel R_G\right) + I_B \times \left(R_P - \left(R_F \parallel R_G\right)\right)$$

where:

- V_{OOS} = output referred offset voltage,
- V_{IOS} = input referred offset voltage,
- I_{OS} = difference of the two input currents,
- I_B = average of the two input currents,
- R_P = total resistance in series with positive input,
- $R_F = 5$ k Ω , $R_G = 3$ k Ω for this part.

This equation leads to the well known conclusion that, for a voltage feedback amplifier to maintain minimum output offset voltage, the value of R_P should be selected to match the parallel combination of R_F and R_G . It should be noted that the AD8026 was designed for an assumed source impedance, of 500 Ω driving the +Input. Therefore, the value of R_P included on the chip is 500 Ω less than the ideal value for minimum output offset. Additional resistance may be added externally, in series with the +Input, if the part is to be driven by a lower impedance source.

APPLICATIONS

The AD8026 is designed with on-chip resistors for each op amp to provide accurate fixed gain and low output-referred offset voltages. This can result in significant cost and board-space savings for systems that can take advantage of the AD8026 specifications.

The part is actually trimmed in three steps. First, the supply current of the part is trimmed. Then the gain is accurately trimmed to specification. This trim adjusts the values of either the gain or feedback resistor for a ratio of 5 to 3. The final trim is for the offset voltage. For this trim, the $-$ Input is connected to ground and the $+$ Input is connected to ground via 500 Ω , while internal offset resistors are trimmed.

In a system application, the part is designed assuming that each $-$ Input will be driven from a low impedance source, while each $+$ Input will be driven by a current-output DAC with a $500\ \Omega$ termination resistor. Thus, to first order, each on-chip series input resistor to each $+$ Input is $500\ \Omega$ less than the parallel combination of the gain-setting resistors. The offset-inducing effect of the bias currents is minimized by this scheme.

Figure 18 shows how to drive the AD8026 with a fixed positive gain of $8/3$ from a current output DAC. The gain and offset errors are minimized by using a $500\ \Omega$ resistor (R_I) to convert the DAC output current into a voltage. The gain resistor (R_G) should be directly connected to ground, or driven from a low output impedance source to ensure minimum offset and maximum gain accuracy.

If the $+$ Input of any of the op amps is driven from a voltage source, the low offset voltage of the AD8026 can be maintained by adding a series resistance of $500\ \Omega$ between the source and the $+$ Input to the AD8026. This is illustrated in Figure 19. If the $-$ Input is to be driven, such as when creating an offset voltage, then a low source impedance should be provided in order to maintain both gain and offset accuracy.

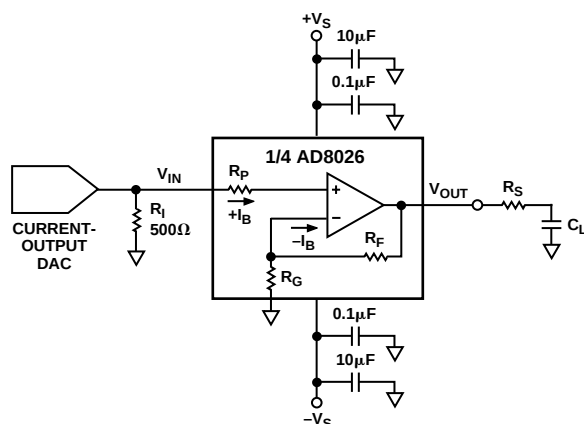


Figure 18. Low Offset and High Gain Accuracy Circuit for Driving the AD8026 from a Current Output DAC

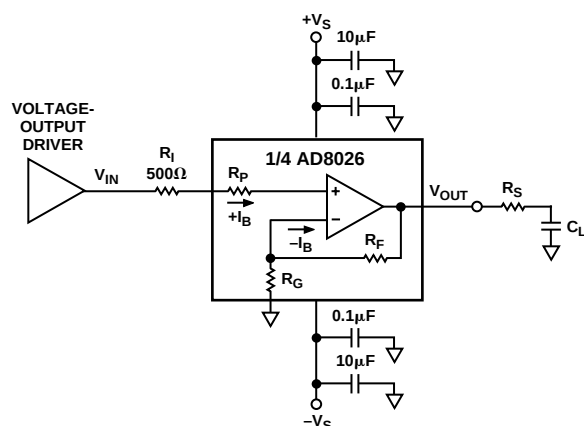


Figure 19. Low Offset and High Gain Accuracy Circuit for Driving the AD8026 from a Voltage Source

QUAD AMPLIFIER CHARACTERIZATION BOARD

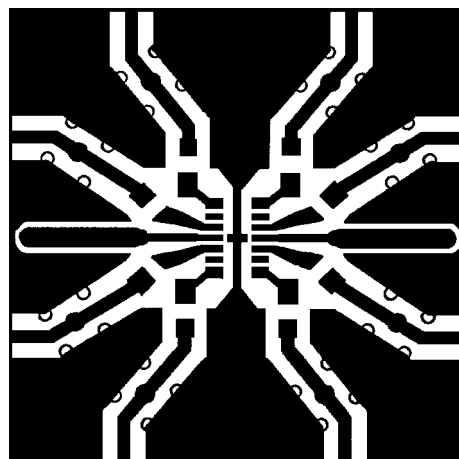


Figure 20. Component Side

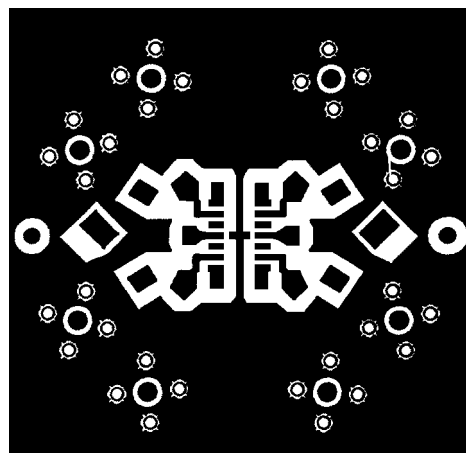


Figure 21. Solder Side

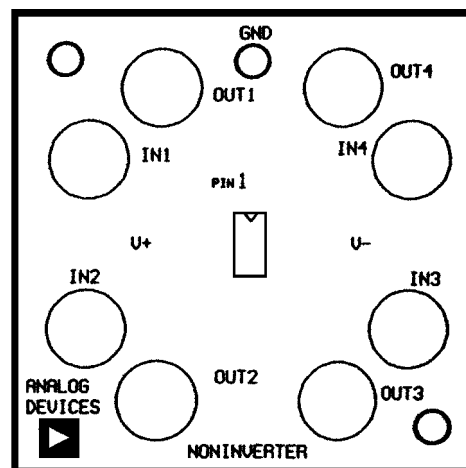
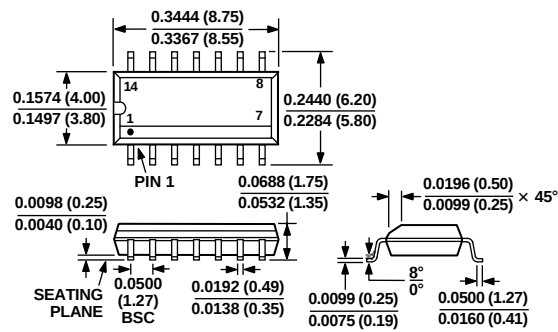


Figure 22. Silkscreen

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

14-Lead SOIC
(SO-14)



C3327-8-4/98

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