High Common-Mode Voltage, Single-Supply Difference Amplifier

AD8200

FEATURES

High Common-Mode Voltage Range –2 V to +24 V at a 5 V Supply Voltage
Operating Temperature Range
Die: –40°C to +150°C
8-Lead SOIC: –40°C to +125°C
Supply Voltage Range: 4.7 V to 12 V
Low-Pass Filter (One Pole or Two Pole)

EXCELLENT AC AND DC PERFORMANCE

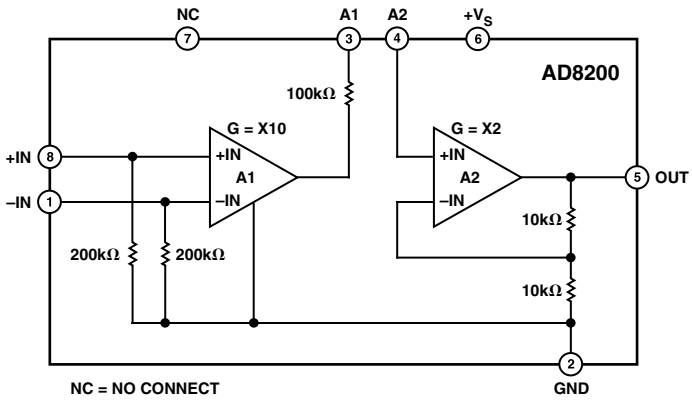
±6 μV/°C Typ Offset Drift
±10 ppm/°C Typ Gain Drift
80 dB CMRR Min DC to 10 kHz

PLATFORMS

Transmission Control
Diesel Injection Control
Engine Management
Adaptive Suspension Control
Vehicle Dynamics Control

FUNCTIONAL BLOCK DIAGRAM

SOIC (R) Package
DIE Form



GENERAL DESCRIPTION

The AD8200 is a single-supply difference amplifier for amplifying and low-pass filtering small differential voltages in the presence of a large common-mode voltage. The input CMV range extends from –2 V to +24 V at a typical supply voltage of 5 V.

The AD8200 is offered in die and packaged form. Both package options are specified over wide temperature ranges, making the AD8200 well suited for use in many automotive platforms. The SOIC package is specified over a temperature range of –40°C to +125°C. The die is specified from –40°C to +150°C.

Automotive platforms demand precision components for better system control. The AD8200 provides excellent ac and dc performance that keeps errors to a minimum in the user's system. Typical offset and gain drift in the SOIC package are 6 μV/°C and 10 ppm/°C, respectively. The device also delivers a minimum CMRR of 80 dB from dc to 10 kHz.

The AD8200 features an externally accessible 100 kΩ resistor at the output of the preamp A1, which can be used for low-pass filter applications and for establishing gains other than 20.

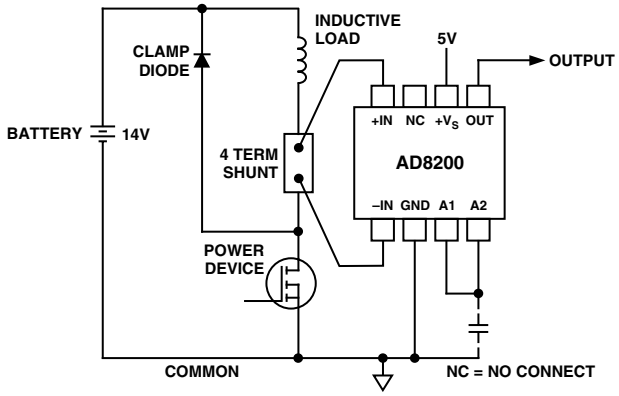


Figure 1. High-Line Current Sensor

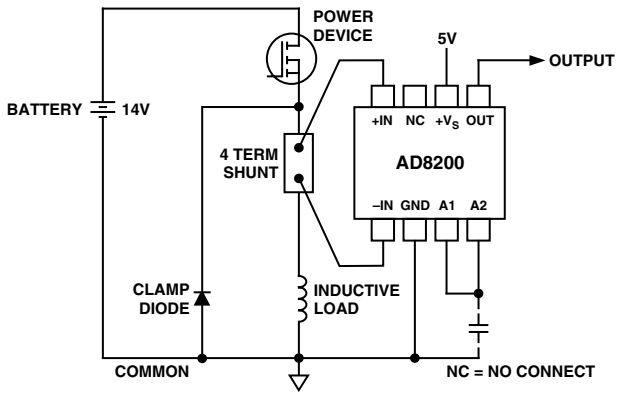


Figure 2. Low-Line Current Sensor

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD8200–SPECIFICATIONS

SINGLE SUPPLY (T_A = 25°C, V_S = 5 V, V_{CM} = 0 V, R_L = 10 kΩ, Pin 5 to ground, unless otherwise noted.)

Parameter	Condition	AD8200 SOIC Min	AD8200 SOIC Typ	AD8200 SOIC Max	AD8200 DIE Min	AD8200 DIE Typ	AD8200 DIE Max	Unit
SYSTEM GAIN								
Initial		20			20			
Error	$V_O \geq 0.1$ V dc	–1		+1	–1		+1	%
vs. Temperature			10	20		25	30	ppm/°C
OFFSET VOLTAGE								
Offset Voltage (RTI)	V_{CM} = 0.15 V	–1		+1	–1		+1	mV
vs. Temperature			±6	±15		±12	±25	µV/°C
INPUT								
Input Impedance								
Differential		320	400	480	320	400	480	kΩ
Common-Mode		160	200	240	160	200	240	kΩ
CMV	Continuous	–2		+24	–2		+24	V
Common-Mode Rejection[1]	V_{CM} = 10 V							
	f = 1 kHz	80			80			dB
	f = 10 kHz[2]	80			80			dB
PREAMPLIFIER								
Gain		10			10			
Gain Error		–1		+1	–1		+1	%
Output Voltage Range		0.02		4.8	0.02		4.8	V
Output Resistance		97	100	103	97	100	103	kΩ
OUTPUT BUFFER								
Gain			2			2		
Gain Error		–1		+1	–1		+1	%
Output Voltage Range		0.02		4.8	0.02		4.8	V
Output Resistance			2			2		Ω
DYNAMIC RESPONSE								
3 dB Bandwidth		30	50		30	50		kHz
Slew Rate			0.22			0.22		V/µs
NOISE								
0.1 Hz to 10 Hz			10			10		µV p-p
Spectral Density, 1 kHz, RTI			300			300		nV/$\sqrt{\text{Hz}}$
POWER SUPPLY								
Operating Range		4.7		12	4.7		12	V
Quiescent Current vs. Temperature	V_O = 0.1 V dc		0.25	1		0.25	1	mA
PSRR	V_S = 4.7 V to 12 V	75	80		75	80		dB
TEMPERATURE RANGE								
For Specified Performance		–40		+125	–40		+150	°C

NOTES

[1]Source Imbalance < 2 Ω.

[2]The AD8200 preamplifier exceeds 80 dB CMRR at 10 kHz. However, since the signal is available only by way of a 100 kΩ resistor, even the small amounts of pin-to-pin capacitance between Pins 1, 8 and 3, 4 may couple an input common-mode signal larger than the greatly attenuated preamplifier output. The effect of pin-to-pin coupling may be neglected in all applications using filter capacitors at Node 3.

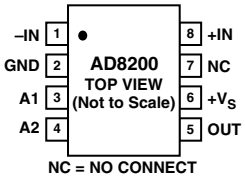
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 12.5 V
Transient Input Voltage (300 ms) . . . . . 44 V
Continuous Input Voltage . . . . . 35 V
Reversed Supply Voltage Protection . . . . . 0.3 V
Operating Temperature . . . . . (Die) –40°C to +150°C
. . . . . (SOIC) –40°C to +125°C
Storage Temperature . . . . . –65°C to +150°C
Output Short Circuit Duration . . . . . Indefinite
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

*Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



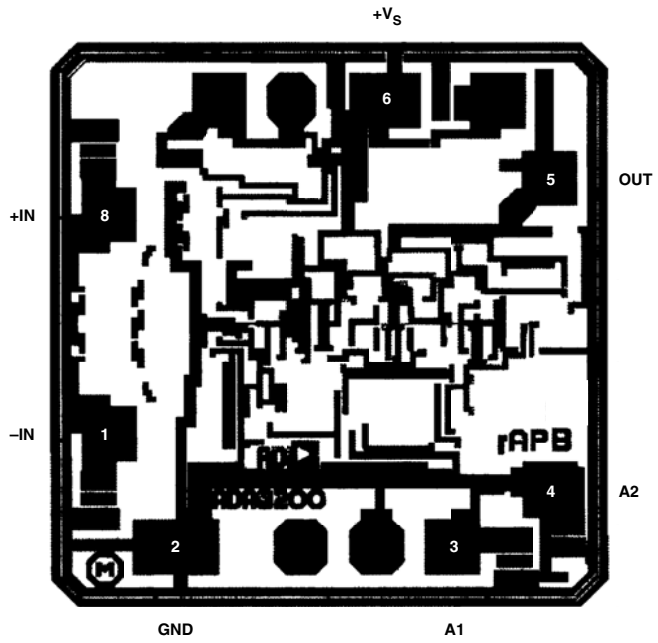
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8200YR	–40°C to +125°C	Plastic SOIC	SO-8
AD8200YR-Reel	–40°C to +125°C	Plastic SOIC	SO-8
AD8200YR-Reel-7	–40°C to +125°C	Plastic SOIC	SO-8
AD8200YCHIPS	–40°C to +150°C	N/A	DIE Form
AD8200YCSURF	–40°C to +150°C	N/A	DIE Form

CAUTION

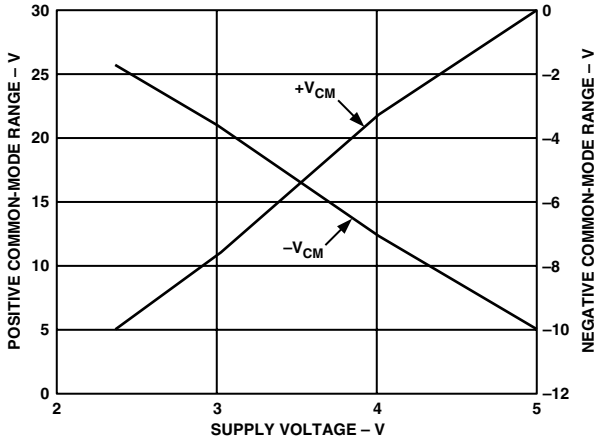
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8200 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

METALLIZATION PHOTOGRAPH

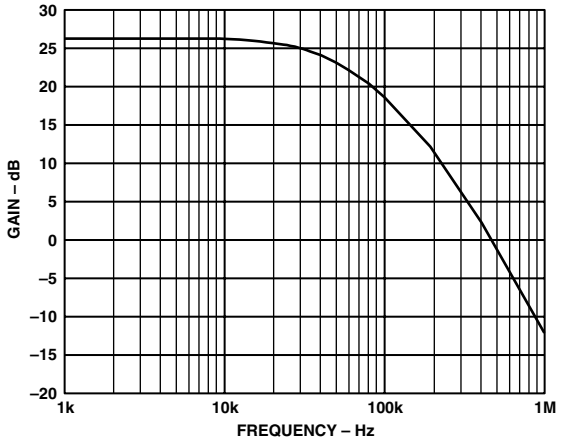


AD8200–Typical Performance Characteristics

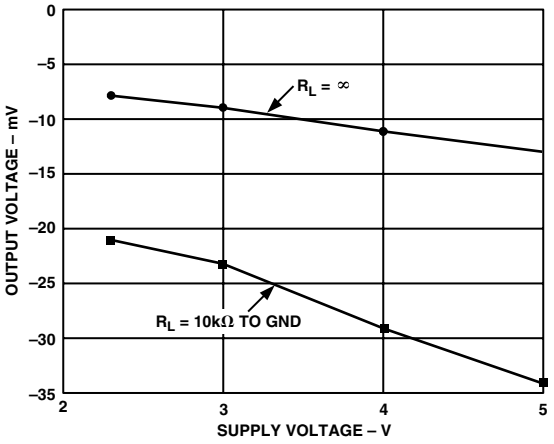
(T_A = 25°C, V_S = 5 V, V_{CM} = 0 V, R_L = 10 kΩ, unless otherwise noted.)



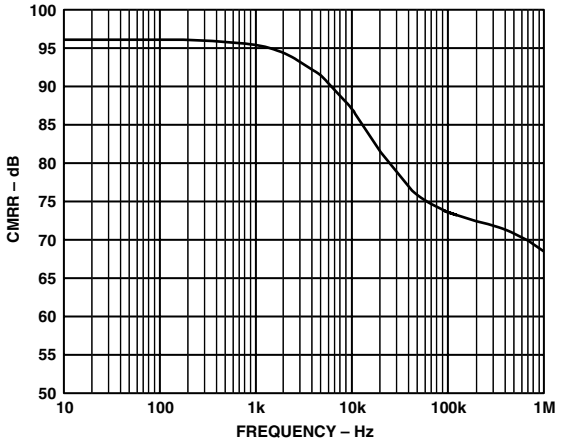
TPC 1. Input Common-Mode Range vs. Supply



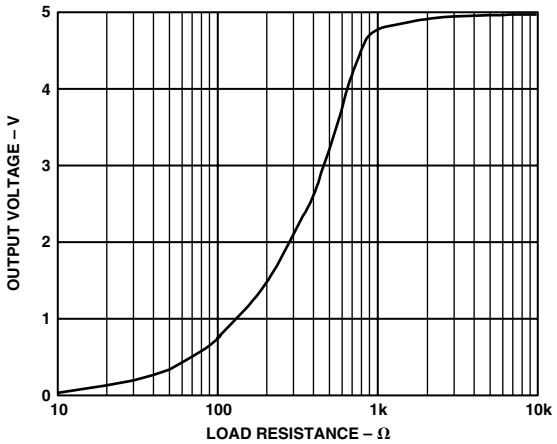
TPC 4. Gain vs. Frequency



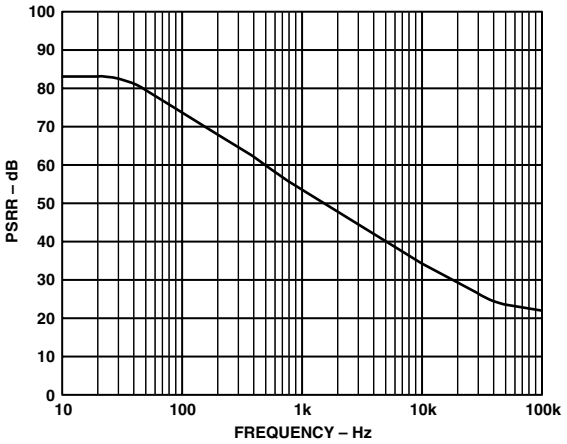
TPC 2. Output Voltage – V_S vs. Supply



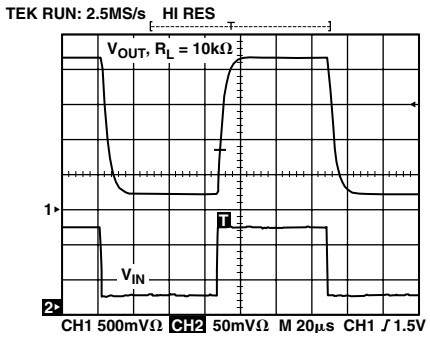
TPC 5. Common-Mode Rejection vs. Frequency



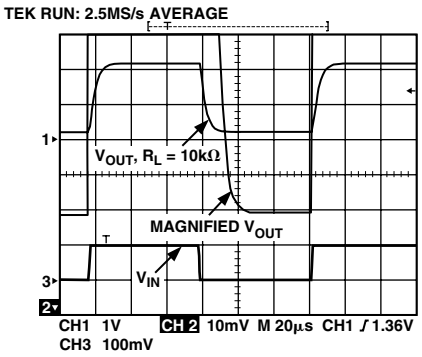
TPC 3. Output Voltage Swing vs. Load Resistance



TPC 6. Power Supply Rejection vs. Frequency



TPC 7. Pulse Response



TPC 8. Settling Time

THEORY OF OPERATION

The AD8200 consists of a preamp and buffer arranged as shown in Figure 3. Like-named resistors have equal values.

The preamp incorporates a dynamic bridge (subtractor) circuit. Identical networks (within the shaded areas), consisting of R_A, R_B, R_C, and R_G, attenuate input signals applied to Pins 1 and 8. Note that when equal amplitude signals are asserted at inputs 1 and 8, and the output of A1 is equal to the common potential (i.e., zero), the two attenuators form a balanced-bridge network. When the bridge is balanced, the differential input voltage at A1 and thus its output will be zero.

Any common-mode voltage applied to both inputs will keep the bridge balanced and the A1 output at zero. Because the resistor networks are carefully matched, the common-mode signal rejection approaches this ideal state.

However, if the signals applied to the inputs differ, the result is a difference at the input to A1. A1 responds by adjusting its output to drive R_B, by way of R_G, to adjust the voltage at its inverting input until it matches the voltage at its noninverting input.

By attenuating voltages at Pins 1 and 8, the amplifier inputs are held within the power supply range, even if Pin 1 and Pin 8 input levels exceed the supply, or fall below common (ground.) The input network also attenuates normal (differential) mode voltages. R_C and R_G form an attenuator that scales A1 feedback, forcing large output signals to balance relatively small differential inputs. The resistor ratios establish the preamp gain at 10.

Because the differential input signal is attenuated, and then amplified to yield an overall gain of 10, the amplifier A1 operates at a higher noise gain, multiplying deficiencies such as input offset voltage and noise with respect to Pins 1 and 8.

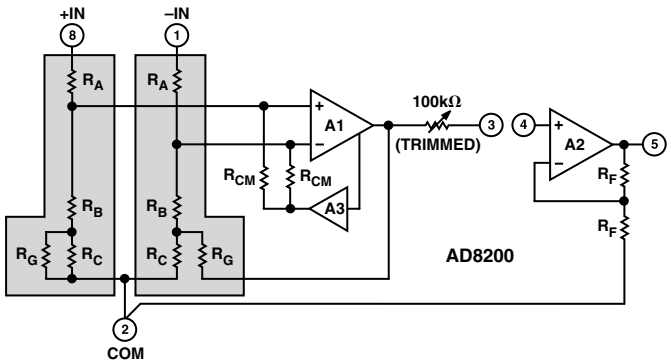


Figure 3. Simplified Schematic

To minimize these errors while extending the common-mode range, a dedicated feedback loop is employed to reduce the range of common-mode voltage applied to A1, for a given overall range at the inputs. By offsetting the range of voltage applied to the compensator, the input common-mode range is also offset to include voltages more negative than the power supply. Amplifier A3 detects the common-mode signal applied to A1 and adjusts the voltage on the matched R_{CM} resistors to reduce the common-mode voltage range at the A1 inputs. By adjusting the common voltage of these resistors, the common-mode input range is extended while, at the same time, the normal mode signal attenuation is reduced, leading to better performance referred to input.

The output of the dynamic bridge taken from A1 is connected to Pin 3 by way of a 100 kΩ series resistor, provided for low-pass filtering and gain adjustment. The resistors in the input networks of the preamp and the buffer feedback resistors are ratio-trimmed for high accuracy.

The output of the preamp drives a gain-of-two buffer-amplifier A2, implemented with carefully matched feedback resistors R_F.

The two-stage system architecture of the AD8200 enables the user to incorporate a low-pass filter prior to the output buffer. By separating the gain into two stages, a full-scale rail-to-rail signal from the preamp can be filtered at Pin 3, and a half-scale signal resulting from filtering can be restored to full scale by the output buffer amp. The source resistance seen by the inverting input of A2 is approximately 100 kΩ, to minimize the effects of A2's input bias current. However, this current is quite small and errors resulting from applications that mismatch the resistance are correspondingly small.

APPLICATIONS

The AD8200 difference amplifier is intended for applications where it is required to extract a small differential signal in the presence of large common-mode voltages. The input resistance is nominally 200 kΩ, and the device can tolerate common-mode voltages higher than the supply voltage and lower than ground.

The open collector output stage will source current to within 20 mV of ground.

CURRENT SENSING

High Line, High Current Sensing

Basic automotive applications making use of the large common-mode range are shown in Figures 1 and 2. The capability of the device to operate as an amplifier in primary battery supply circuits is shown in Figure 1; Figure 2 illustrates the ability of the device to withstand voltages below system ground.

Low Current Sensing

The AD8200 can also be used in low current sensing applications, such as a 4–20 mA current loop shown in Figure 4. In such applications, the relatively large shunt resistor can degrade the common-mode rejection. Adding a resistor of equal value in the low impedance side of the input corrects for this error.

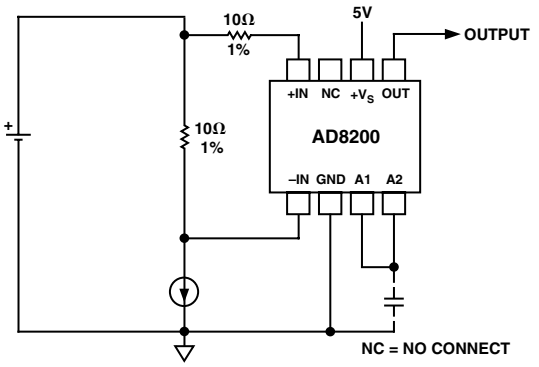


Figure 4. 4–20 mA Current Loop Receiver

GAIN ADJUSTMENT

The default gain of the preamplifier and buffer are ×10 and ×2, respectively, resulting in a composite gain of ×20. With the addition of external resistor(s) or trimmer(s), the gain may be lowered, raised, or finely calibrated.

Gains Less than 20

See Figure 5. Since the preamplifier has an output resistance of 100 kΩ, an external resistor connected from Pins 3 and 4 to GND will decrease the gain by a factor $R_{EXT}/(100\ k\Omega + R_{EXT})$.

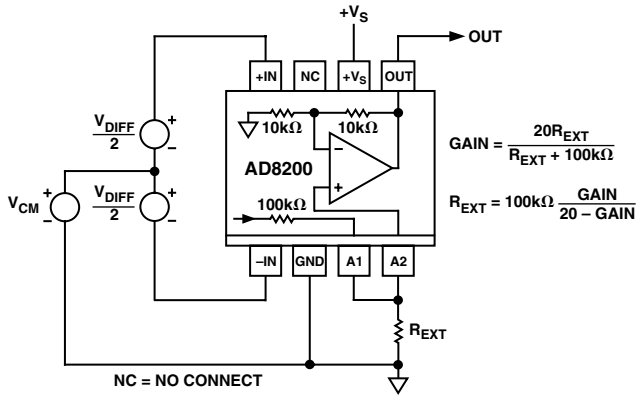


Figure 5. Adjusting for Gains Less than 20

The overall bandwidth is unaffected by changes in gain using this method, although there may be a small offset voltage due to the imbalance in source resistances at the input to the buffer. In many cases this can be ignored, but if desired, can be nulled by inserting a resistor equal to 100 kΩ minus the parallel sum of R_{EXT} and 100 kΩ, in series with Pin 4. For example, with R_{EXT} = 100 kΩ (yielding a composite gain of ×10), the optional offset nulling resistor is 50 kΩ (see Figure 11.)

Gains Greater than 20

Connecting a resistor from the output of the buffer amplifier to its noninverting input, as shown in Figure 6, will increase the gain. The gain is now multiplied by the factor $R_{EXT}/(R_{EXT} - 100\ k\Omega)$; for example, it is doubled for R_{EXT} = 200 kΩ. Overall gains as high as 50 are achievable in this way. Note that the accuracy of the gain becomes critically dependent on resistor value at high gains. Also, the effective input offset voltage at Pins 1 and 8 (about six times the actual offset of A1) limits the part's use in very high gain, dc-coupled applications.

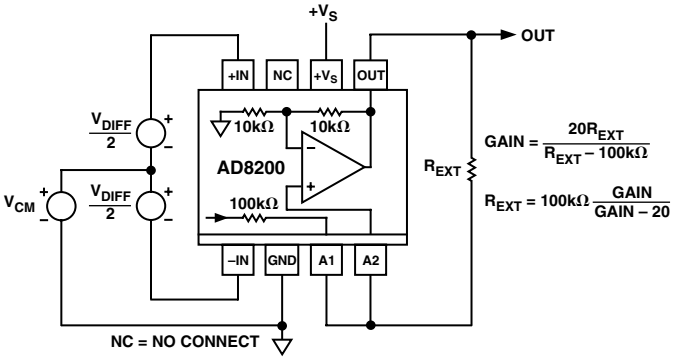


Figure 6. Adjusting for Gains Greater than 20

GAIN TRIM

Figure 7 shows a method for incremental gain trimming using a trimpot and external resistor R_{EXT}.

The following approximation is useful for small gain ranges:

$$\Delta G \approx (10\ M\Omega \div R_{EXT})\ \%$$

Thus, the adjustment range would be ±2% for R_{EXT} = 5 MΩ; ±10% for R_{EXT} = 1 MΩ, and so on.

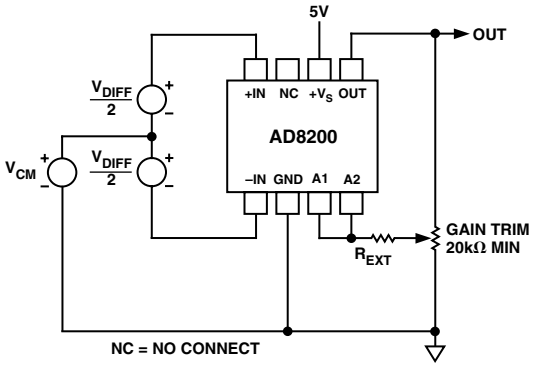


Figure 7. Incremental Gain Trim

Internal Signal Overload Considerations

When configuring gain for values other than 20, the maximum input voltage with respect to the supply voltage and ground must be considered, since either the preamplifier or the output buffer will reach its full-scale output (approximately $V_S - 0.2\ V$) with large differential input voltages. The input of the AD8200 is limited to $(V_S - 0.2) \div 10$, for overall gains ≤10, since the preamplifier, with its fixed gain of ×10, reaches its full-scale output before the output buffer. For gains greater than 10, the swing at the buffer output reaches its full scale first and limits the AD8200 input to $(V_S - 0.2) \div G$, where G is the overall gain.

LOW-PASS FILTERING

In many transducer applications it is necessary to filter the signal to remove spurious high frequency components, including noise, or to extract the mean value of a fluctuating signal with a peak-to-average ratio (PAR) greater than unity. For example, a full-wave rectified sinusoid has a PAR of 1.57, a raised cosine has a PAR of 2, and a half-wave sinusoid has a PAR of 3.14. Signals having large spikes may have PARs of 10 or more.

When implementing a filter, the PAR should be considered so the output of the AD8200 preamplifier (A1) does not clip before A2, since this nonlinearity would be averaged and appear as an error at the output. To avoid this error, both amplifiers should be made to clip at the same time. This condition is achieved when the PAR is no greater than the gain of the second amplifier (2 for the default configuration). For example, if a PAR of 5 is expected, the gain of A2 should be increased to 5.

Low-pass filters can be implemented in several ways using the features provided by the AD8200. In the simplest case, a single-pole filter (20 dB/decade) is formed when the output of A1 is connected to the input of A2 via the internal 100 kΩ resistor by strapping Pins 3 and 4 and a capacitor added from this node to ground, as shown in Figure 8. If a resistor is added across the capacitor to lower the gain, the corner frequency will increase; it should be calculated using the parallel sum of the resistor and 100 kΩ.

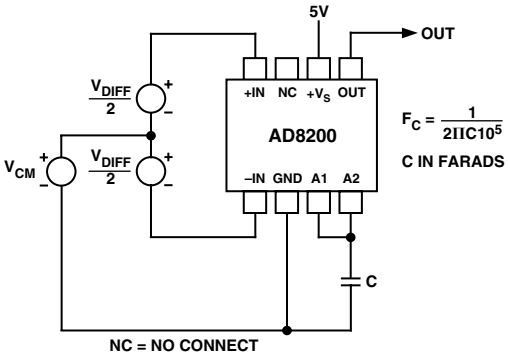


Figure 8. A Single-Pole, Low-Pass Filter Using the Internal 100 kΩ Resistor

If the gain is raised using a resistor, as shown in Figure 8, the corner frequency is lowered by the same factor as the gain is raised. Thus, using a resistor of 200 kΩ (for which the gain would be doubled) the corner frequency is now 0.796 Hz-μF, (0.039 μF for a 20 Hz corner frequency.)

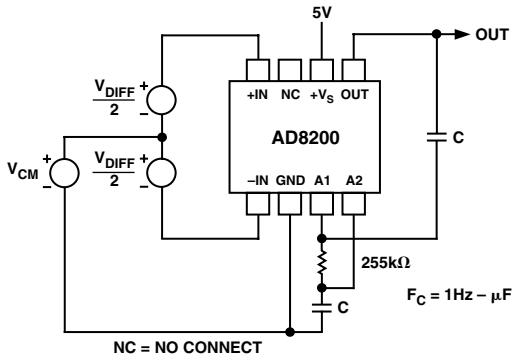


Figure 9. 2-Pole Low-Pass Filter

A 2-pole filter (with a roll-off of 40 dB/decade) can be implemented using the connections shown in Figure 9. This is a Sallen-Key form based on a ×2 amplifier. It is useful to remember that a 2-pole filter with a corner frequency f_2 and a 1-pole filter with a corner at f_1 have the same attenuation at the frequency (f_2^2/f_1). The attenuation at that frequency is 40 Log (f_2/f_1). This is illustrated in Figure 10. Using the standard resistor value shown and equal capacitors (Figure 9), the corner frequency is conveniently scaled at 1 Hz-μF (0.05 μF for a 20 Hz corner). A maximally flat response occurs when the resistor is lowered to 196 kΩ and the scaling is then 1.145 Hz-μF. The output offset is raised by about 5 mV (equivalent to 250 μV at the input pins).

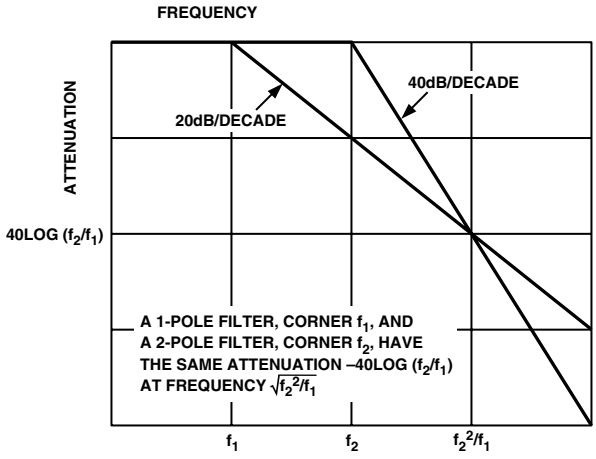


Figure 10. Comparative Responses of 1- and 2-Pole Low-Pass Filters

HIGH LINE CURRENT SENSING WITH LPF AND GAIN ADJUSTMENT

Figure 11 is another refinement of Figure 1, including gain adjustment and low-pass filtering.

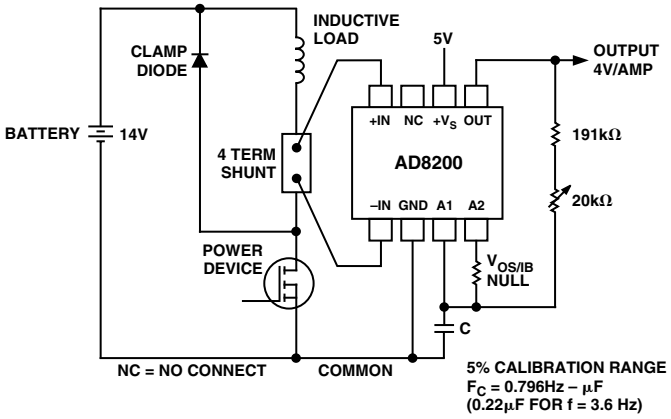


Figure 11. High-Line Current Sensor Interface. Gain = ×40, Single-Pole, Low-Pass Filter

A power device that is either 'ON' or 'OFF' controls the current in the load. The average current is proportional to the duty cycle of the input pulse, and is sensed by a small value resistor. The average differential voltage across the shunt is typically 100 mV, although its peak value will be higher by an amount that depends on the inductance of the load and the control frequency. The common-mode voltage, on the other hand, extends from roughly 1 V above ground, when the switch is 'ON,' to about 1.5 V above the battery voltage, when the device is 'OFF,' and the clamp diode conducts. If the maximum battery voltage spikes up to 20 V, the common-mode voltage at the input can be as high as 21.5 V.

To produce a full-scale output of 4 V, a gain ×40 is used, adjustable by ±5% to absorb the tolerance in the shunt. There is sufficient headroom to allow 10% overrange (to 4.4 V). The roughly triangular voltage across the sense resistor is averaged by a single-pole, low-pass filter, here set with a corner frequency = 3.6 Hz, which provides about 30 dB of attenuation at 100 Hz. A higher rate of attenuation can be obtained using a two-pole filter having f_C = 20 Hz, as shown in Figure 12. Although this circuit uses two separate capacitors, the total capacitance is less than half that needed for the single-pole filter.

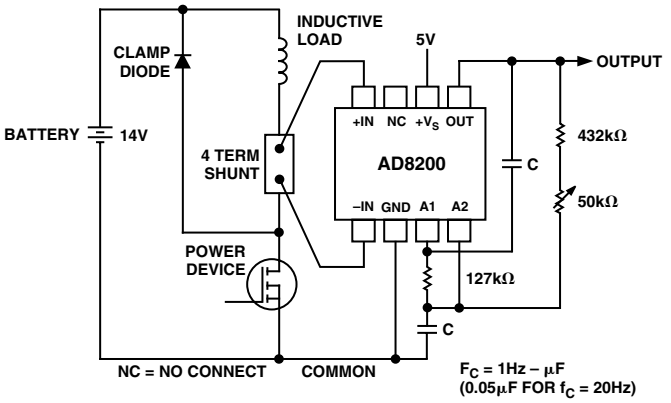


Figure 12. Illustration of 2-Pole Low-Pass Filtering

DRIVING CHARGE REDISTRIBUTION A/D CONVERTERS

When driving CMOS ADCs, such as those embedded in popular microcontrollers, the charge injection (ΔQ) can cause a significant deflection in the output voltage of the AD8200. Though generally of short duration, this deflection may persist until after the sample period of the ADC has expired, due to the relatively high open-loop output impedance of the AD8200. Including an R-C network in the output can significantly reduce the effect. The capacitor helps to absorb the transient charge, effectively lowering the high frequency output impedance of the AD8200. For these applications, the output signal should be taken from the midpoint of the R_{LAG}–C_{LAG} combination as shown in Figure 13.

Since the perturbations from the analog-to-digital converter are small, the output impedance of the AD8200 will appear to be low. The transient response will, therefore, have a time constant governed by the product of the two LAG components, $C_{LAG} \times R_{LAG}$. For the values shown in Figure 13, this time constant is programmed at approximately 10 μs. Therefore, if samples are taken at several tens of microseconds or more, there will be negligible charge "stack-up."

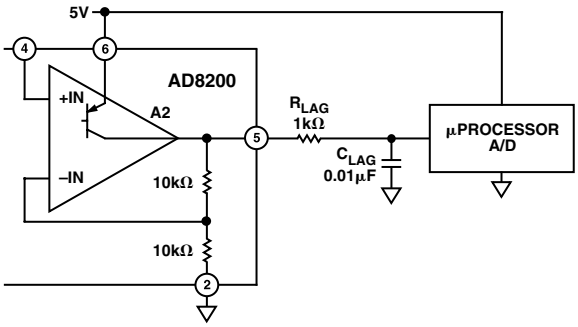
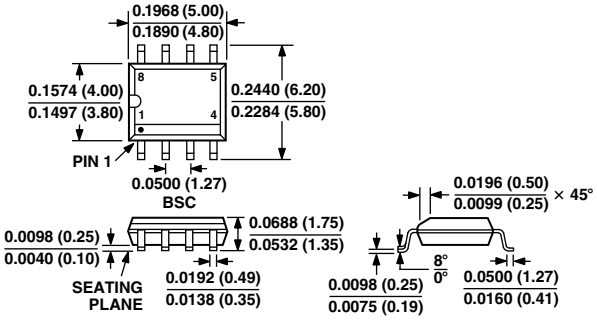


Figure 13. Recommended Circuit for Driving CMOS A/D

OUTLINE DIMENSIONS

Dimensions shown in inches and (millimeters)

8-Lead SOIC Package
(SO-8)



Revision History

Location	Page
6/02—Change from REV. 0 to REV. A.	
CHANGE to ORDERING GUIDE	3

C02054–0–6/02(A)

PRINTED IN U.S.A.