$1nV/\sqrt{Hz}$ Low Noise Instrumentation Amplifier

AD8229S

1.0. SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aeroinfo

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD8229.

2.0. Part Number: The complete part number(s) of this specification follows:

Part Number	Description
AD8229R703F	Radiation tested to 100K, Low Noise Instrumentation Amplifier

3.0. Case Outline

The case outline(s) are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F14	14	Bottom Brazed Flat Pack

Package: X			
Pin Number	Terminal Symbol	Pin Type	Pin Description
1	NC/GND	N/A	No Connection or ground this terminal
2	-IN	Analog Input	Negative input terminal
3	RG	Analog Input	Gain setting terminal. Place resistor across the RG pins to set the Gain. G = 1 + (6KΩ/RG)
4	RG	Analog Input	Gain setting terminal. Place resistor across the RG pins to set the Gain. G = 1 + (6KΩ/RG)
5	+IN	Analog Input	Positive input terminal
6	NC/GND	N/A	No Connection or ground this terminal
7	NC/GND	N/A	No Connection or ground this terminal
8	NC/GND	N/A	No Connection or ground this terminal
9	NC/GND	N/A	No Connection or ground this terminal
10	-Vs	Supply	Negative Power Supply Terminal
11	REF	Analog Input	Reference voltage terminal. Drive this terminal with low impedance voltage source to level shift the output
12	VOUT	Analog Output	Output Terminal
13	+Vs	Supply	Positive Power Supply Terminal
14	NC/GND	N/A	No Connection or ground this terminal

Figure 1 - Terminal connections.

ASD0016545 Rev. A

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4.0. Specifications

4.1. Absolute maximum ratings (TA = 25°C, unless otherwise noted) 1/

Supply Voltage (+Vs to -Vs)....................36 V
Output Short-Circuit Current Duration.................... Indefinite
Maximum Voltage at -IN, +IN....................+/- VS 2/
Differential Input Voltage –IN to +IN, Gain ≤ 4.................... +/- VS 2/
Differential Input Voltage –IN to +IN, 4 > Gain > 50.................... +/-50 V/Gain 2/
Differential Input Voltage –IN to +IN, Gain ≥ 50.................... +/-1 V 2/
Maximum Voltage at REF....................+/- VS 2/
Storage Temperature Range....................–65°C to +150°C
Power Dissipation (P_D)....................400 mW 3/
Lead Temperature (Soldering 10 Sec)....................+300°C
Junction Temperature (T_J)....................150°C
Thermal resistance, junction-to-case (θ_{JC}).................... 27 °C/W 4/
Thermal resistance, junction-to-ambient (θ_{JA}).................... 50 °C/W 4/

4.2. Recommended operating conditions

Supply Voltage (+/-Vs)....................+/- 5V to +/-15 V
Ambient operating temperature range (TA)....................-55°C to +125°C

4.3. Nominal operating performance characteristics 5/

Input / Output Characteristics:
Gain Nonlinearity RL = 10 kΩ, VOUT = +/-10V, G = 1 to 1000....................2 ppm
Gain Temperature Drift: G = 1....................2 ppm/°C
Gain Temperature Drift: G > 1....................-100 ppm/°C
CMRR DC to 60Hz with 1 kΩ imbalance, VCM = +/-10V, G=1....................90 dB
CMRR DC to 60Hz with 1 kΩ imbalance, VCM = +/-10V, G=10....................110 dB
CMRR DC to 60Hz with 1 kΩ imbalance, VCM = +/-10V, G=100....................130 dB
CMRR DC to 60Hz with 1 kΩ imbalance, VCM = +/-10V, G=1000....................140 dB
CMRR @ 5KHz, VCM = +/-10V, G=1....................80 dB
CMRR @ 5KHz, VCM = +/-10V, G=10 to 1000....................90 dB
Offset RTI vs. Supply (PSRR), Vs = +/-5V to +/-15V, G=10....................120 dB
Offset RTI vs. Supply (PSRR), Vs = +/-5V to +/-15V, G=100/1000....................130 dB
Output Swing, RL = 2 kΩ....................-VS + 1.8 V to +VS - 1.2 V
Output Swing, RL = 2 kΩ, TA = -55C to +125°C....................-VS + 1.9 V to +VS - 1.3 V
Output Short Circuit Current....................35 mA
Input Impedance (+/-IN to Ground)....................1.5 GΩ || 3 pF 6/

Reference Characteristics:
Reference Input Resistance....................10 kΩ
Reference Input Current, +/-IN= 0V....................70 µA
Reference Input Voltage Range.................... +/- VS

Noise Characteristics:
Voltage Noise RTI, Peak to Peak, 0.1Hz to 10Hz, +/-IN= 0V, G = 1000....................100 nV p-p
Current Noise Spectral Density: 1 KHz....................1.5 pA / √Hz
Peak to Peak Current Noise, 0.1Hz to 10Hz, G = 1000....................100 pA p-p

Dynamic Signal Response:

Small Signal Bandwidth -3dB, G=10..4 Mhz
Small Signal Bandwidth -3dB, G=100..1.2 Mhz
Small Signal Bandwidth -3dB, G=1000..0.15 Mhz
Settling Time 0.01%, 10V Step, G=1..0.75 μS
Settling Time 0.01%, 10V Step, G=10..0.65 μS
Settling Time 0.01%, 10V Step, G=100..0.85 μS
Settling Time 0.01%, 10V Step, G=1000..5 μS
Settling Time 0.001%, 10V Step, G=1..0.9 μS
Settling Time 0.001%, 10V Step, G=10..0.9 μS
Settling Time 0.001%, 10V Step, G=100..1.2 μS
Settling Time 0.001%, 10V Step, G=1000..7 μS
Total Harmonic Distortion, First five harmonics, f = 1 KHz, RL = 2 kΩ, VOUT = 10Vp-p G=1................-130 dBc
Total Harmonic Distortion, First five harmonics, f = 1 KHz, RL = 2 kΩ, VOUT = 10Vp-p G=10..............-116 dBc
Total Harmonic Distortion, First five harmonics, f = 1 KHz, RL = 2 kΩ, VOUT = 10Vp-p G=100............-113 dBc
Total Harmonic Distortion, First five harmonics, f = 1 KHz, RL = 2 kΩ, VOUT = 10Vp-p G=1000..........-111 dBc
Total Harmonic Distortion + N, f = 1 KHz, RL = 2 kΩ, VOUT = 10Vp-p G=100....................................0.0005 %

NOTES

1/ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2/ For voltages beyond these limits, use input protection resistors. See the Section 7.0 Application notes for more information.

3/ Include supply and output drive current for total power dissipation in actual application. Absolute maximum power limited by application actual maximum operating temperature and actual θ_{JA} to prevent exceeding absolute maximum Tj limit.

4/ Measurement taken under absolute worst case condition and represents data taken with thermal camera for highest power density location. See MIL-STD-1835 for average package θ_{JC} number.

5/ Unless otherwise noted, +/ −VS = +/−15 V, VREF = 0 V, TA = 25°C, G = 1, RL = 10 kΩ See commercial datasheet for other product application details.

6/ Differential and common-mode input impedance can be calculated from the pin impedance: ZDIFF = 2(ZPIN); ZCM = ZPIN/2.

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS
(+/-VS = +/-5V and +/-15V, Ta Max = +125C, Ta Min = -55C)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified		Sub-Group	Limit Min	Limit Max	Units
INPUT/OUTPUT CHARACTERISTICS							
Input Offset Voltage 2/	VOSI			1	-100	100	μV
				2,3	-125	125	μV
			M, D, P, L, R	1	-100	100	μV
Input Offset Voltage Drift 2/ 3/	$\Delta V_{OSI}/\Delta T$			2,3	-1	1	μV/°C
Output Offset Voltage 2/	VOSO			1	-1000	1000	μV
				2,3	-1250	1250	μV
			M, D, P, L, R	1	-1000	1000	μV
Output Offset Voltage Drift 2/ 3/	$\Delta V_{OSO}/\Delta T$			2,3	-10	10	μV/°C
Gain Range (G = 1 + 6 kΩ/RGain)	G			1,2,3	1	1000	V/V
			M, D, P, L, R	1	1	1000	V/V
Gain Error Gain = 1	GERR1	For Vs = +/-5V, V_{OUT} = +/-2V		1	-0.03	0.03	%
		For Vs = +/-15V, V_{OUT} = +/-10V		2,3	-0.04	0.04	%
		G = 1	M, D, P, L, R	1	-0.03	0.03	%
Gain Error Gain >1 4/	GERR>1	G =1000		1	-0.6	0.6	%
				2,3	-1.2	1.2	%
			M, D, P, L, R	1	-0.6	0.6	%
Input Bias Current	I_B	Vs = +/-15V		1	-150	150	nA
				2,3	-175	175	nA
			M, D, P, L, R	1	-150	150	nA
		Vs = +/-5V		1	-150	150	nA
				2	-175	175	nA
				3	-275	275	nA
			M, D, P, L, R	1	-150	150	nA
Input Offset Current	I_{OS}			1,2,3	-30	30	nA
			M, D, P, L, R	1	-30	30	nA
Input Voltage Range 5/	IVR	For CMRR1000 Min 126dB		1	-VS+2.8	+VS-2.5	V
		For CMRR1000 Min 125dB		2,3	-VS+2.8	+VS-2.5	V
			M, D, P, L, R	1	-VS+2.8	+VS-2.5	V
Common-Mode Rejection Ratio Gain = 1	CMRR1	For Vs = +/-5V, V_{CM} = -2.2V/+2.5V		1	86		dB
		For Vs = +/-15V, V_{CM} = +/-10V		2,3	85		dB
		G = 1	M, D, P, L, R	1	86		dB
Common-Mode Rejection Ratio Gain = 1000	CMRR1000	For Vs = +/-5V, V_{CM} = -2.2V/+2.5V		1	134		dB
		For Vs = +/-15V, V_{CM} = +/-10V		2,3	133		dB
		G = 1000	M, D, P, L, R	1	134		dB

See notes at end of Table

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)
(+/-VS = +/-5V and +/-15V, Ta Max = +125C, Ta Min = -55C)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified		Sub-Group	Limit Min	Limit Max	Units
INPUT/OUTPUT CHARACTERISTICS (continued)							
Output Swing	V_{SWING}	R_L = 10 kΩ		1	-Vs + 1.7	+Vs - 1.1	V
				2	-Vs + 1.8	+Vs - 1.2	
				3	-Vs + 2.0	+Vs - 1.2	
			M, D, P, L, R	1	-Vs + 1.7	+Vs - 1.1	
REFERENCE / POWER SUPPLY							
Reference Gain Error	REFerr	For Vs = +/-5V, REF = +/-2.5V For Vs = +/-15V, REF = +/-10V		1,2,3	-0.05	0.05	%
			M, D, P, L, R	1	-0.05	0.05	
Power Supply Rejection Ratio	PSRR	Vs = +/-5V to +/-15V		1	87		dB
				2,3	89		
			M, D, P, L, R	1	87		
Supply Current	I_S	Vs = +/-5V, +/-15V Vcm = 0V		1,2,3		9	mA
			M, D, P, L, R	1		9	
DYNAMIC PERFORMANCE							
Peak to Peak Voltage Noise 3/ 6/	Enp-p	Vs = +/-15V 0.1Hz to 10Hz, +/-IN = 0V		4,5,6		5	µV p-p
Input Spectral Density Voltage Noise 3/ 6/	Eni	Vs = +/-15V 10 KHz, +/-IN = 0V		4		1.1	nV / √Hz
				5		1.3	
				6		1.0	
Output Spectral Density Voltage Noise 3/ 6/	Eno	Vs = +/-15V 10 KHz, +/-IN = 0V		4		50	nV / √Hz
				5		57	
				6		42	
Small Signal Bandwidth 3/	BWss	Vs = +/-15V Vin = 100mVp-p single ended		4,5	15		Mhz
				6	13		
Slew Rate 3/	SR	Vs = +/-15V G = 1, 100 10% to 90% of 10V Output		4	22		V/ µS
				5	24		
				6	12		

TABLE I NOTES:
1/ Ta = Tambient, Ta Max = +125C, Ta Min = -55C. Unless otherwise noted, +/-VS = +/-5V and +/-15V; VREF = 0 V; G = 1; RL = 10 kΩ. See Section 7 Application Notes for more details

2/ Total RTI (Reference to Input) Vos = VOSI + VOSO/G).

3/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots. The test parameter Enp-p is also 100% production tested at Ta = Tambient.

4/ This specification is based on internal AD8229S gain setting resistors accuracies only and does not include the tolerance of the external gain setting resistor, RG. For G>1, external RGain errors should be added to the GERR>1 specifications.

5/ Input voltage range of the AD8229S input stage only. CMRR only specified under VCM input range conditions specified. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage. See Section 7 Application Notes for more details.

6/ RL = 50 Ω for Eno/Eni tests. No RL used on Enp-p. Total Voltage Noise = √(eni2 + (eno/G)2)+ eRG2). See Section 7 Application Notes for more details.

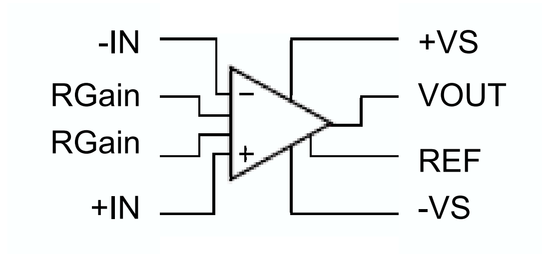

Figure 2 – AD8229 Block Diagram.

TABLE IIA – ELECTRICAL TEST REQUIREMENTS:

Table IIA	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4 1/ 2/ 3/
Group A Test Requirements	1, 2, 3, 4 2/ 3/
Group C end-point electrical parameters	1, 2, 3
Group D end-point electrical parameters	1, 2, 3
Group E end-point electrical parameters	1

Table IIA Notes:
1/ PDA apply to subgroup 1 only.
2/ See Table IIB for delta parameters.
3/ Parameters noted in Table I are part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

TABLE IIB – BURN-IN/GROUP C DELTA LIMITS 1/

Table IIB				
Parameter	Condition	Symbol	Delta	Units
Supply Current	Vs = +/-15V	I_S	+/-0.3	mA
Input Offset Voltage	Vs = +/-5V	VOSI	+/-13	μV
Output Offset Voltage	Vs = +/-15V	VOSO	+/-380	μV
Input Bias Current	Vs = +/-15V	I_B	+/-16	nA

1/ Conditions match Table I unless otherwise noted.

5.0. BURN-IN, LIFE TEST, AND RADIATION

5.1. Burn-in test circuit, Life Test circuit

The test conditions and circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 test condition B and alternate test condition D of MIL-STD-883.

HTRB is not applicable for this drawing.

5.2. Radiation exposure circuit.

The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A.

6.0. MIL-PRF-38535 QMLV EXCEPTIONS

6.1. Wafer Fabrication

Wafer fabrication occurs at a MIL-PRF-38535 QML Class Q certified facility.

6.2. Wafer Lot Acceptance (WLA)

WLA per MIL-STD-883 TM 5007 is not available for this product.

7.0. Application Notes

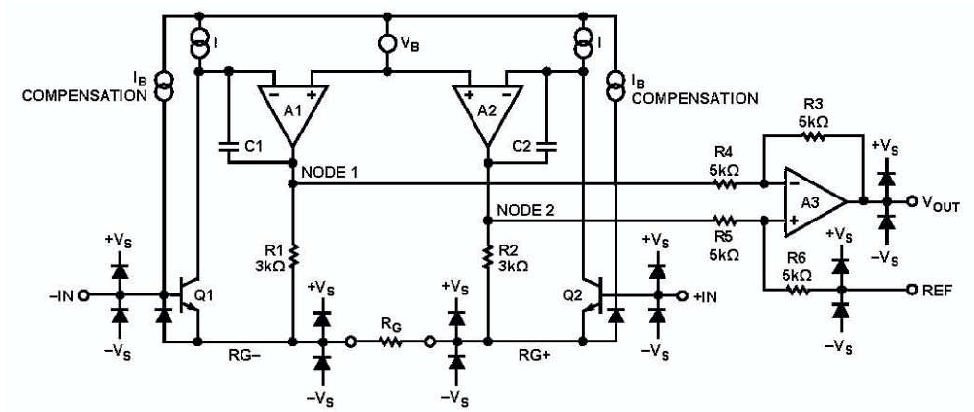

Figure 3 – AD8229S Simplified Schematic

ARCHITECTURE

The AD8229S is based on the classic 3-op-amp topology. This topology has two stages: a preamplifier to provide differential amplification followed by a difference amplifier that removes the common-mode voltage and provides additional amplification. The first stage works as follows. To keep its two inputs matched, Amplifier A1 must keep the collector of Q1 at a constant voltage. It does this by forcing RG− to be a precise diode drop from –IN. Similarly, A2 forces RG+ to be a constant diode drop from +IN. Therefore, a replica of the differential input voltage is placed across the gain setting resistor, RG. The current that flows through this resistance must also flow through the R1 and R2 resistors, creating a gained differential signal between the A2 and A1 outputs.

The second stage is a G = 1 difference amplifier, composed of Amplifier A3 and the R3 through R6 resistors. This stage removes the common-mode signal from the amplified differential signal. The transfer function is

$$VOUT = G \times (VIN+ - VIN-) + VREF \text{ where: } G = 1 + 6k\Omega/RG$$

GAIN SELECTION

Placing a resistor across the RG terminals sets the gain of the AD8229S, which can be calculated by using the following gain equation:

$$RG = 6k\Omega/ (G-1)$$

The AD8229S defaults to G = 1 when no gain resistor is used. Add the tolerance and gain drift of the RG resistor to the specifications of the AD8229S to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are minimal. The AD8229S duplicates the differential voltage across its inputs onto the RG resistor. Choose an RG resistor size sufficient to handle the expected power dissipation.

REFERENCE TERMINAL

The output voltage of the AD8229S is developed with respect to the potential on the reference terminal. This is useful when the output signal must be offset to a precise mid supply level. For example, a voltage source can be tied to the REF pin to level shift the output, allowing the AD8229S to drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either +VS or −VS by more than 0.3 V.

For best performance, maintain a source impedance to the REF terminal that is well below 1 Ω. The reference terminal, REF, is at one end of a 5 kΩ resistor. Additional impedance at the REF terminal adds to this 5 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional RREF can be calculated as follows:

2(5 kΩ + RREF)/(10 kΩ + RREF)

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades CMRR.

INPUT VOLTAGE RANGE

Figure 4 and Figure 5 show the allowable common-mode input voltage ranges for various output voltages and supply voltages. The 3-op-amp architecture of the AD8229S applies gain in the first stage before removing common-mode voltage with the difference amplifier stage. Internal nodes between the first and second stages (Node 1 and Node 2 in Figure 3) experience a combination of a gained signal, a common-mode signal, and a diode drop. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not limited.

$T = 25°C$, $V_S = ±15$, $V_{REF} = 0$, $R_L = 10$ kΩ, unless otherwise noted.

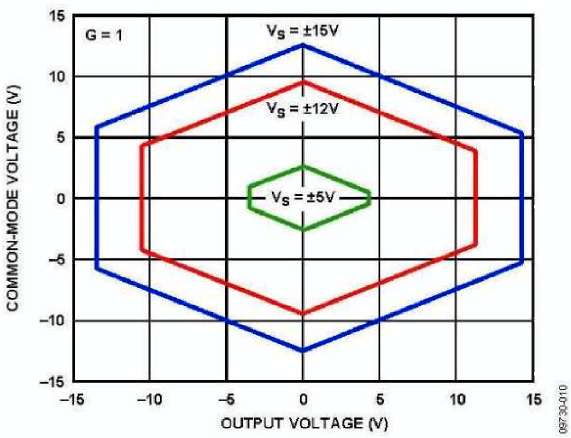

Figure 4. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±5 V, ±12 V, ±15 V (G = 1)

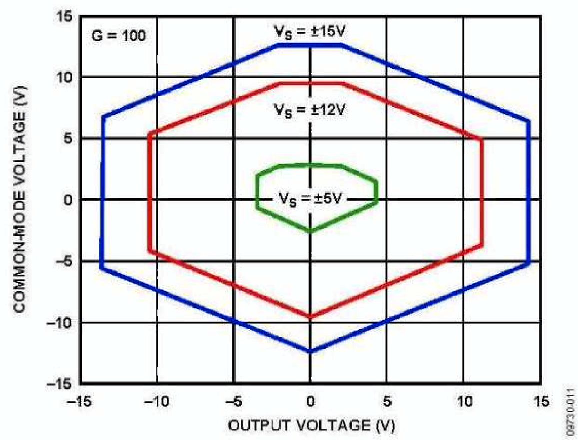

Figure 5. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, V_S = ±5 V, ±12 V, ±15 V (G = 100)

PCB LAYOUT

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To maintain high CMRR over frequency, closely match the input source impedance and capacitance of each path. Place additional source resistance in the input path (for example, for input protection) close to the in-amp inputs, which minimizes their interaction with parasitic capacitance from the PCB traces. Parasitic capacitance at the gain setting pins can also affect CMRR over frequency. If the board design has a component at the gain setting pins (for example, a switch or jumper), choose a component such that the parasitic capacitance is as small as possible.

Power Supplies and Grounding

Use a stable dc voltage to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance as specified by PSRR. Place a 0.1 μF capacitor as close as possible to each supply pin. Because the length of the bypass capacitor leads is critical at high frequency, surface-mount capacitors are recommended. A parasitic inductance in the bypass ground trace works against the low impedance created by the bypass capacitor. A 10 μF capacitor can be used farther away from the device. For larger value capacitors, intended to be effective at lower frequencies, the current return path distance is less critical. In most cases, this capacitor can be shared by other precision integrated circuits.

A ground plane layer is helpful to reduce parasitic inductances. This minimizes voltage drops with changes in current. The area of the current path is directly proportional to the magnitude of parasitic inductances and, therefore, the impedance of the path at high frequency. Large changes in currents in an inductive decoupling path or ground return create unwanted effects, due to the coupling of such changes into the amplifier inputs. Because load currents flow from the supplies, the load should be connected at the same physical location as the bypass capacitor grounds.

Reference Pin

The output voltage of the AD8229S is developed with respect to the potential on the reference terminal. Ensure that REF is tied to the appropriate local ground.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8229S must have a return path to ground. When using a floating source without a current return path, such as a thermocouple, create a current return path as shown in the ADI AD8229 commercial datasheet.

CALCULATING THE NOISE OF THE INPUT STAGE

The total noise of the amplifier front end depends on much more than the 1 nV/√Hz specification of this data sheet. There are three main contributors: the source resistance, the voltage noise of the instrumentation amplifier, and the current noise of the instrumentation amplifier. In the following calculations, noise is referred to the input (RTI). In other words, everything is calculated as if it appeared at the amplifier input. To calculate the noise referred to the amplifier output (RTO), simply multiply the RTI noise by the gain of the instrumentation amplifier.

Source Resistance Noise

Any sensor connected to the AD8229S has some output resistance. There may also be resistance placed in series with inputs for protection from either overvoltage or radio frequency interference. This combined resistance will be the total resistance at each input (+IN & -IN). Any resistor, no matter how well made, has an intrinsic level of noise. This noise is proportional to the square root of the resistor value. At room temperature, the value is approximately equal to 4 nV/√Hz × √(resistor value in kΩ). For example, assuming that the combined sensor and protection resistance on the +IN is 4 kΩ, and on the -IN is 1 kΩ, the total noise from the input resistance equals:

$$\sqrt{[(4 \times \sqrt{4})^{2} + \sqrt{[(4 \times \sqrt{1})^{2}}]} = 8.9 \text{ nV}/\sqrt{\text{Hz}}.$$

Voltage Noise of the Instrumentation Amplifier

The voltage noise of the instrumentation amplifier is calculated using three parameters: the device input noise, output noise, and the RG resistor noise. It is calculated as follows:

$$\text{Total Voltage Noise} = \sqrt{[(\text{Output Noise}/G)^{2} + (\text{Input Noise})^{2} + (\text{Noise of RG Resistor})^{2}]}$$

For example, for a gain of 100, the gain resistor is 60.4 Ω. Therefore, the voltage noise of the in-amp is

$$\sqrt{[(45/100)^{2} + (1)^{2} + (4 \times \sqrt{0.0604})^{2}]} = 1.5 \text{ nV}/\sqrt{\text{Hz}}$$

Current Noise of the Instrumentation Amplifier

Current noise is calculated by multiplying the source resistance by the current noise. For example, if the combined sensor and protection resistance on the +IN is 4 kΩ, and on the -IN is 1 kΩ, the total effect from the current noise is calculated as follows:

$$\sqrt{[(4 \times 1.5)^{2} + (1 \times 1.5)^{2}]} = 6.2 \text{ nV}/\sqrt{\text{Hz}}$$

Total Noise Density Calculation

To determine the total noise of the in-amp, referred to input, combine the source resistance noise, voltage noise, and current noise contribution by the sum of squares method. For example, if the combined sensor and protection resistance on the +IN is 4 kΩ, and on the -IN is 1 kΩ and the gain of the in-amp is 100, and using noise calculated above, the total noise, referred to input, is $\sqrt{[(8.9 \text{ nV}/\sqrt{\text{Hz}})^{2} + (1.5 \text{ nV}/\sqrt{\text{Hz}})^{2} + (6.2 \text{ nV}/\sqrt{\text{Hz}})^{2}]} = 11.0 \text{ nV}/\sqrt{\text{Hz}}$

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8229R703F	−55°C to +125°C	14 Pin Dual Flat Pack	CDFP3-F14

Revision History

Rev	Description of Change	Date
A	Initial Release	5/29/2013