1.8 V Low Power CMOS Rail-to-Rail Input/Output Operational Amplifier

AD8515

FEATURES

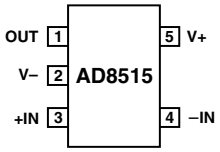
Single-Supply Operation: 1.8 V to 5 V
Offset Voltage: 6 mV Max
Space-Saving SOT-23 and SC70 Packages
Slew Rate: 2.7 V/μs
Bandwidth: 5 MHz
Rail-to-Rail Input and Output Swing
Low Input Bias Current: 2 pA Typ
Low Supply Current @ 1.8 V: 450 μA Max

APPLICATIONS

Portable Communications
Portable Phones
Sensor Interfaces
Laser Scanners
PCMCIA Cards
Battery-Powered Devices
New Generation Phones
Personal Digital Assistants

PIN CONFIGURATION

5-Lead SC70 and SOT-23
(KS and RT Suffixes)



GENERAL DESCRIPTION

The AD8515 is a rail-to-rail amplifier that can operate from a single-supply voltage as low as 1.8 V.

The AD8515 single amplifier, available in SOT-23-5L and SC70-5L packages, is small enough to be placed next to sensors, reducing external noise pickup.

The AD8515 is a rail-to-rail input and output amplifier with a gain bandwidth of 5 MHz and typical offset voltage of 1 mV from a 1.8 V supply. The low supply current makes these parts ideal for battery-powered applications. The 2.7 V/μs slew rate makes the AD8515 a good match for driving ASIC inputs, such as voice codecs.

The AD8515 is specified over the extended industrial temperature range (–40°C to +125°C).

REV. B

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AD8515–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = 1.8 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = V_S/2		1	6	mV
		–40°C < T_A < +125°C			8	mV
Input Bias Current	I_B	V_S = 1.8 V		2	30	pA
		–40°C < T_A < +85°C			600	pA
		–40°C < T_A < +125°C			8	nA
Input Offset Current	I_{OS}			1	10	pA
		–40°C < T_A < +125°C			300	pA
Input Voltage Range			0		1.8	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.8 V	50			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, 0.3 V ≤ V_{OUT} ≤ 1.5 V	110	400		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA, –40°C < T_A < +125°C	1.79			V
		I_L = 750 µA, –40°C < T_A < +125°C	1.77			V
Output Voltage Low	V_{OL}	I_L = 100 µA, –40°C < T_A < +125°C			10	mV
		I_L = 750 µA, –40°C < T_A < +125°C			30	mV
Short Circuit Limit	I_{SC}			20		mA
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	V_{OUT} = V_S/2		300	450	µA
		–40°C < T_A < +125°C			500	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		2.7		V/µs
Gain Bandwidth Product	GBP			5		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		22		nV/$\sqrt{\text{Hz}}$
		f = 10 kHz		20		nV/$\sqrt{\text{Hz}}$
Current Noise Density	i_n	f = 1 kHz		0.05		pA/$\sqrt{\text{Hz}}$

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = 3.0 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} =V_S/2		1	6	mV
		–40°C < T_A < +125°C			8	mV
Input Bias Current	I_B	V_S = 3.0 V		2	30	pA
		–40°C < T_A < +85°C			600	pA
		–40°C < T_A < +125°C			8	nA
Input Offset Current	I_{OS}			1	10	pA
		–40°C < T_A < +125°C			300	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 3.0 V	54			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, 0.3 V ≤ V_{OUT} ≤ 2.7 V	250	1,000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA, –40°C < T_A < +125°C	2.99			V
		I_L = 750 µA, –40°C < T_A < +125°C	2.98			V
Output Voltage Low	V_{OL}	I_L = 100 µA, –40°C < T_A < +125°C			10	mV
		I_L = 750 µA, –40°C < T_A < +125°C			20	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 1.8 V to 5.0 V,				
		–40°C < T_A < +125°C	65	85		dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = V_S/2		300	450	µA
		–40°C < T_A < +125°C			500	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		2.7		V/µs
Gain Bandwidth Product	GBP			5		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		22		nV/$\sqrt{\text{Hz}}$
		f = 10 kHz		20		nV/$\sqrt{\text{Hz}}$
Current Noise Density	i_n	f = 1 kHz		0.05		pA/$\sqrt{\text{Hz}}$

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = 5.0 V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = V_S/2		1	6	mV
		–40°C < T_A < +125°C			8	mV
Input Bias Current	I_B	V_S = 5.0 V		5	30	pA
		–40°C < T_A < +85°C			600	pA
		–40°C < T_A < +125°C			8	nA
Input Offset Current	I_{OS}			1	10	pA
		–40°C < T_A < +125°C			300	pA
Input Voltage Range			0		5.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 5.0 V	60	75		dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, 0.3 V ≤ V_{OUT} ≤ 4.7 V	500	2,000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 100 µA, –40°C < T_A < +125°C	4.99			V
		I_L = 750 µA, –40°C < T_A < +125°C	4.98			V
Output Voltage Low	V_{OL}	I_L = 100 µA, –40°C < T_A < +125°C			10	mV
		I_L = 750 µA, –40°C < T_A < +125°C			20	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 1.8 V to 5.0 V,				
		–40°C < T_A < +125°C	65	82		dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = V_S/2		350	500	µA
		–40°C < T_A < +125°C			600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		2.7		V/µs
Gain Bandwidth Product	GBP			5		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		22		nV/$\sqrt{\text{Hz}}$
		f = 10 kHz		20		nV/$\sqrt{\text{Hz}}$
Current Noise Density	i_n	f = 1 kHz		0.05		pA/$\sqrt{\text{Hz}}$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

Supply Voltage . . . . . 6 V
Input Voltage . . . . . GND to V_S
Differential Input Voltage . . . . . ±6 V or ±V_S
Output Short-Circuit Duration
to GND . . . . . Observe Derating Curves
Storage Temperature Range
KS and RT Packages . . . . . –65°C to +150°C
Operating Temperature Range
AD8515 . . . . . –40°C to +125°C
Junction Temperature Range
KS and RT Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}*	θ_{JC}	Unit
5-Lead SOT-23 (RT)	230	146	°C/W
5-Lead SC70 (KS)	376	126	°C/W

*θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

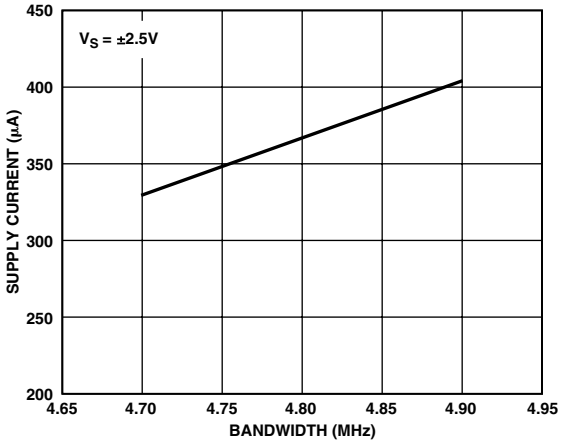
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8515ART	–40°C to +125°C	5-Lead SOT-23	RT-5
AD8515AKS	–40°C to +125°C	5-Lead SC70	KS-5

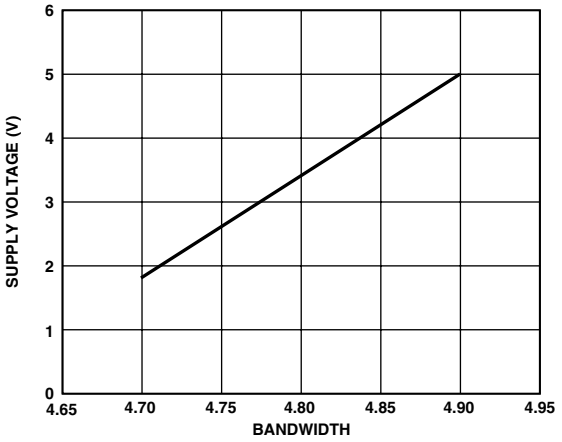
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8515 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

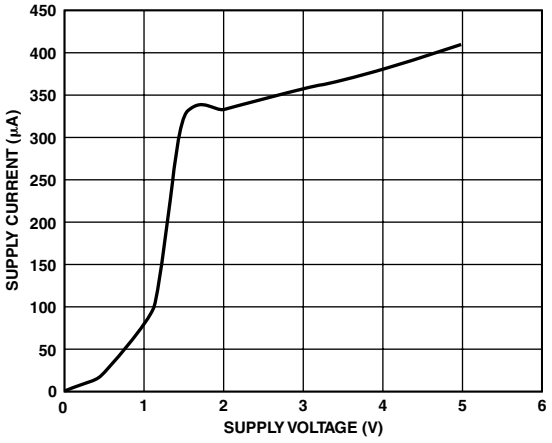
AD8515–Typical Performance Characteristics



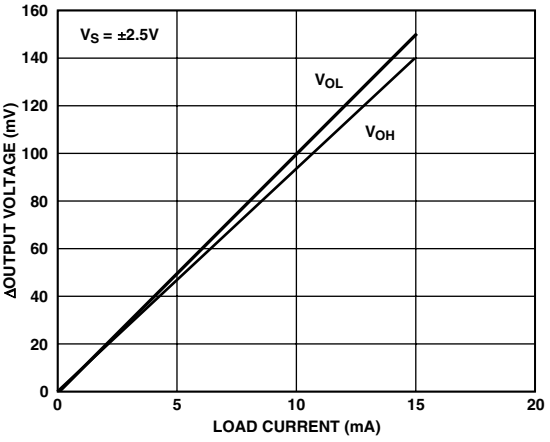
TPC 1. Supply Current vs. Bandwidth



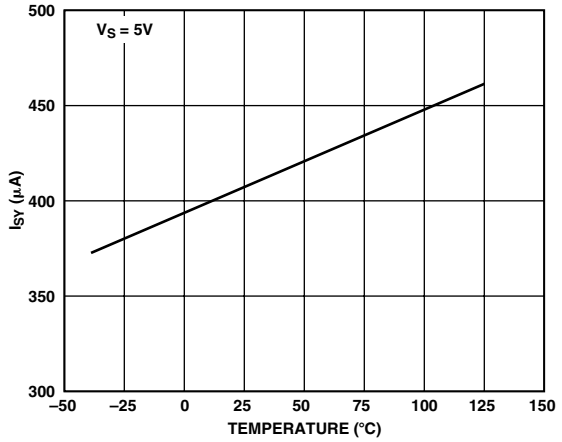
TPC 4. Supply Voltage vs. Bandwidth



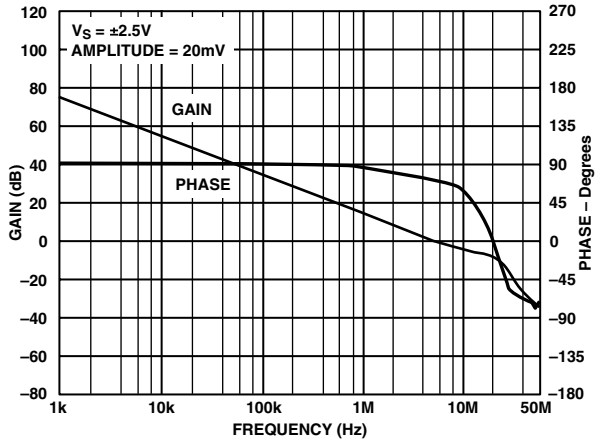
TPC 2. Supply Current vs. Supply Voltage



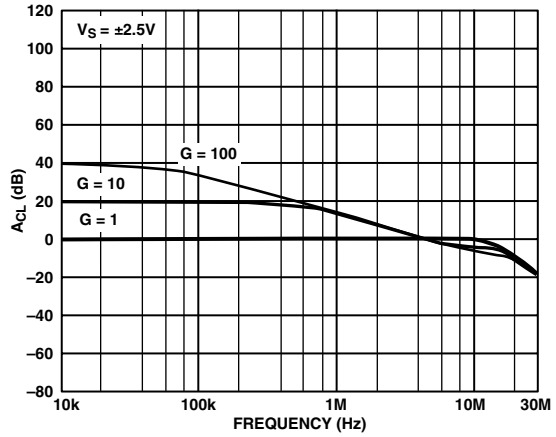
TPC 5. Output Voltage to Supply Rail vs. Load Current



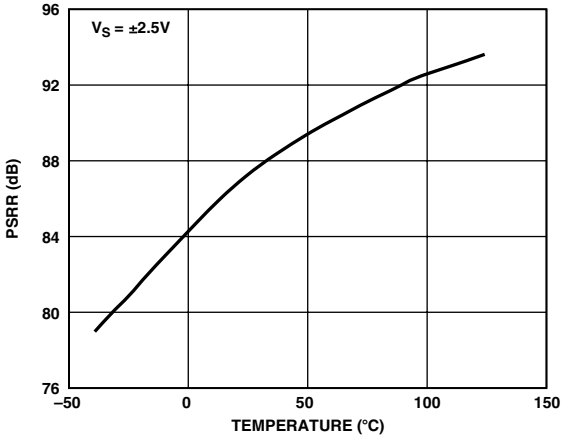
TPC 3. I_{SY} vs. Temperature



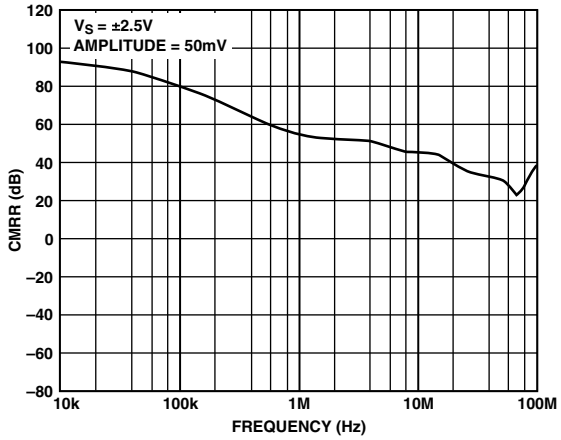
TPC 6. Gain and Phase vs. Frequency



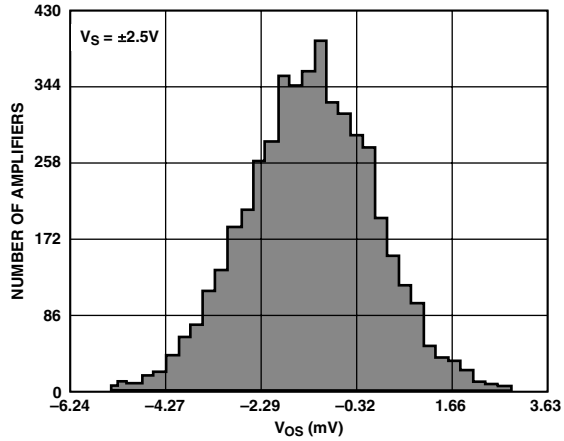
TPC 7. A_{CL} vs. Frequency



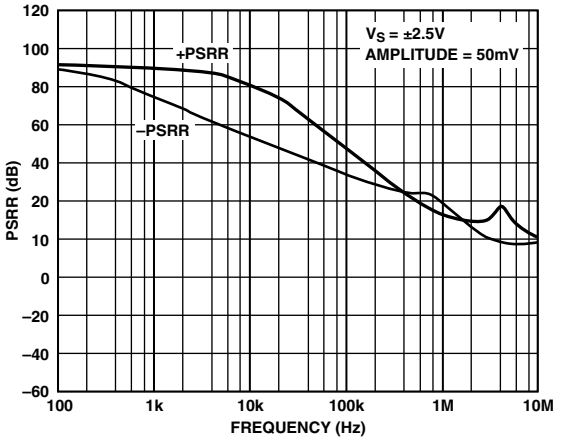
TPC 10. PSRR vs. Temperature



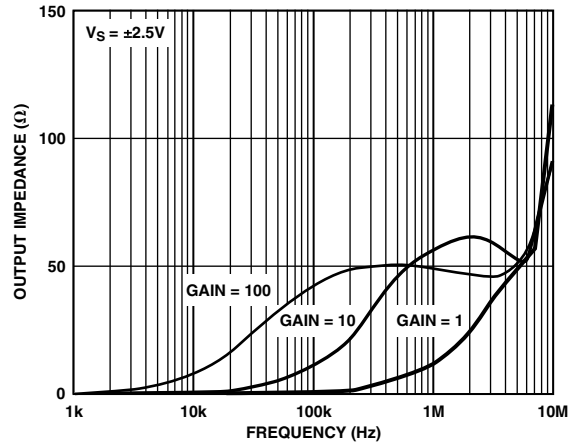
TPC 8. CMRR vs. Frequency



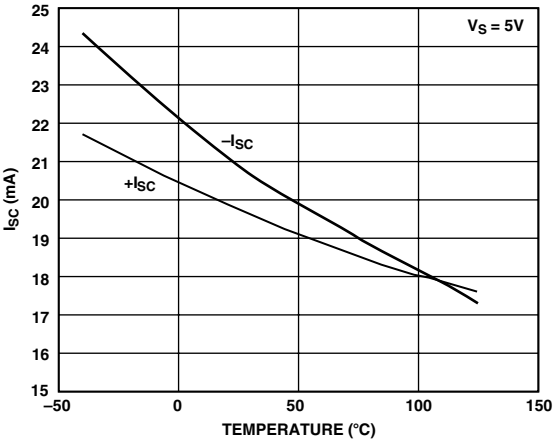
TPC 11. V_{OS} Distribution



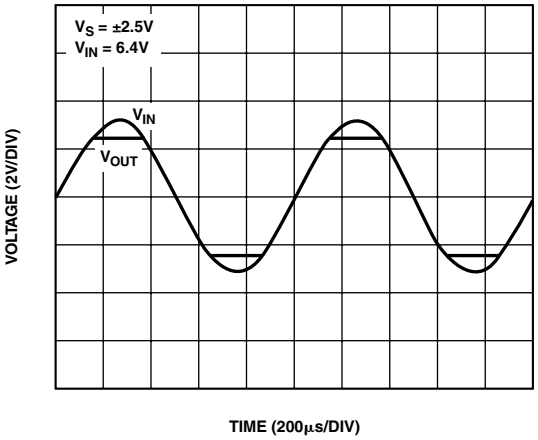
TPC 9. PSRR vs. Frequency



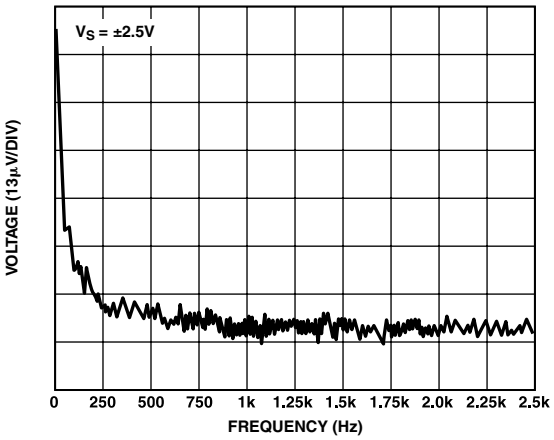
TPC 12. Output Impedance vs. Frequency



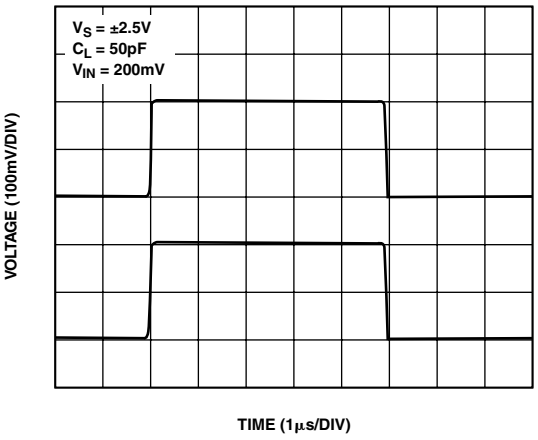
TPC 13. I_{SC} vs. Temperature



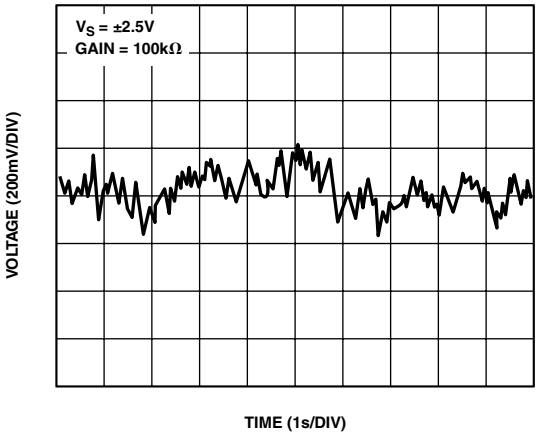
TPC 16. No Phase Reversal



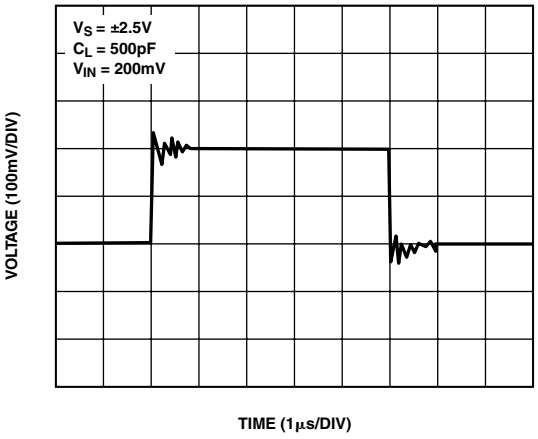
TPC 14. Voltage Noise Density



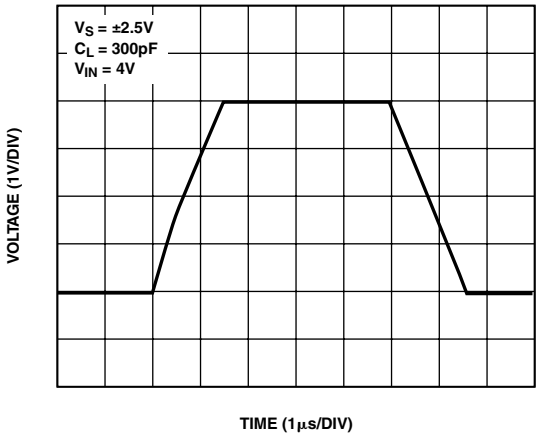
TPC 17. Small Signal Transient Response



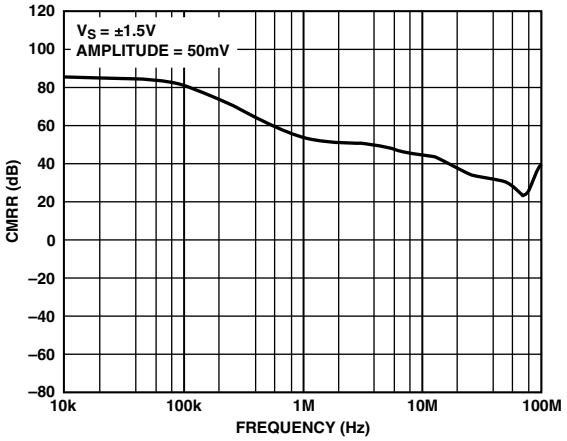
TPC 15. Input Voltage Noise



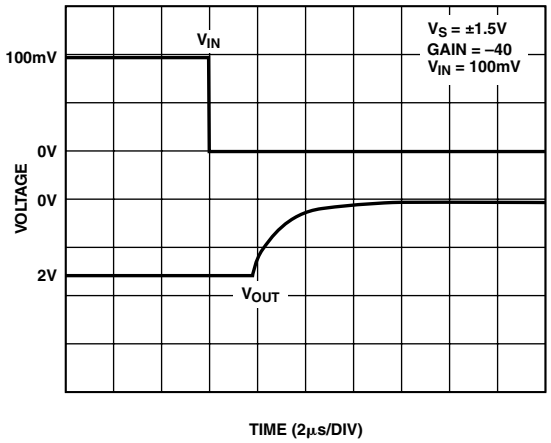
TPC 18. Small Signal Transient Response



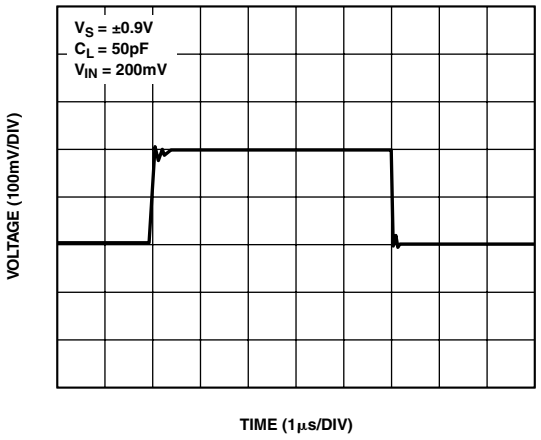
TPC 19. Large Signal Transient Response



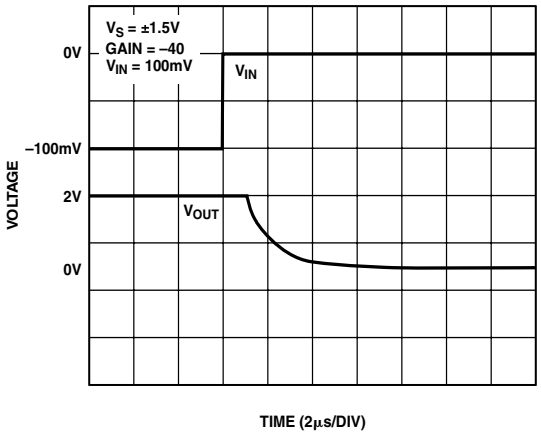
TPC 22. CMRR vs. Frequency



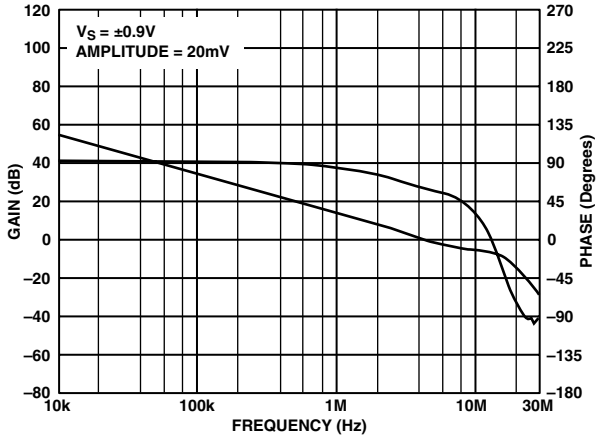
TPC 20. Saturation Recovery



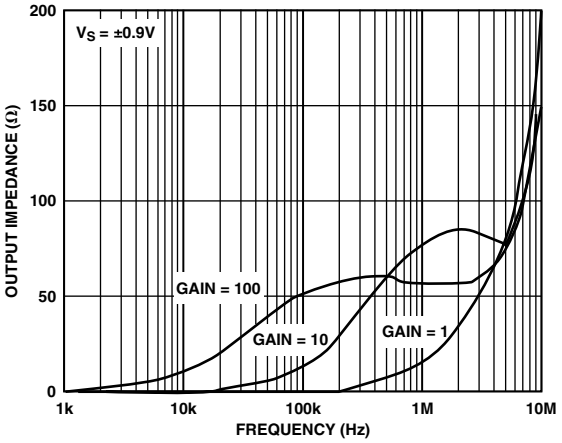
TPC 23. Small Signal Transient Response



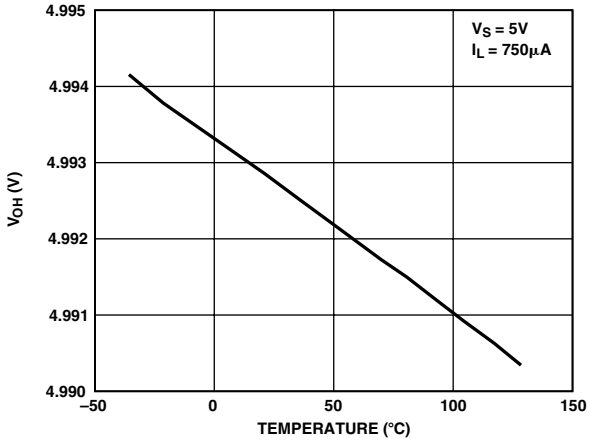
TPC 21. Saturation Recovery



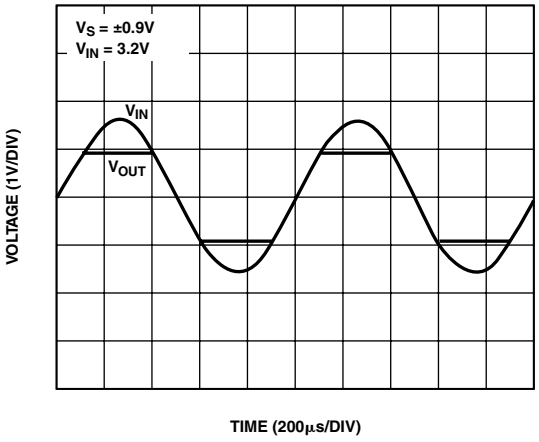
TPC 24. Gain and Phase vs. Frequency



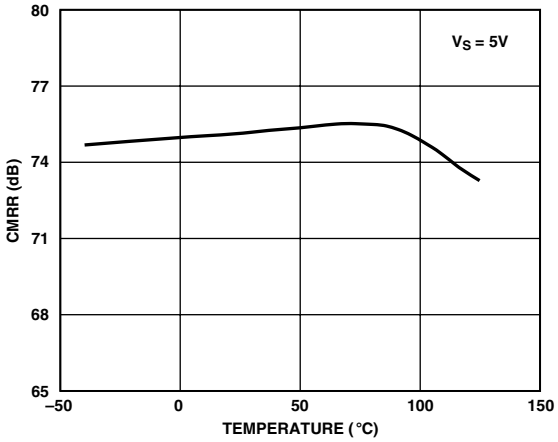
TPC 25. Output Impedance vs. Frequency



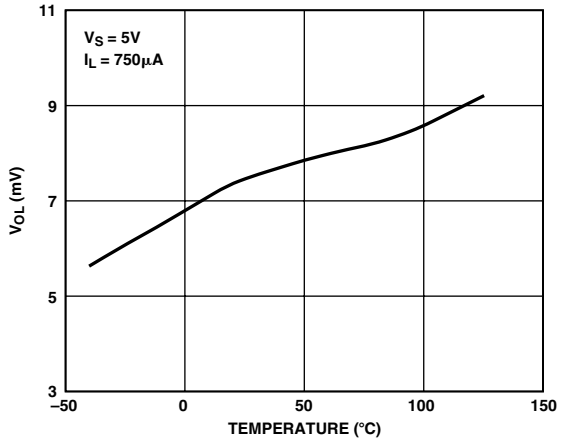
TPC 28. V_{OH} vs. Temperature



TPC 26. No Phase Reversal



TPC 29. CMRR vs. Temperature



TPC 27. V_{OL} vs. Temperature

FUNCTIONAL DESCRIPTION

The AD8515, offered in space-saving SOT-23 and SC70 packages, is a rail-to-rail input and output operational amplifier that can operate at supply voltages as low as 1.8 V. This product is fabricated using 0.6 micron CMOS to achieve one of the best power consumption to speed ratios (i.e., bandwidth) in the industry. With a small amount of supply current (less than 400 μA), a wide unity gain bandwidth of 4.5 MHz is available for signal processing.

The input stage consists of two parallel, complementary, differential pairs of PMOS and NMOS. The AD8515 exhibits no phase reversal as the input signal exceeds the supply by more than 0.6 V. Currents into the input pin must be limited to 5 mA or less by the use of external series resistance(s). The AD8515 has a very robust ESD design and can stand ESD voltages of up to 4,000 V.

Power Consumption vs. Bandwidth

One of the strongest features of the AD8515 is the bandwidth stability over the specified temperature range while consuming small amounts of current. This effect is shown in TPC 1 through TPC 3. This product solves the speed/power requirements for many applications. The wide bandwidth is also stable even when operated with low supply voltages. TPC 4 shows the relationship between the supply voltage versus the bandwidth for the AD8515.

The AD8515 is ideal for battery-powered instrumentation and handheld devices since it can operate at the end of discharge voltage of most popular batteries. Table I lists the nominal and end of discharge voltages of several typical batteries.

Table I. Typical Battery Life Voltage Range

Battery	Nominal Voltage (V)	End of Discharge Voltage (V)
Lead-Acid	2	1.8
Lithium	2.6–3.6	1.7–2.4
NiMH	1.2	1
NiCd	1.2	1
Carbon-Zinc	1.5	1.1

DRIVING CAPACITIVE LOADS

Most amplifiers have difficulty driving large capacitive loads. Additionally, higher capacitance at the output can increase the amount of overshoot and ringing in the amplifier's step response and could even affect the stability of the device. This is due to the degradation of phase margin caused by additional phase lag from the capacitive load. The value of capacitive load that an amplifier can drive before oscillation varies with gain, supply voltage, input signal, temperature, and other parameters. Unity gain is the most challenging configuration for driving capacitive loads. The AD8515 is capable of driving large capacitive loads without any external compensation. The graphs in Figures 1a and 1b show the amplifier's capacitive load driving capability when configured in unity gain of +1.

The AD8515 is even capable of driving higher capacitive loads in inverting gain of –1, as shown in Figure 2.

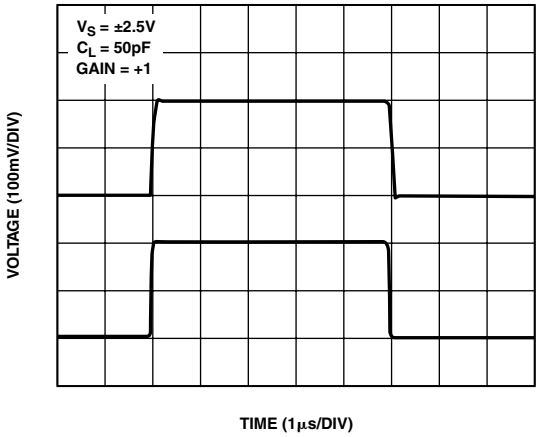


Figure 1a. Capacitive Load Driving @ C_L = 50 pF

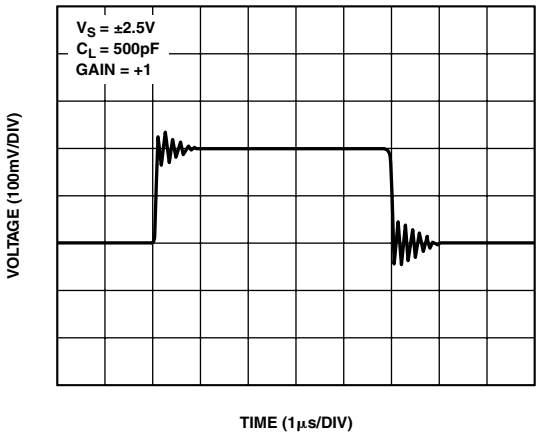


Figure 1b. Capacitive Load Driving @ C_L = 500 pF

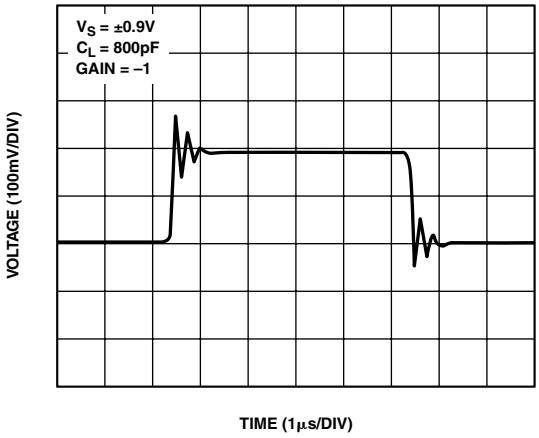


Figure 2. Capacitive Load Driving @ C_L = 800 pF

Full Power Bandwidth

The slew rate of an amplifier determines the maximum frequency at which it can respond to a large input signal. This frequency (known as full power bandwidth, *FPBW*) can be calculated from the equation

$$FPBW = \frac{SR}{2\pi \times V_{PEAK}}$$

for a given distortion. The *FPBW* of AD8515 is shown in Figure 3 to be close to 200 kHz.

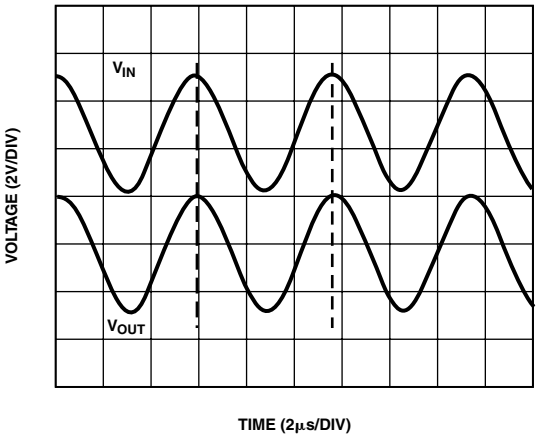


Figure 3. Full Power Bandwidth

A MICROPOWER REFERENCE VOLTAGE GENERATOR

Many single-supply circuits are configured with the circuit biased to one-half of the supply voltage. In these cases, a false ground reference can be created by using a voltage divider buffered by an amplifier. Figure 4 shows the schematic for such a circuit. The two 1 MΩ resistors generate the reference voltages while drawing only 0.9 μA of current from a 1.8 V supply. A capacitor connected from the inverting terminal to the output of the op amp provides compensation to allow for a bypass capacitor to be connected at the reference output. This bypass capacitor helps establish an ac ground for the reference output.

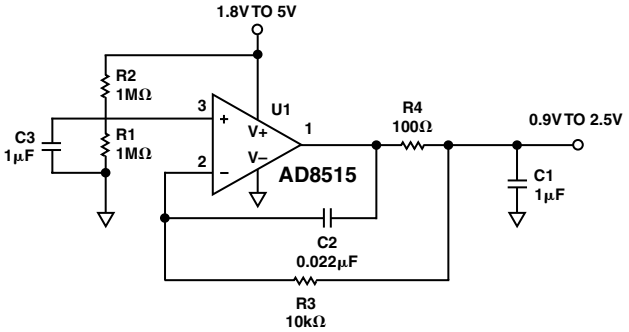


Figure 4. Micropower Voltage Reference Generator

A 100 kHz Single-Supply Second Order Band-Pass Filter

The circuit in Figure 5 is commonly used in portable applications where low power consumption and wide bandwidth are required. This figure shows a circuit for a single-supply band-pass filter with a center frequency of 100 kHz. It is essential that the op amp has a loop gain at 100 kHz in order to maintain an accurate center frequency. This loop gain requirement necessitates the choice of an op amp with a high unity gain crossover frequency, such as the AD8515. The 4.5 MHz bandwidth of the AD8515 is sufficient to accurately produce the 100 kHz center frequency, as the response in Figure 6 shows. When the op amp's bandwidth is close to the filter's center frequency, the amplifier's internal phase shift causes excess phase shift at 100 kHz, which alters the filter's response. In fact, if the chosen op amp has a bandwidth close to 100 kHz, the phase shift of the op amps will cause the loop to oscillate.

A common-mode bias level is easily created by connecting the noninverting input to a resistor divider consisting of two resistors connected between VCC and ground. This bias point is also decoupled to ground with a 1 μF capacitor.

$$f_L = \frac{1}{2\pi \times R1 \times C1}$$

$$f_H = \frac{1}{2\pi \times R1 \times C1}$$

$$H_0 = 1 + \frac{R2}{R1}$$

$$VCC = 1.8\ V - 5\ V$$

where:

f_L is the low –3 db frequency.

f_H is the high –3 db frequency.

H_0 is the midfrequency gain.

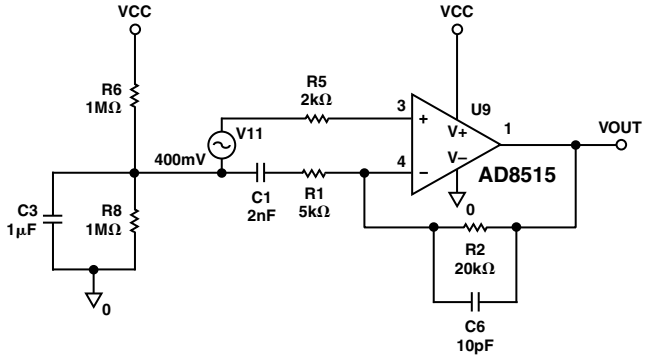


Figure 5. Second Order Band-Pass Filter

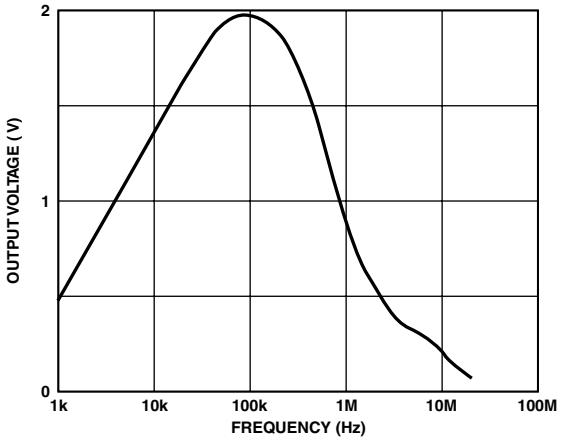


Figure 6. Frequency Response of the Band-Pass Filter

Wien Bridge Oscillator

The circuit in Figure 7 can be used to generate a sine wave, one of the most fundamental waveforms. Known as a Wien Bridge oscillator, it has the advantage of requiring only one low power amplifier. This is an important consideration, especially for battery-operated applications where power consumption is a critical issue. To keep the equations simple, the resistor and capacitor values used are kept equal. For the oscillation to happen, two conditions have to be met. First, there should be a zero phase shift from the input to the output, which will happen at the oscillation frequency of

$$F_{OSC} = \frac{1}{2\pi R10 \times C10}$$

Second, at this frequency, the ratio of VOUT to the voltage at +input (Pin 3) has to be 3, which means that the ratio of R11/R12 should be greater than 2.

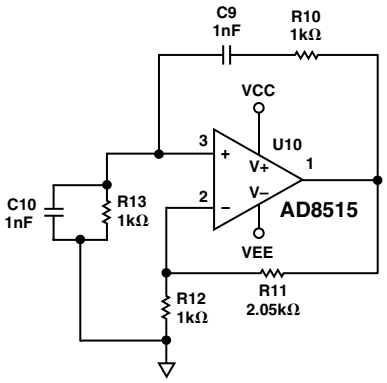


Figure 7. Low Power Wien Bridge Oscillator

High frequency oscillators can be built with the AD8515 due to its wide bandwidth. Using the values shown, an oscillation frequency of 130 kHz is created and is shown in Figure 8. If R11 is too low, the oscillation might converge; if too large, the oscillation will diverge until the output clips (V_S = ±2.5 V, F_{OSC} = 130 kHz).

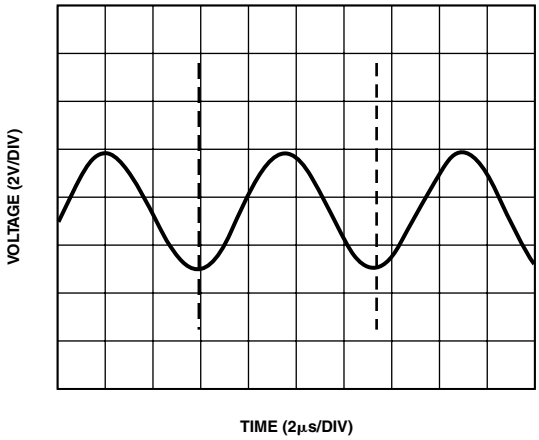
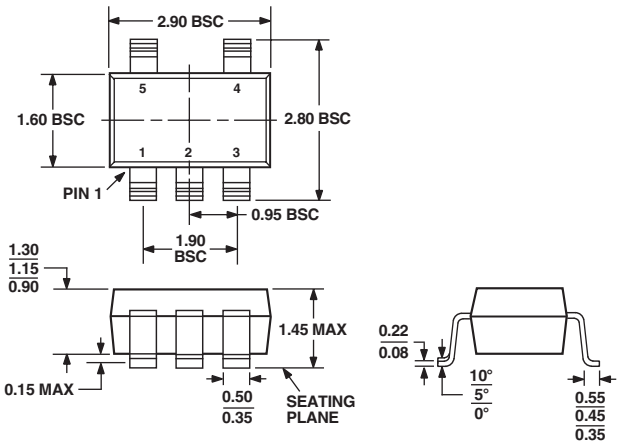


Figure 8. Output of Wien Bridge Oscillator

OUTLINE DIMENSIONS

5-Lead Small Outline Transistor Package [SOT-23]
(RT-5)

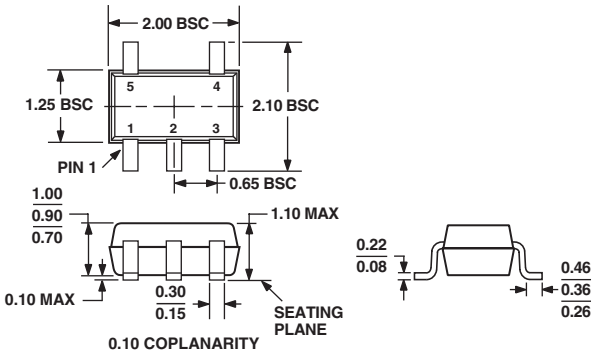
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178AA

5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203AA

Revision History

Location	Page
4/03—Data Sheet changed from REV. A to REV. B.	
Change to Figure 5	12
2/03—Data Sheet changed from REV. 0 to REV. A.	
Added new SC70 Package	Universal
Changes to FEATURES	1
Changes to GENERAL DESCRIPTION	1
Changes to PIN CONFIGURATION	1
Changes to SPECIFICATIONS	2
Changes to ABSOLUTE MAXIMUM RATINGS	5
Changes to ORDERING GUIDE	5
Changes to TPC 3	6
Changes to TPC 10	7
Changes to TPC 13	8
Changes to TPC 27	10
Changes to TPC 28	10
Added new TPC 29	10
Changes to FUNCTIONAL DESCRIPTION	11
Updated to OUTLINE DIMENSIONS	14