



Dual 8-Bit 50 MSPS A/D Converter

AD9058

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD9058

2.0 Part Number. The complete part number(s) of this specification follow:

<u>Part Number</u>	<u>Description</u>
AD9058R803D	Radiation Tested, Dual 8-Bit 50 MSPS A/D Converter

2.1 Case Outline.

<u>Letter</u>	<u>Descriptive designator</u>	<u>Case Outline (Lead Finish per MIL-PRF-38535)</u>
D	CDIP2-T48	48-Lead ceramic dual-in-line package (SIDEBRAZED)

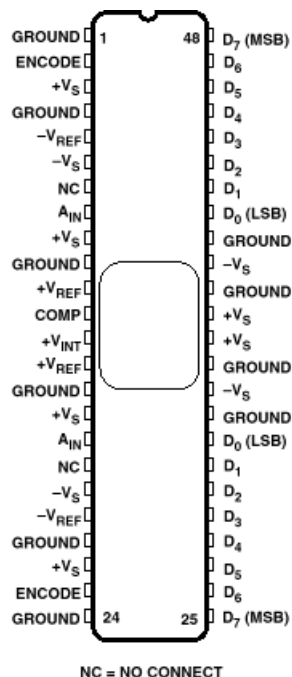


Figure 1 - Terminal connections.

ASD0011184

Rev. I

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AD9058

3.0 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Positive Supply Voltage	+6V
Negative Supply Voltage.....	+0.8V to -6V
Analog Input	-1.5V to +2.5V
Digital Inputs	-0.5V to V+
Digital Output Current	20 mA
Voltage Reference Current.....	53 mA
+V _{REF}	+2.5V
-V _{REF}	-1.5V
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	+300°C
Dice Junction Temperature (T _J)	+175°C

3.1 Thermal Characteristics:

Thermal Resistance, SIDEBRAZED (D) Package

Junction-to-Case (Θ_{JC}) = 12°C/W Max

Junction-to-Ambient (Θ_{JA}) = 40 °C/W Max

4.0 Electrical Table:

Table I

Parameter	Symbol	Conditions <u>1/</u>	Sub-group	Limit Min	Limit Max	Units
Differential nonlinearity <u>5/</u>	DNL		1		0.5	LSB
			2,3		1.0	
Integral nonlinearity <u>5/</u>	INL		1		1.0	
			2,3		1.25	
Input Bias current <u>5/</u>	I _B		1		170	μA
			2,3		340	
Input resistance <u>5/</u>	R _I		1	12		KΩ
Input capacitance <u>2/</u> <u>5/</u>	C _I	A _{IN} =0V	4		15	pF
Reference Ladder resistance <u>5/</u>	R _{RL}		1	120	220	Ω
			2,3	80	270	
Reference Ladder offset (top) <u>5/</u>	O _{RLT}		1		16	mV
			2,3		24	
Reference Ladder offset (bottom) <u>5/</u>	O _{RLB}		1		23	
			2,3		33	
Reference voltage	V _{REF}		1	1.95	2.2	V
			2,3	1.90	2.25	
		M, D, L, R <u>6/</u>	1	1.95	2.2	
High level output voltage	V _{OH}		1,2,3	2.4		V
		M, D, L, R <u>6/</u>		2.4		
Low level output voltage	V _{OL}		1,2,3		0.4	V
		M, D, L, R <u>6/</u>			0.4	
Positive supply current	+I _S		1,2,3		167	mA
		M, D, L, R <u>6/</u>			167	
Negative supply current	-I _S		1,2,3		41	
		M, D, L, R <u>6/</u>			41	
Power dissipation <u>4/</u> <u>5/</u>	P _D		1,2,3		1040	mW

Table I (cont'd)

Parameter	Symbol	Conditions <u>1/</u>	Sub-group	Limit Min	Limit Max	Units
Encode pulse voltage (high) <u>2/</u> <u>5/</u>	V_{EH}		1,2,3	2.0		V
Encode pulse voltage (low) <u>2/</u> <u>5/</u>	V_{EL}		1,2,3		0.8	
Encode pulse current (high) <u>5/</u>	I_{EH}		1,2,3		300	μA
Encode pulse current (low) <u>5/</u>	I_{EL}		1,2,3		500	
V_{REF} Power supply rejection ratio	PSRR	No Load	1		25	mV/V
		M, D, L, R <u>6/</u>	1		25	mV/V
Conversion rate <u>5/</u>	CONV		4	50		MSPS
Output delay (valid) <u>5/</u>	t_V	2K Ω pulldowns	9	5		nS
Aperature delay <u>2/</u> <u>5/</u>	t_A		9	0.1	1.5	
Aperature delay matching <u>2/</u> <u>5/</u>	t_{AM}		9		0.5	
Propagation delay <u>5/</u>	t_{PD}	2K Ω pulldowns	9		19	
Effective number of bits <u>3/</u> <u>5/</u>	ENOB	$A_{IN} = 2.3$ MHz	4	6.9		Bits
		$A_{IN} = 10.3$ MHz		6.8		
Signal-to-noise ratio <u>3/</u> <u>5/</u>	SNR	$A_{IN} = 2.3$ MHz	4	44		dB
		$A_{IN} = 10.3$ MHz		43		
		$A_{IN} = 2.3$ MHz, 50 MSPS encode		41		
		$A_{IN} = 2.3$ MHz, 8 nS HIGH encode		44		
		$A_{IN} = 2.3$ MHz, 8 nS LOW encode		44		
2 nd harmonic distortion <u>5/</u>	HD ₂	$A_{IN} = 2.3, 10.3$ MHz	4	48		dBc
3 rd harmonic distortion <u>5/</u>	HD ₃	$A_{IN} = 2.3, 10.3$ MHz	4	50		dBc
Crosstalk rejection <u>2/</u> <u>5/</u>	CR	$A_{IN} = 2.3, 3.5$ MHz, 40 MSPS	4	48		

NOTES:

1/ $\pm V_S = \pm 5V$; $+V_{REF} = +2V$ (internal); $-V_{REF} = \text{Ground}$; Encode = 40 MSPS; $A_{IN} = 0V$ to $+2V$.

2/ Test limit is characterized and is guaranteed at $T_C = +25^\circ C$ but not tested.

3/ Measured with analog input signal 1 dB below full scale at specified frequency.

4/ Test limit applies to both A/D's and includes Ladder dissipation.

5/ Not radiation tested.

6/ Radiation tested at 100Krad

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 9 <u>1/</u> <u>2/</u>
Group A Test Requirements	1, 2, 3, 4, 9
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1 only. Delta limits are excluded from PDA

2/ See table III for delta limits.

4.2 Table III. Burn-in test delta limits.

Parameter	Symbol	Post Burn In Limit		Post Life Test Limit		Life Test Delta	Units
		Min	Max	Min	Max		
Power Supply Current	+I _S		167		167	±16.7	mA
	-I _S		41		41	±4.1	
Input Bias Current	I _{IB}		170		190	20	μA
Digital Output High Voltage	V _{OH}	2.4		2.4		±.24	V
Digital Output Low Voltage	V _{OL}		0.4		0.4	±0.1	

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

6.0 MIL-STD-38535 QMLV exceptions:

6.1 Full WLA per MIL-STD-883 TM5007 is not available for this product. SEM inspection only is available per MIL-STD-883, TM2018.

Rev	Description of Change	Date
A	Initiate	June 9, 2000
B	Delete reference to case X and case Y in Table I.	Aug. 28, 2000
C	Update web address.	Feb. 7, 2002
D	Add <u>1</u> / to conditions, add <u>2</u> / to Vin conditions, change ENOB from 7.0 to 6.9 Bits, Delete delta V_{REF} , add Delta V_{OL} , V_{OH} , and I_{IB} .	Oct. 16, 2002
E	Change part number AD9058R803D to part number AD9058-813D. ADI accepts no lot jeopardy for new die revision. Add V_{REF} to PSSR test title.	Oct. 18, 2002
F	Update web address. Change SNR limits to minimum. Add “R” part number. Add post irradiation limits. Limits for V_{REF} and $V_{REF}PSSR$ to be added when data is collected.	Apr. 22, 2003
G	Update table III. Change VOL delta limit from .04 V to 0.1 V. Remove burn-in schematic	May 21, 2003
H	Update header/footer & add to 1.0 Scope description.	Feb. 21, 2008
I	Remove P/N AD9058-803D, change AD9058-813D to AD9058R803D	June 11, 2008

