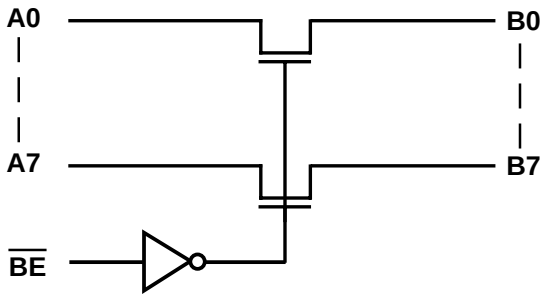
2.5 V/3.3 V, 8 Bit, 2 Port Level Translator, Bus Switch

Preliminary Technical Data — ADG3245

FEATURES
175ps Propagation Delay through the switch
3.5 Ω Switch Connection between Ports
2.5 V/3.3 V Supply Operation
Selectable Level Shifting/Translation
Level Translation
3.3 V to 2.5 V
3.3 V to 1.8 V
2.5 V to 1.8 V
20 Lead TSSOP & CSP Packages

APPLICATIONS
3.3 V to 1.8 V Voltage Translation
3.3 V to 2.5 V Voltage Translation
2.5 V to 1.8 V Voltage Translation
Bus Switching
Bus Isolation
Analog Switch Applications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG3245 is a 2.5 V or 3.3 V 8 bit, 2 port digital switch. It is designed on a low voltage CMOS process which provides low power dissipation yet gives high switching speed and very low on resistance allowing inputs to be connected to the outputs without additional propagation delay or generating additional ground bounce noise.

The switches are enabled by means of the Bus Enable, ($\overline{BE}$) input signal. These digital switches allow bi-directional signals to be switched when ON. In the OFF condition, signal levels up to the supplies are blocked. This device is ideal for applications requiring level translation. When operated from a 3.3 V supply, level translation from 3.3V inputs to 2.5V outputs is allowed. Similarly, if the device is operated from a 2.5 V supply and 2.5 V inputs are applied, the device will translate the outputs to 1.8 V. In addition to this, a level translating select pin ($\overline{SEL}$) is included. When $\overline{SEL}$ is low, V_{CC} is reduced internally allowing for level translation between 3.3V inputs and 1.8V outputs. This makes the device suited to applications requiring level translation between different supplies, such as converter to DSP interfacing.

PRODUCT HIGHLIGHTS

1. 3.3 V or 2.5 V Supply Operation.
2. Extremely low Propagation Delay through switch.
3. 3.5 Ω Switches connect inputs to Outputs.
4. Level/Voltage Translation.
5. 20 Lead TSSOP and CSP (4mm x 4mm) packages.

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ADG3245–SPECIFICATIONS[1]

(V_{CC} = +2.3 V to +3.6 V, GND = 0 V, All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Symbol	Conditions[2]	B Version Min	Typ[3]	Max	Units
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V_{INH}	V_{CC} = 2.7 V to 3.6 V	2.0			V
	V_{INH}	V_{CC} = 2.3 V to 2.7 V	1.7			V
Input Low Voltage	V_{INL}	V_{CC} = 2.7 V to 3.6 V	-0.5		0.8	V
	V_{INL}	V_{CC} = 2.3 V to 2.7 V	-0.5		0.7	V
Input Leakage Current	I_I	$0 \le V_{IN} \le 3.6$ V			±1	µA
OFF State leakage Current	I_{OZ}	$0 \le A, B \le V_{CC}$		±0.001	±1	µA
ON State leakage Current		$0 \le A, B \le V_{CC}$		±0.001	±1	µA
Max Pass Voltage	V_P	$V_{IN} = V_{CC} = \overline{SEL}$ = 3.3 V, I_O = -5µA	tbd	2.5	2.9	V
		$V_{IN} = V_{CC} = \overline{SEL}$ = 2.5 V, I_O= -5µA		1.8		V
		$V_{IN} = V_{CC}$ = 3.3 V, $\overline{SEL}$ = 0 V, I_O= -5µA		1.8		V
CAPACITANCE[4]						
A Port Off Capacitance	C_A OFF	f = 1 MHz		5		pF
B Port Off Capacitance	C_B OFF	f = 1 MHz		5		pF
A, B Port On Capacitance	C_A,C_B ON	f = 1 MHz		10		pF
Control Input Capacitance	C_{IN}	f = 1 MHz		3		pF
SWITCHING CHARACTERISTICS[3]						
Propagation Delay A to B or B to A, t_{PD}[5]	t_{PHL}, t_{PLH}	C_L = 50 pF, V_{CC} = 3.3 V			0.175	ns
Propagation Delay Matching[6]					TBD	ps
Bus Enable Time $\overline{BE}$ to A or B	t_{PZH}, t_{PZL}	C_L = 50 pF, R_L = 500 Ω, V_{CC} = 3.0 V	tbd	6	9	ns
Bus Disable Time $\overline{BE}$ to A or B	t_{PLZ}, t_{PLZ}	C_L = 50 pF, R_L = 500 Ω, V_{CC} = 3.0 V	tbd	3	8	ns
Bus Enable Time $\overline{BE}$ to A or B	t_{PZH}, t_{PZL}	C_L = 50 pF, R_L = 500 Ω, V_{CC} = 2.3 V	tbd	6	9	ns
Bus Disable Time $\overline{BE}$ to A or B	t_{PLZ}, t_{PLZ}	C_L = 50 pF, R_L = 500 Ω, V_{CC} = 2.3 V	tbd	3	8	ns
Max Data Rate				TBD		Mbps
Channel Jitter				TBD		ps p-p
DIGITAL SWITCH						
On Resistance	R_{ON}	V_{CC} = 3 V, $\overline{SEL} = V_{CC}$, V_A = 0 V, I_{IN} = 15 mA		3.5	6	Ω
		V_{CC} = 3 V, $\overline{SEL} = V_{CC}$, V_A = 2.4 V, I_{IN} = 8 mA		tbd	tbd	Ω
		V_{CC} = 2.3 V, $\overline{SEL} = V_{CC}$, V_A = 0 V, I_{IN} = 15 mA		5	8	Ω
		V_{CC} = 2.3 V, $\overline{SEL} = V_{CC}$, V_A = 1.7 V, I_{IN} = 8 mA		tbd	tbd	Ω
		V_{CC} = 3.3 V, $\overline{SEL}$ = 0 V V_A = 0 V, I_{IN} = 15 mA		5	8	Ω
		V_{CC} = 3.3 V, $\overline{SEL}$ = 0 V, V_A = 1.7 V, I_{IN} = 8 mA		tbd	tbd	Ω
On Resistance Matching	ΔR_{ON}	V_{CC} = 3.3 V, $\overline{SEL} = V_{CC}$, V_A = 0 V, I_{IN} = 15 mA		tbd	tbd	Ω
		V_{CC} = 3.3 V, $\overline{SEL} = V_{CC}$, V_A = 1.7 V, I_{IN} = 8 mA		tbd	tbd	Ω
POWER REQUIREMENTS						
V_{CC}			2.3		3.6	V
Quiescent Power Supply Current	I_{CC}	Digital Inputs = 0 V or V_{CC}		0.001	1	µA
Increase in I_{CC} per input[5]	ΔI_{CC}	V_{CC} = + 3.6 V, One input at 3.0 V;				
		Others at V_{CC} or GND			50	µA

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]See Test Circuits and Waveforms.

[3]Typical values are at +25°C unless otherwise stated.

[4]Guaranteed by design, not subject to production test.

[5]The digital switch contributes no propagation delay other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propogation delay to the system. Propogation Delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

[6]Propagation delay matching between channels is calculated from the On Resistance matching and load capacitance of 50pF.

[7]This current applies to the control pins only and represents the current required to switch internal capacitance at the specified frequency. The A and B ports contribute no significant AC or DC currents as they transition. This parameter is guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{CC} to GND	-0.5 V to +4.6 V
Digital Inputs to GND	-0.5 V to +4.6 V
DC Input Voltage	-0.5 V to +4.6 V
DC Output Current	120mA
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
CSP Package	
θ_{JA} Thermal Impedance	35°C/W
TSSOP Package	
θ_{JA} Thermal Impedance	143°C/W
Lead Temperature, Soldering (10seconds)	300°C
IR Reflow, Peak Temperature (<20 seconds)	+235°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

Table 1. Pin Description

Pin Mnemonic	Description
$\overline{BE}$	Bus Enable (Active Low)
$\overline{SEL}$	Level Translation Select
Ax	Port A, Inputs or Ouputs
Bx	Port B, Inputs or Outputs

Table 2. Truth Table

$\overline{BE}$	$\overline{SEL}$	Function
L	L	A = B, 3.3 V to 1.8 V Level Shifting
L	H	A = B
H	X	Disconnect

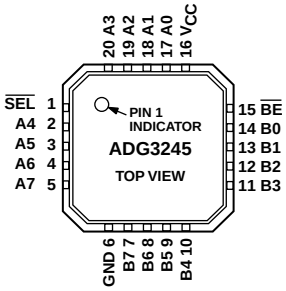
ORDERING GUIDE

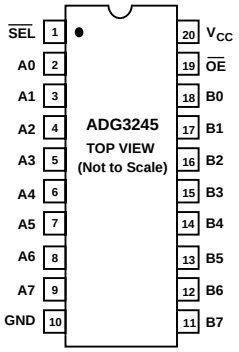
Model	Temperature Range	Package Descriptions	Package Options
ADG3245BCP	–40°C to +85°C	Leaded Chip Scale Package (CSP)	CP-20
ADG3245BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG3245 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

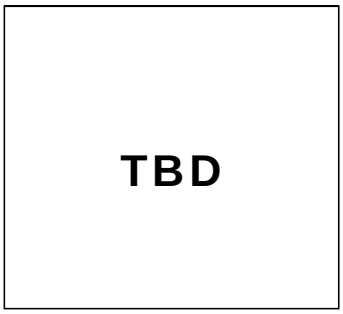
PIN CONFIGURATION
20 LEAD CSP & 20 LEAD TSSOP



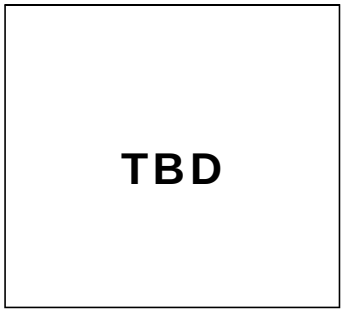


ADG3245

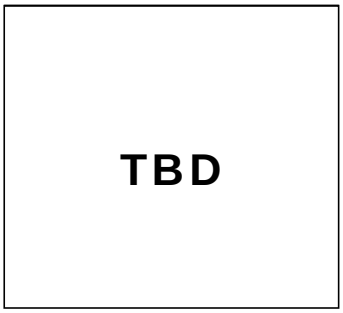
TYPICAL PERFORMANCE CHARACTERISTICS



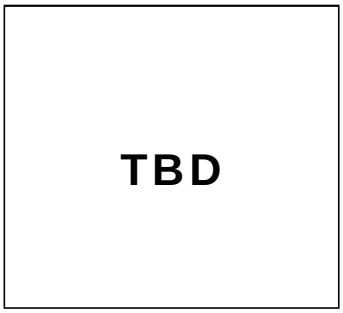
TPC 1. On Resistance vs Input Voltage(V_{CC} = 3.3 V)



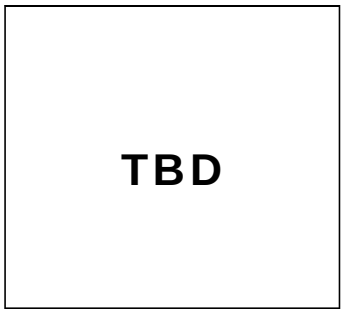
TPC 2. On Resistance vs Input Voltage (V_{CC} = 2.5 V)



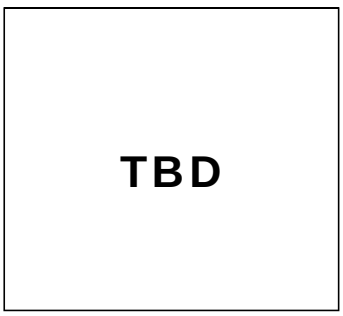
TPC 3. Max Pass Voltage vs V_{CC}



TPC 4. I_{CC} vs Enable Frequency



TPC 5. Output Low Characteristic



TPC 6. Output High Characteristic

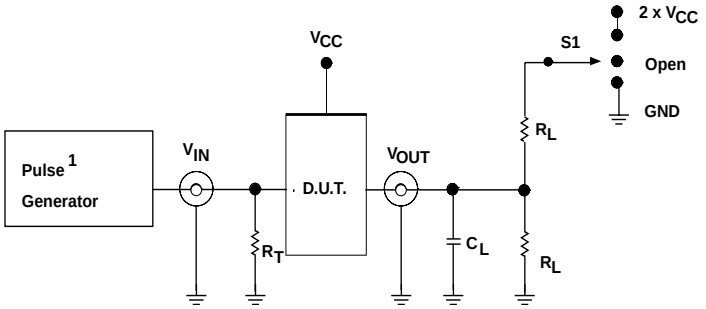


Figure 1. Load Circuit

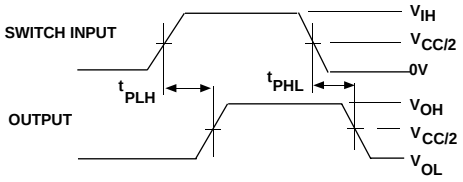


Figure 2. Propagation Delay

Note
1. Pulse Generator for all pulses: $t_R \leq 2.5$ns, $t_F \leq 2.5$ns, Frequency $\leq$ 10MHz
C_L = includes board, stray and load capacitances.
R_T is the termination resistor, should be equal to Zout of the pulse generator

Table 3 Switch Position

TEST	S1
t_{PLH}, t_{PHL}	OPEN
t_{PLZ}, t_{PZL}	2 x V_{CC}
t_{PHZ}, t_{PZH}	GND

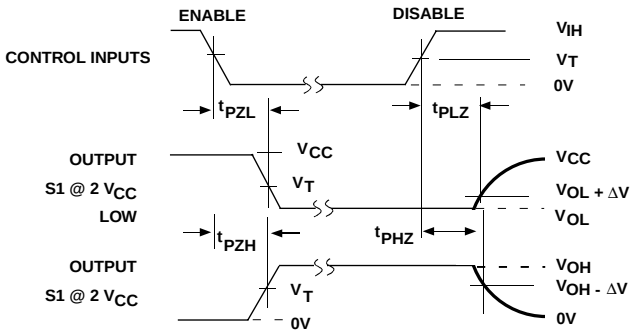


Figure 3. Enable and Disable Times

Test Conditions

Symbol	V_{CC} = 3.3 V ± 0.3V	V_{CC} = 2.5 ± 0.2V	V_{CC} = 3.3 ±0.3V ($\overline{SEL}$ = 0 V)	Units
R_L	500	500	500	Ω
V_Δ	300	150	150	mV
C_L	50	30	30	pF
V_T	1.5	$V_{CC}/2$	1.5	V

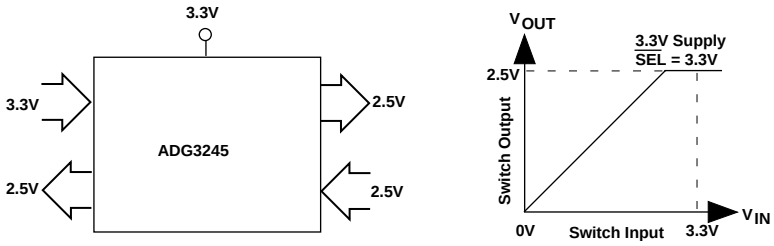


Figure 4. 3.3 V to 2.5 V Voltage Translation, $\overline{SEL}$ = 3.3V

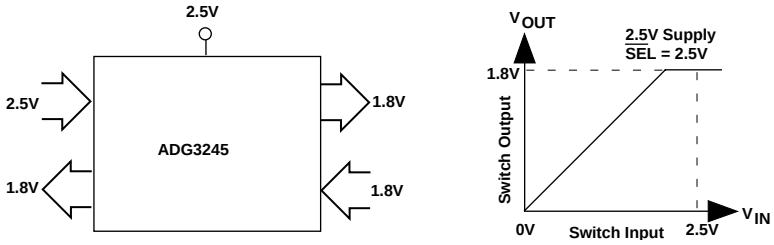


Figure 5. 2.5 V to 1.8 V Voltage Translation, $\overline{SEL}$ = 2.5V

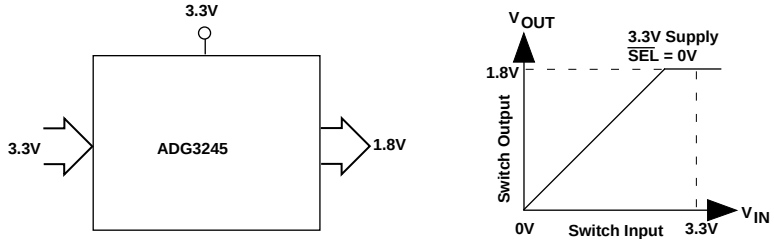
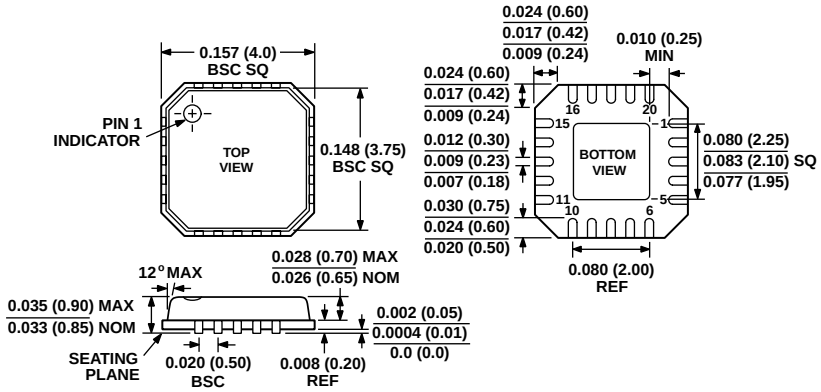


Figure 6. 3.3 V to 1.8 V Voltage Translation, $\overline{SEL}$ = 0V

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead CSP
(CP-20)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS

20-Lead TSSOP
(RU-20)