

ADG708/ADG709

FEATURES

1.8 V to 5.5 V Single Supply
 ± 3 V Dual Supply
3 Ω On-Resistance
0.75 Ω On-Resistance Flatness
100 pA Leakage Currents
14 ns Switching Times
Single 8-to-1 Multiplexer ADG708
Differential 4-to-1 Multiplexer ADG709
16-Lead TSSOP Package
Low Power Consumption
TTL/CMOS-Compatible Inputs

APPLICATIONS

Data Acquisition Systems
Communication Systems
Relay Replacement
Audio and Video Switching
Battery-Powered Systems

GENERAL DESCRIPTION

The ADG708 and ADG709 are low voltage, CMOS analog multiplexers comprising eight single channels and four differential channels respectively. The ADG708 switches one of eight inputs (S1–S8) to a common output, D, as determined by the 3-bit binary address lines A0, A1, and A2. The ADG709 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF.

Low power consumption and operating supply range of 1.8 V to 5.5 V make the ADG708 and ADG709 ideal for battery-powered, portable instruments. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels.

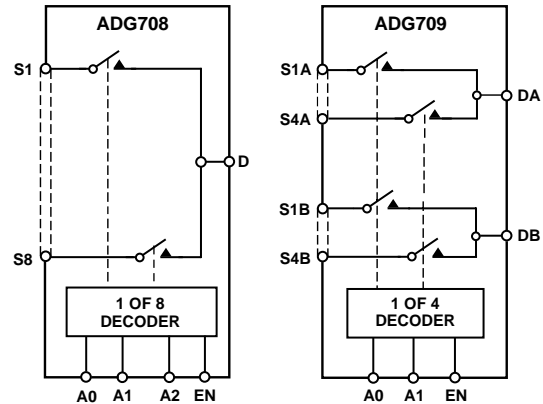
These switches are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on-resistance and leakage currents. On-resistance is in the region of a few ohms and is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either Multiplexers or Demultiplexers, and have an input signal range that extends to the supplies.

The ADG708 and ADG709 are available in a 16-lead TSSOP package.

REV. 0

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FUNCTIONAL BLOCK DIAGRAMS



PRODUCT HIGHLIGHTS

1. Single/Dual Supply Operation. The ADG708 and ADG709 are fully specified and guaranteed with 3 V and 5 V single supply and ± 3 V dual supply rails.
2. Low R_{ON} (3 Ω Typical).
3. Low Power Consumption (<0.01 μ W).
4. Guaranteed Break-Before-Make Switching Action.
5. Small 16-Lead TSSOP Package.

ADG708/ADG709—SPECIFICATIONS¹ ($V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Version –40°C		C Version –40°C		Unit	Test Conditions/Comments
	+25°C	to +85°C	+25°C	to +85°C		
ANALOG SWITCH						
Analog Signal Range	0 V to V_{DD}		0 V to V_{DD}		V	$V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 10\text{ mA}$; Test Circuit 1
On-Resistance (R_{ON})	3		3		Ω typ	
	4.5	5	4.5	5	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.4		0.4		Ω typ	$V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 10\text{ mA}$; $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.75	0.8	0.75	0.8	Ω max	
		1.2		1.2	Ω typ	
					Ω max	
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	± 0.01		± 0.01		nA typ	$V_{DD} = 5.5\text{ V}$ $V_D = 4.5\text{ V/1 V}$, $V_S = 1\text{ V/4.5 V}$; Test Circuit 2
		± 20	± 0.1	± 0.3	nA max	
Drain OFF Leakage I_D (OFF)	± 0.01		± 0.01		nA typ	$V_D = 4.5\text{ V/1 V}$, $V_S = 1\text{ V/4.5 V}$; Test Circuit 3
		± 20	± 0.1	± 0.75	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.01		± 0.01		nA typ	$V_D = V_S = 1\text{ V}$, or 4.5 V, Test Circuit 4
		± 20	± 0.1	± 0.75	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4		2.4		V min	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}	0.8		0.8		V max	
Input Current I_{INL} or I_{INH}	0.005		0.005		μA typ	
		± 0.1		± 0.1	μA max	
C_{IN} , Digital Input Capacitance	2		2		pF typ	
DYNAMIC CHARACTERISTICS²						
$t_{TRANSITION}$	14		14		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 5 $V_{S1} = 3\text{ V/0 V}$, $V_{SS} = 0\text{ V/3 V}$
		25		25	ns max	
Break-Before-Make Time Delay, t_D	8		8		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 6
		1		1	ns min	
$t_{ON(EN)}$	14		14		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 7
		25		25	ns max	
$t_{OFF(EN)}$	7		7		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$, Test Circuit 7
		12		12	ns max	
Charge Injection	± 3		± 3		pC typ	$V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 8
Off Isolation	–60		–60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 9
	–80		–80		dB typ	
Channel-to-Channel Crosstalk	–60		–60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 10
	–80		–80		dB typ	
–3 dB Bandwidth	55		55		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	13		13		pF typ	
C_D (OFF)						
ADG708	85		85		pF typ	
ADG709	42		42		pF typ	
C_D , C_S (ON)						
ADG708	96		96		pF typ	
ADG709	48		48		pF typ	
POWER REQUIREMENTS						
I_{DD}	0.001		0.001		μA typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
		1.0		1.0	μA max	

NOTES

¹Temperature range is as follows: B and C Versions: –40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS¹(V_{DD} = 3 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted)

Parameter	B Version		C Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C		
ANALOG SWITCH						
Analog Signal Range		0 V to V _{DD}		0 V to V _{DD}	V	
On-Resistance (R _{ON})	8		8		Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA;
	11	12	11	12	Ω max	Test Circuit 1
On-Resistance Match Between Channels (ΔR _{ON})		0.4		0.4	Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA
		1.2		1.2	Ω max	
LEAKAGE CURRENTS						
Source OFF Leakage I _S (OFF)	±0.01		±0.01		nA typ	V _{DD} = 3.3 V
		±20	±0.1	±0.3	nA max	V _S = 3 V/1 V, V _D = 1 V/3 V;
Drain OFF Leakage I _D (OFF)	±0.01		±0.01		nA typ	Test Circuit 2
		±20	±0.1	±0.75	nA max	V _S = 3 V/1 V, V _D = 1 V/3 V;
Channel ON Leakage I _D , I _S (ON)	±0.01		±0.01		nA typ	Test Circuit 3
		±20	±0.1	±0.75	nA max	V _S = V _D = 1 V or 3 V, Test Circuit 4
DIGITAL INPUTS						
Input High Voltage, V _{INH}		2.0		2.0	V min	
Input Low Voltage, V _{INL}		0.4		0.4	V max	
Input Current						
I _{INL} or I _{INH}	0.005		0.005		μA typ	V _{IN} = V _{INL} or V _{INH}
		±0.1		±0.1	μA max	
C _{IN} , Digital Input Capacitance	2		2		pF typ	
DYNAMIC CHARACTERISTICS²						
t _{TRANSITION}	18		18		ns typ	R _L = 300 Ω, C _L = 35 pF, Test Circuit 5
		30		30	ns max	V _{S1} = 2 V/0 V, V _{S2} = 0 V/2 V
Break-Before-Make Time Delay, t _D	8		8		ns typ	R _L = 300 Ω, C _L = 35 pF
		1		1	ns min	V _S = 2 V, Test Circuit 6
t _{ON} (EN)	18		18		ns typ	R _L = 300 Ω, C _L = 35 pF
		30		30	ns max	V _S = 2 V, Test Circuit 7
t _{OFF} (EN)	8		8		ns typ	R _L = 300 Ω, C _L = 35 pF
		15		15	ns max	V _S = 2 V, Test Circuit 7
Charge Injection	±3		±3		pC typ	V _S = 1.5 V, R _S = 0 Ω, C _L = 1 nF;
						Test Circuit 8
Off Isolation	-60		-60		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz
	-80		-80		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz;
						Test Circuit 9
Channel-to-Channel Crosstalk	-60		-60		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz
	-80		-80		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz;
						Test Circuit 10
-3 dB Bandwidth	55		55		MHz typ	R _L = 50 Ω, C _L = 5 pF, Test Circuit 9
C _S (OFF)	13		13		pF typ	
C _D (OFF)						
ADG708	85		85		pF typ	
ADG709	42		42		pF typ	
C _D , C _S (ON)						
ADG708	96		96		pF typ	
ADG709	48		48		pF typ	
POWER REQUIREMENTS						
I _{DD}	0.001		0.001		μA typ	V _{DD} = 3.3 V
		1.0		1.0	μA max	Digital Inputs = 0 V or 3.3 V

NOTES

¹Temperature ranges are as follows: B and C Versions: -40°C to +85°C.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG708/ADG709—SPECIFICATIONS¹

DUAL SUPPLY ($V_{DD} = +3\text{ V} \pm 10\%$, $V_{SS} = -3\text{ V} \pm 10\%$, $GND = 0\text{ V}$)

Parameter	B Version -40°C +25°C to +85°C		C Version -40°C +25°C to +85°C		Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range	V_{SS} to V_{DD}		V_{SS} to V_{DD}		V	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$; Test Circuit 1
On-Resistance (R_{ON})	2.5		2.5		Ω typ	
	4.5	5	4.5	5	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})		0.4		0.4	Ω typ	$V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$; $V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$
		0.8		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.6		0.6		Ω typ	
		1.0		1.0	Ω max	
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	± 0.01		± 0.01		nA typ	$V_{DD} = +3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$; $V_S = +2.25\text{ V}/-1.25\text{ V}$, $V_D = -1.25\text{ V}/+2.25\text{ V}$; Test Circuit 2
		± 20	± 0.1	± 0.3	nA max	
Drain OFF Leakage I_D (OFF)	± 0.01		± 0.01		nA typ	$V_S = +2.25\text{ V}/-1.25\text{ V}$, $V_D = -1.25\text{ V}/+2.25\text{ V}$; Test Circuit 3
		± 20	± 0.1	± 0.75	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.01		± 0.01		nA typ	$V_S = V_D = +2.25\text{ V}/-1.25\text{ V}$, Test Circuit 4
		± 20	± 0.1	± 0.75	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.0		2.0		V min	$V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}	0.4		0.4		V max	
Input Current I_{INL} or I_{INH}	0.005		0.005		μA typ	
		± 0.1		± 0.1	μA max	
C_{IN} , Digital Input Capacitance	2		2		pF typ	
DYNAMIC CHARACTERISTICS²						
$t_{TRANSITION}$	14		14		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, Test Circuit 5 $V_S = 1.5\text{ V}/0\text{ V}$, Test Circuit 5
		25		25	ns max	
Break-Before-Make Time Delay, t_D	8		8		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$, Test Circuit 6
		1		1	ns min	
$t_{ON(EN)}$	14		14		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$, Test Circuit 7
		25		25	ns max	
$t_{OFF(EN)}$	8		8		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$, Test Circuit 7
		15		15	ns max	
Charge Injection	± 3		± 3		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Test Circuit 8
Off Isolation	-60		-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 9
	-80		-80		dB typ	
Channel-to-Channel Crosstalk	-60		-60		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$ $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Test Circuit 10
	-80		-80		dB typ	
-3 dB Bandwidth	55		55		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, Test Circuit 9
C_S (OFF)	13		13		pF typ	
C_D (OFF)						
ADG708	85		85		pF typ	
ADG709	42		42		pF typ	
C_D , C_S (ON)						
ADG708	96		96		pF typ	
ADG709	48		48		pF typ	
POWER REQUIREMENTS						
I_{DD}	0.001		0.001		μA typ	$V_{DD} = 3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V
		1.0		1.0	μA max	
I_{SS}	0.001		0.001		μA typ	$V_{SS} = -3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V
		1.0		1.0	μA max	

NOTES

¹Temperature range is as follows: B and C Versions: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C unless otherwise noted)

V _{DD} to V _{SS}	7 V
V _{DD} to GND	-0.3 V to +7 V
V _{SS} to GND	+0.3 V to -3.5 V
Analog Inputs ²	V _{SS} - 0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs ²	-0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (B, C Versions)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C

TSSOP Package, Power Dissipation	432 mW
θ _{JA} Thermal Impedance	150.4°C/W
θ _{JC} Thermal Impedance	27.6°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overtolerages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG708/ADG709 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table I. ADG708 Truth Table

A2	A1	A0	EN	Switch Condition
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

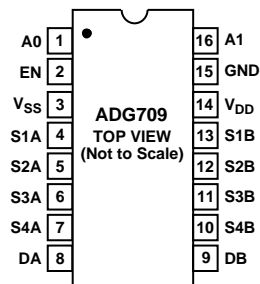
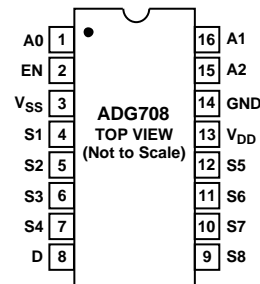
Table II. ADG709 Truth Table

A1	A0	EN	ON Switch Pair
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care.

PIN CONFIGURATIONS

TSSOP



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG708BRU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG709BRU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG708CRU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG709CRU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16

TERMINOLOGY

V_{DD}	Most positive power supply potential.	$t_{ON} (EN)$	Delay time between the 50% and 90% points of the EN digital input and the switch “ON” condition.
V_{SS}	Most negative power supply in a dual supply application. In single supply applications, this should be tied to ground at the device.	$t_{OFF} (EN)$	Delay time between the 50% and 90% points of the EN digital input and the switch “OFF” condition.
GND	Ground (0 V) Reference.	t_{OPEN}	“OFF” time measured between the 80% points of both switches when switching from one address state to another.
S	Source Terminal. May be an input or output.	Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
D	Drain Terminal. May be an input or output.	Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
IN	Logic Control Input.	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
R_{ON}	Ohmic resistance between D and S.	Bandwidth	The frequency at which the output is attenuated by 3 dBs.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.	On Response	The frequency response of the “ON” switch.
$I_S (OFF)$	Source leakage current with the switch “OFF.”	On Loss	The loss due to the ON resistance of the switch.
$I_D (OFF)$	Drain leakage current with the switch “OFF.”	V_{INL}	Maximum input voltage for Logic “0.”
$I_D, I_S (ON)$	Channel leakage current with the switch “ON.”	V_{INH}	Minimum input voltage for Logic “1.”
$V_D (V_S)$	Analog voltage on terminals D, S.	$I_{INL} (I_{INH})$	Input current of the digital input.
$C_S (OFF)$	“OFF” switch source capacitance. Measured with reference to ground.	I_{DD}	Positive Supply Current.
$C_D (OFF)$	“OFF” switch drain capacitance. Measured with reference to ground.	I_{SS}	Negative Supply Current.
$C_D, C_S (ON)$	“ON” switch capacitance. Measured with reference to ground.		
C_{IN}	Digital Input Capacitance.		
$t_{TRANSITION}$	Delay time measured between the 50% and 90% points of the digital inputs and the switch “ON” condition when switching from one address state to another.		

Typical Performance Characteristics—ADG708/ADG709

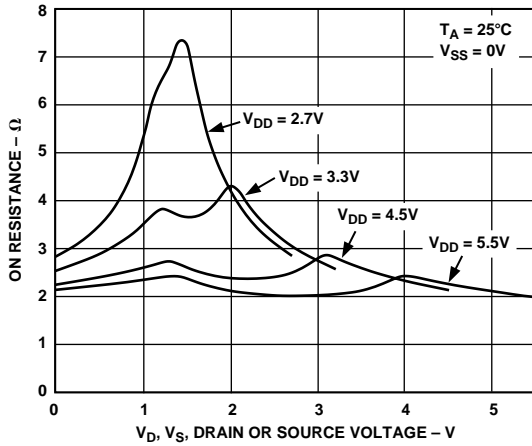


Figure 1. On Resistance as a Function of V_D (V_S) for Single Supply

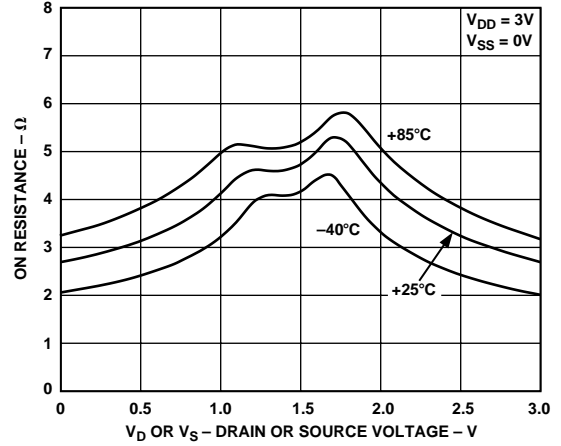


Figure 4. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

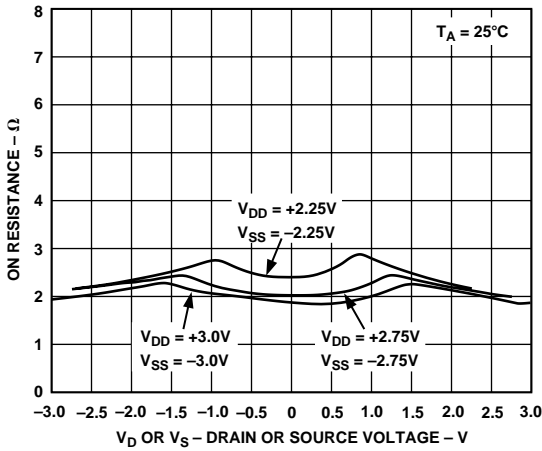


Figure 2. On Resistance as a Function of V_D (V_S) for Dual Supply

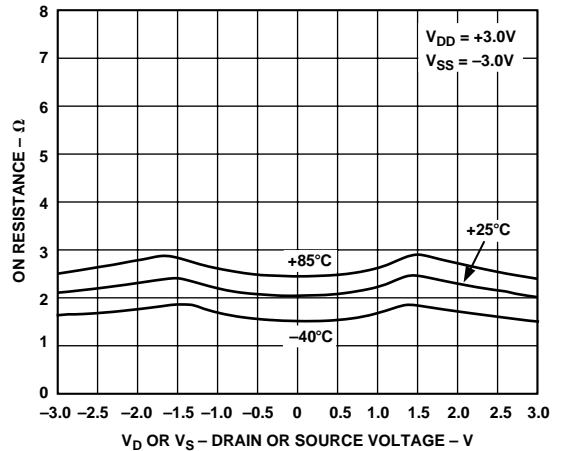


Figure 5. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

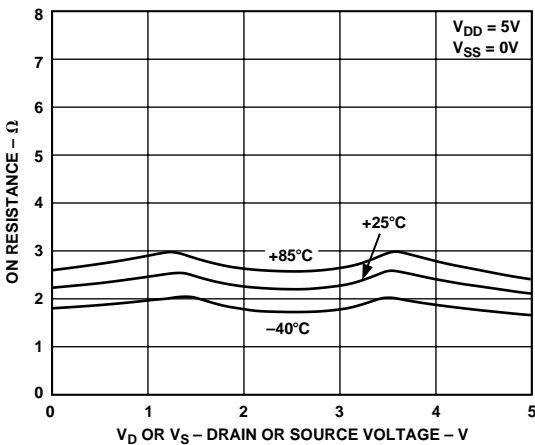


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

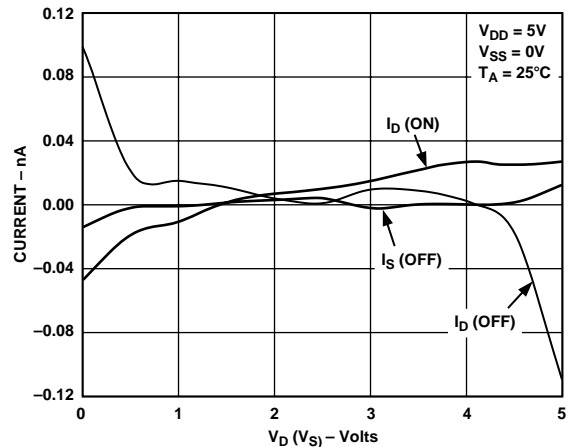


Figure 6. Leakage Currents as a Function of V_D (V_S)

ADG708/ADG709

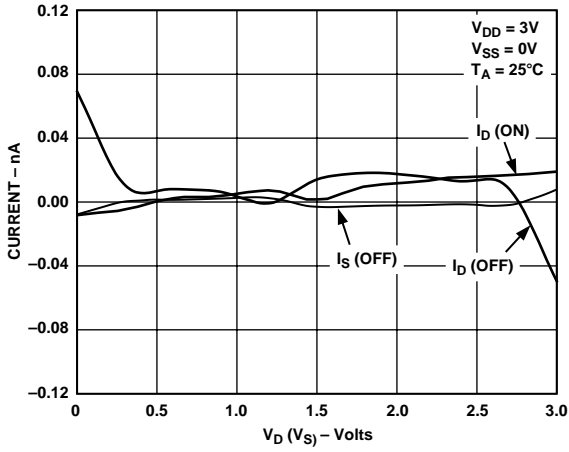


Figure 7. Leakage Currents as a Function of V_D (V_S)

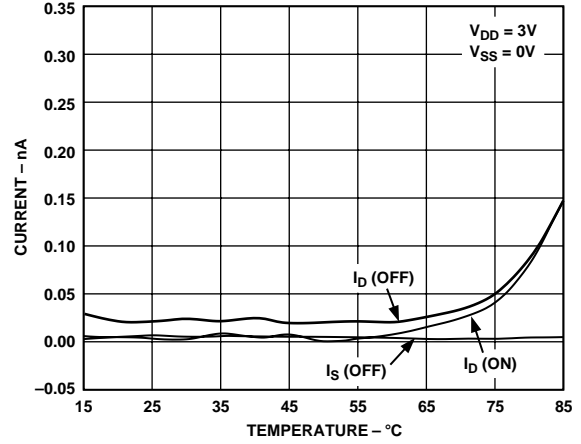


Figure 10. Leakage Currents as a Function of Temperature

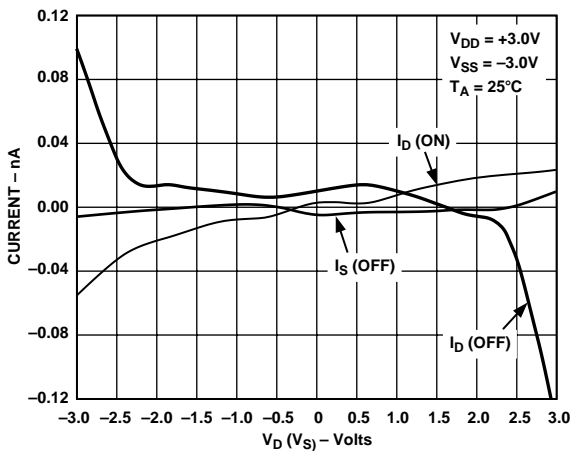


Figure 8. Leakage Currents as a Function of V_D (V_S)

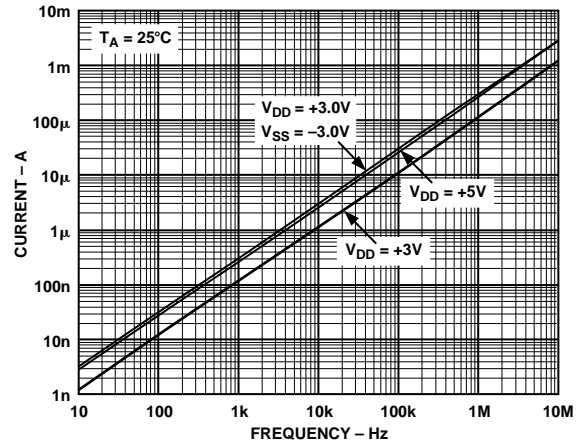


Figure 11. Supply Current vs. Input Switching Frequency

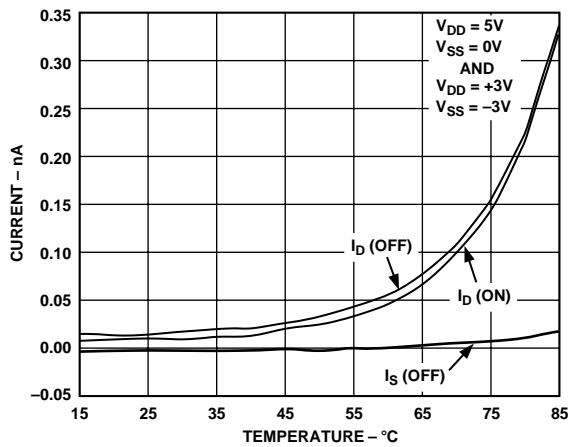


Figure 9. Leakage Currents as a Function of Temperature

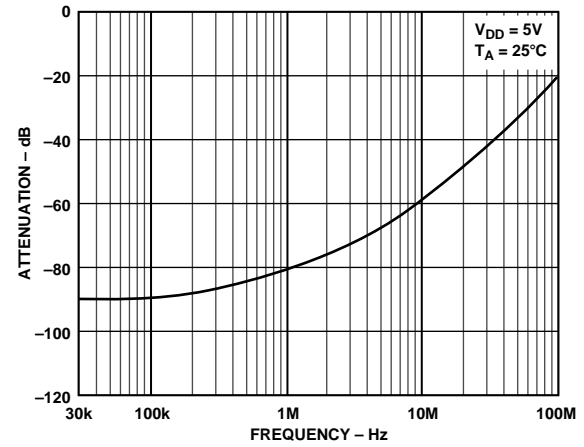


Figure 12. Off Isolation vs. Frequency

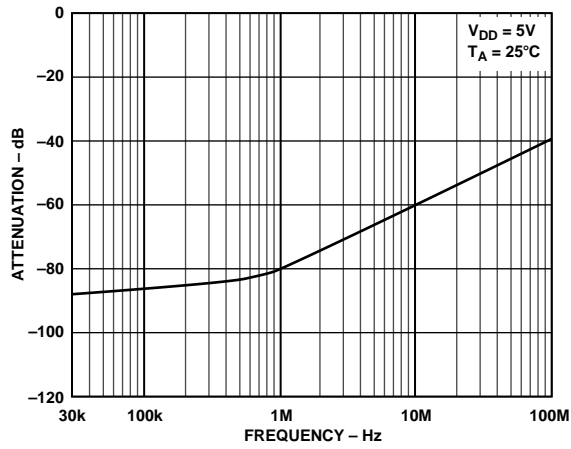


Figure 13. Crosstalk vs. Frequency

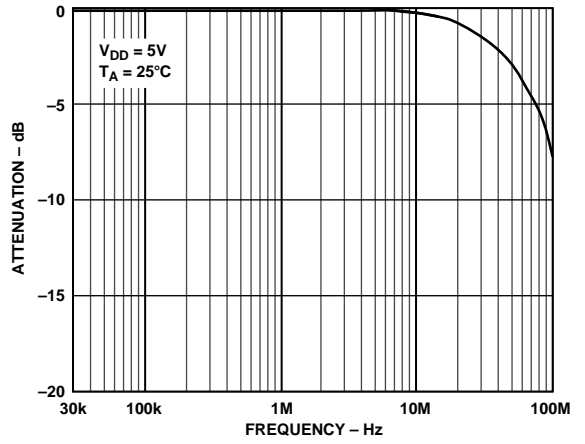


Figure 14. On Response vs. Frequency

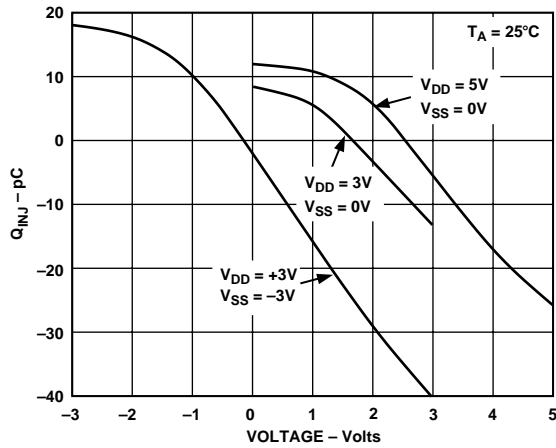
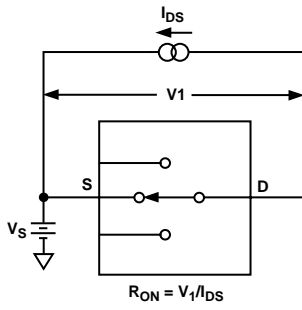


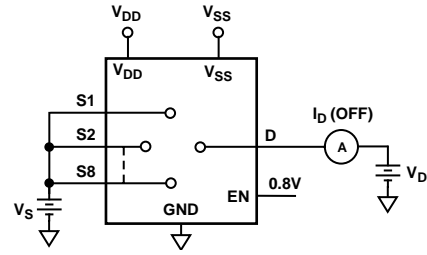
Figure 15. Charge Injection vs. Source Voltage

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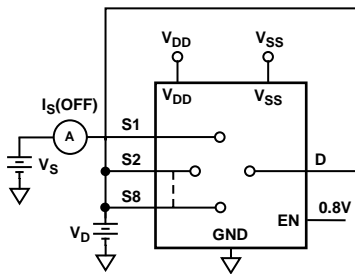
Test Circuits



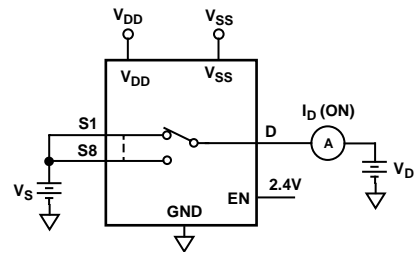
Test Circuit 1. On Resistance



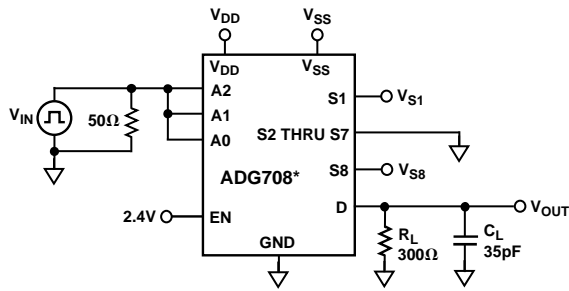
Test Circuit 3. I_D (OFF)



Test Circuit 2. I_S (OFF)

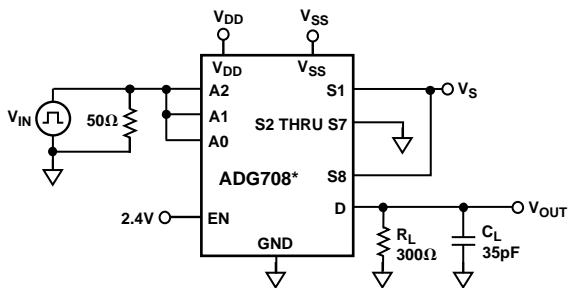
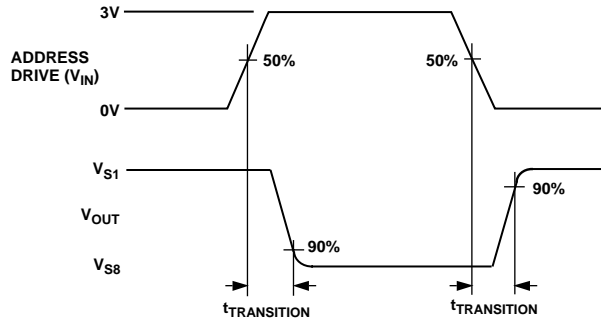


Test Circuit 4. I_D (ON)



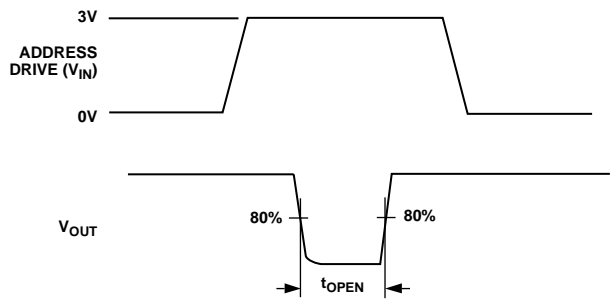
* SIMILAR CONNECTION FOR ADG709

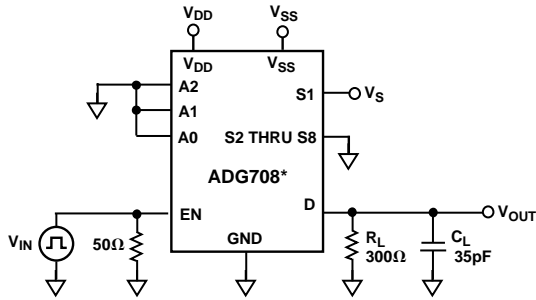
Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$



* SIMILAR CONNECTION FOR ADG709

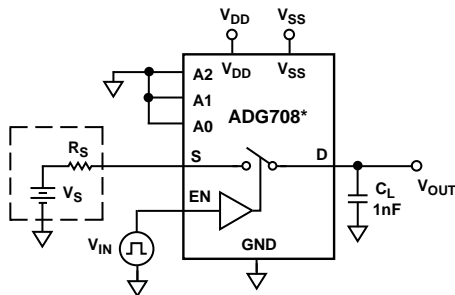
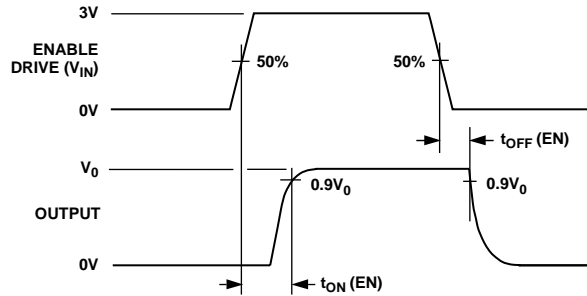
Test Circuit 6. Break-Before-Make Delay, t_{OPEN}





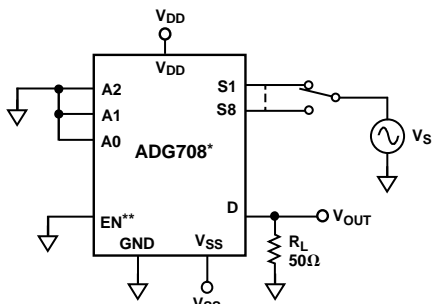
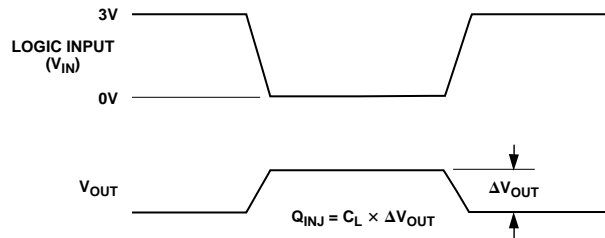
* SIMILAR CONNECTION FOR ADG709

Test Circuit 7. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$



*SIMILAR CONNECTION FOR ADG709

Test Circuit 8. Charge Injection



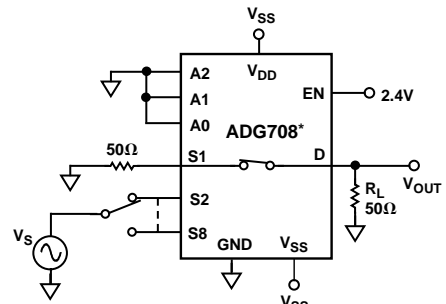
$$\text{OFF ISOLATION} = 20\text{LOG}_{10} \frac{V_{\text{OUT}}}{V_{\text{S}}}$$

$$\text{INSERTION LOSS} = 20\text{LOG}_{10} \left(\frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}} \right)$$

* SIMILAR CONNECTION FOR ADG709

** CONNECT TO 2.4V FOR BANDWIDTH MEASUREMENTS

Test Circuit 9. OFF Isolation and Bandwidth



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20\text{LOG}_{10} \frac{V_{\text{OUT}}}{V_{\text{S}}}$$

* SIMILAR CONNECTION FOR ADG709

Test Circuit 10. Channel-to-Channel Crosstalk

Power-Supply Sequencing

When using CMOS devices, care must be taken to ensure correct power-supply sequencing. Incorrect power-supply sequencing can result in the device being subjected to stresses beyond the maximum ratings listed in the data sheet. Digital and analog inputs should always be applied after power supplies and ground. For single supply operation, V_{SS} should be tied to GND as close to the device as possible.

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OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP (RU-16)

