



# 3.3 V, $\pm 15$ kV ESD-Protected, Half- and Full-Duplex, RS-485/RS-422 Transceivers

ADM3070E/ADM3071E/ADM3072E/ADM3073E/ADM3074E/ADM3075E/ADM3076E/ADM3077E/ADM3078E

## FEATURES

TIA/EIA RS-485/RS-422 compliant

$\pm 15$  kV ESD protection on RS-485 input/output pins

Data rates

ADM3070E/ADM3071E/ADM3072E: 250 kbps

ADM3073E/ADM3074E/ADM3075E: 500 kbps

ADM3076E/ADM3077E/ADM3078E: 16 Mbps

Half- and full-duplex options

True fail-safe receiver inputs

Up to 256 nodes on the bus

$-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature option

Hot-swap input structure on DE and RE pins

Reduced slew rates for low EMI

Low power shutdown current (all except ADM3071E/

ADM3074E/ADM3077E)

Outputs high-Z when disabled or powered off

Common-mode input range:  $-7$  V to  $+12$  V

Thermal shutdown and short-circuit protection

8-lead and 14-lead narrow SOIC packages

## APPLICATIONS

Power/energy metering

Industrial control

Lighting systems

Telecommunications

Security systems

Instrumentation

## GENERAL DESCRIPTION

The ADM307xE are 3.3 V, low power data transceivers with  $\pm 15$  kV ESD protection suitable for full- and half-duplex communication on multipoint bus transmission lines. They are designed for balanced data transmission, and they comply with TIA/EIA standards: RS-485 and RS-422.

The devices have a  $\frac{1}{2}$  unit load receiver input impedance, which allows up to 256 transceivers on a bus. Because only one driver should be enabled at any time, the output of a disabled or powered-down driver is tristated to avoid overloading the bus.

The receiver inputs have a true fail-safe feature, which eliminates the need for external bias resistors and ensures a logic high output level when the inputs are open or shorted. This guarantees that the receiver outputs are in a known state before communication begins and when communication ceases.

## FUNCTIONAL BLOCK DIAGRAMS

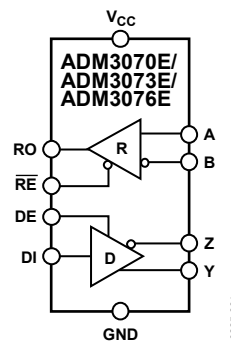


Figure 1.

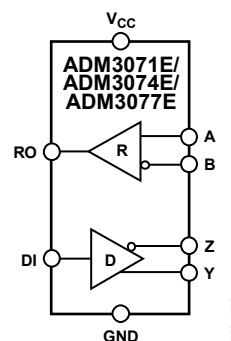


Figure 2.

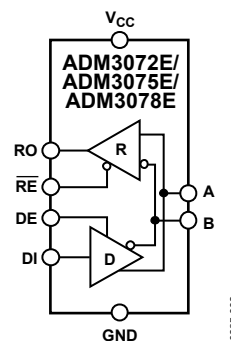


Figure 3.

Rev. E

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## REVISION HISTORY

|                                          |           |
|------------------------------------------|-----------|
| <b>8/09—Rev. D to Rev. E</b>             |           |
| Changes to Ordering Guide .....          | 20        |
| <b>4/09—Rev. C to Rev. D</b>             |           |
| Changes to Ordering Guide .....          | 20        |
| <b>1/09—Rev. B to Rev. C</b>             |           |
| Changes to Ordering Guide .....          | 20        |
| <b>8/08—Rev. A to Rev. B</b>             |           |
| Changes to Table 3 .....                 | 5         |
| Changes to Figure 36 .....               | 18        |
| Updated Outline Dimensions .....         | 19        |
| Changes to Ordering Guide .....          | 20        |
| <b>10/06—Rev. 0 to Rev. A</b>            |           |
| Added ADM3077E and ADM3078E .....        | Universal |
| Changes to Figure 2 and Figure 3 .....   | 1         |
| Changes to Figure 5 and Figure 6 .....   | 9         |
| Changes to Figure 34 and Figure 35 ..... | 17        |
| Updated Outline Dimensions .....         | 19        |
| Changes to Ordering Guide .....          | 20        |
| <b>8/06—Revision 0: Initial Version</b>  |           |

# ADM3070E/ADM3071E/ADM3072E/ADM3073E/ADM3074E/ADM3075E/ADM3076E/ADM3077E/ADM3078E

The driver outputs of the 250 kbps and 500 kbps devices are slew rate limited to reduce EMI and data errors caused by reflections from improperly terminated buses. Excessive power dissipation caused by bus contention or by output shorting is prevented with a thermal shutdown circuit.

The parts are fully specified over the industrial temperature ranges and are available in 8-lead and 14-lead narrow SOIC packages.

**Table 1. Selection Table**

| Part No. | Half/Full Duplex | Data Rate (Mbps) | Slew Rate Limited | Driver/Receiver Enable | Low Power Shutdown | Nodes on Bus | ±15 kV ESD on Bus Pins | Pin Count |
|----------|------------------|------------------|-------------------|------------------------|--------------------|--------------|------------------------|-----------|
| ADM3070E | Full             | 0.25             | Yes               | Yes                    | Yes                | 256          | Yes                    | 14        |
| ADM3071E | Full             | 0.25             | Yes               | No                     | No                 | 256          | Yes                    | 8         |
| ADM3072E | Half             | 0.25             | Yes               | Yes                    | Yes                | 256          | Yes                    | 8         |
| ADM3073E | Full             | 0.5              | Yes               | Yes                    | Yes                | 256          | Yes                    | 14        |
| ADM3074E | Full             | 0.5              | Yes               | No                     | No                 | 256          | Yes                    | 8         |
| ADM3075E | Half             | 0.5              | Yes               | Yes                    | Yes                | 256          | Yes                    | 8         |
| ADM3076E | Full             | 16               | No                | Yes                    | Yes                | 256          | Yes                    | 14        |
| ADM3077E | Full             | 16               | No                | No                     | No                 | 256          | Yes                    | 8         |
| ADM3078E | Half             | 16               | No                | Yes                    | Yes                | 256          | Yes                    | 8         |

# ADM3070E/ADM3071E/ADM3072E/ADM3073E/ADM3074E/ADM3075E/ADM3076E/ADM3077E/ADM3078E

## SPECIFICATIONS

$V_{CC} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

**Table 2.** ADM3070E/ADM3071E/ADM3072E/ADM3073E/ADM3074E/ADM3075E/ADM3076E/ADM3077E/ADM3078E

| Parameter                                                        | Symbol                          | Min                   | Typ                | Max             | Unit | Test Conditions/Comments                                                                |
|------------------------------------------------------------------|---------------------------------|-----------------------|--------------------|-----------------|------|-----------------------------------------------------------------------------------------|
| DRIVER                                                           |                                 |                       |                    |                 |      |                                                                                         |
| Differential Outputs                                             |                                 |                       |                    |                 |      |                                                                                         |
| Differential Output Voltage                                      | V <sub>OD</sub>                 | 2.0<br>1.5            |                    | V <sub>CC</sub> | V    | R <sub>L</sub> = 100 Ω (RS-422) (see Figure 7)                                          |
|                                                                  |                                 |                       |                    | V <sub>CC</sub> | V    | R <sub>L</sub> = 54 Ω (RS-485) (see Figure 7)                                           |
|                                                                  |                                 |                       |                    | V <sub>CC</sub> | V    | No load                                                                                 |
| Δ V <sub>OD</sub>   for Complementary Output States <sup>1</sup> | ΔV <sub>OD</sub>                |                       |                    | 0.2             | V    | R <sub>L</sub> = 54 Ω or 100 Ω (see Figure 7)                                           |
| Common-Mode Output Voltage                                       | V <sub>OC</sub>                 |                       | V <sub>CC</sub> /2 | 3               | V    | R <sub>L</sub> = 54 Ω or 100 Ω (see Figure 7)                                           |
| Δ V <sub>OC</sub>   for Complementary Output States <sup>1</sup> | ΔV <sub>OC</sub>                |                       |                    | 0.2             | V    | R <sub>L</sub> = 54 Ω or 100 Ω (see Figure 7)                                           |
| Short-Circuit Output Current                                     | I <sub>OSD</sub>                | 40                    |                    | 250             | mA   | 0 V < V <sub>OUT</sub> < 12 V                                                           |
|                                                                  |                                 | –250                  |                    | –40             | mA   | –7 V < V <sub>OUT</sub> < V <sub>CC</sub>                                               |
| Short-Circuit Foldback Output Current                            | I <sub>OSDF</sub>               | 20                    |                    |                 | mA   | (V <sub>CC</sub> – 1 V) < V <sub>OUT</sub> < 12 V                                       |
|                                                                  |                                 |                       |                    | –20             | mA   | –7 V < V <sub>OUT</sub> < +1 V                                                          |
| Output Leakage (Y, Z) Full Duplex                                | I <sub>O</sub>                  |                       |                    | 125             | μA   | DE = 0 V, $\overline{RE}$ = 0 V, V <sub>CC</sub> = 0 V or 3.6 V, V <sub>IN</sub> = 12 V |
|                                                                  |                                 | –100                  |                    |                 | μA   | DE = 0 V, $\overline{RE}$ = 0 V, V <sub>CC</sub> = 0 V or 3.6 V, V <sub>IN</sub> = –7 V |
| Logic Inputs                                                     |                                 |                       |                    |                 |      |                                                                                         |
| Input High Voltage                                               | V <sub>IH</sub>                 | 2.0                   |                    |                 | V    | DE, DI, $\overline{RE}$                                                                 |
| Input Low Voltage                                                | V <sub>IL</sub>                 |                       |                    | 0.8             | V    | DE, DI, $\overline{RE}$                                                                 |
| Input Hysteresis                                                 | V <sub>HYS</sub>                |                       | 100                |                 | mV   | DE, DI, $\overline{RE}$                                                                 |
| Logic Input Current                                              | I <sub>IN</sub>                 |                       |                    | ±1              | μA   | DE, DI, $\overline{RE}$                                                                 |
| Input Impedance First Transition                                 |                                 | 1                     |                    | 10              | kΩ   | DE                                                                                      |
| Thermal Shutdown Threshold                                       | T <sub>TS</sub>                 |                       | 175                |                 | °C   |                                                                                         |
| Thermal Shutdown Hysteresis                                      | T <sub>TSH</sub>                |                       | 15                 |                 | °C   |                                                                                         |
| RECEIVER                                                         |                                 |                       |                    |                 |      |                                                                                         |
| Differential Inputs                                              |                                 |                       |                    |                 |      |                                                                                         |
| Differential Input Threshold Voltage                             | V <sub>TH</sub>                 | –200                  | –125               | –50             | mV   | –7 V < V <sub>CM</sub> < +12 V                                                          |
| Input Hysteresis                                                 | ΔV <sub>TH</sub>                |                       | 15                 |                 | mV   | V <sub>A</sub> + V <sub>B</sub> = 0 V                                                   |
| Input Resistance (A, B)                                          | R <sub>IN</sub>                 | 96                    |                    |                 | kΩ   | –7 V < V <sub>CM</sub> < +12 V                                                          |
| Input Current (A, B)                                             | I <sub>A</sub> , I <sub>B</sub> |                       |                    | 125             | μA   | DE = 0 V, V <sub>CC</sub> = 0 V or 3.6 V, V <sub>IN</sub> = 12 V                        |
|                                                                  |                                 | –100                  |                    |                 | μA   | DE = 0 V, V <sub>CC</sub> = 0 V or 3.6 V, V <sub>IN</sub> = –7 V                        |
| RO Logic Output                                                  |                                 |                       |                    |                 |      |                                                                                         |
| Output High Voltage                                              | V <sub>OH</sub>                 | V <sub>CC</sub> – 0.6 |                    |                 | V    | I <sub>OUT</sub> = –1 mA                                                                |
| Output Low Voltage                                               | V <sub>OL</sub>                 |                       |                    | 0.4             | V    | I <sub>OUT</sub> = 1 mA                                                                 |
| Short-Circuit Output Current                                     | I <sub>OSR</sub>                |                       |                    | ±80             | mA   | 0 V < V <sub>RO</sub> < V <sub>CC</sub>                                                 |
| Tristate Output Leakage Current                                  | I <sub>OZR</sub>                |                       |                    | ±1              | μA   | V <sub>CC</sub> = 3.6 V, 0 V < V <sub>OUT</sub> < V <sub>CC</sub>                       |
| POWER SUPPLY                                                     |                                 |                       |                    |                 |      |                                                                                         |
| Supply Current                                                   | I <sub>CC</sub>                 |                       | 0.8                | 1.5             | mA   | No load, DE = V <sub>CC</sub> , $\overline{RE}$ = 0 V                                   |
|                                                                  |                                 |                       | 0.8                | 1.5             | mA   | No load, DE = V <sub>CC</sub> , $\overline{RE}$ = V <sub>CC</sub>                       |
|                                                                  |                                 |                       | 0.8                | 1.5             | mA   | No load, DE = 0 V, $\overline{RE}$ = 0 V                                                |
| Shutdown Current                                                 | I <sub>SHDN</sub>               |                       | 0.05               | 10              | μA   | DE = 0 V, $\overline{RE}$ = V <sub>CC</sub>                                             |
| ESD PROTECTION                                                   |                                 |                       |                    |                 |      |                                                                                         |
| A, B, Y, Z Pins                                                  |                                 |                       | ±15                |                 | kV   | Human body model                                                                        |
| All Pins Except A, B, Y, Z Pins                                  |                                 |                       | ±4                 |                 | kV   | Human body model                                                                        |

<sup>1</sup>  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in  $V_{OD}$  and  $V_{OC}$ , respectively, when the DI input changes state.

# TIMING SPECIFICATIONS—ADM3070E/ADM3071E/ADM3072E

$V_{CC} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 3.

| Parameter                                               | Symbol          | Min | Typ | Max  | Unit | Test Conditions/Comments                                                           |
|---------------------------------------------------------|-----------------|-----|-----|------|------|------------------------------------------------------------------------------------|
| <b>DRIVER</b>                                           |                 |     |     |      |      |                                                                                    |
| Maximum Data Rate                                       |                 | 250 |     |      | kbps |                                                                                    |
| Propagation Delay, Low-to-High Level                    | $t_{DPLH}$      | 250 |     | 1500 | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9)              |
| Propagation Delay, High-to-Low Level                    | $t_{DPHL}$      | 250 |     | 1500 | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9)              |
| Rise Time/Fall Time                                     | $t_{DR}/t_{DF}$ | 350 |     | 1600 | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9)              |
| $ t_{DPLH} - t_{DPHL} $ Differential Driver Output Skew | $t_{DSKEW}$     |     |     | 200  | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9) <sup>1</sup> |
| Enable to Output High                                   | $t_{DZH}$       |     |     | 2500 | ns   | See Figure 10                                                                      |
| Enable to Output Low                                    | $t_{DZL}$       |     |     | 2500 | ns   | See Figure 11                                                                      |
| Disable Time from Low                                   | $t_{DLZ}$       |     |     | 100  | ns   | See Figure 11                                                                      |
| Disable Time from High                                  | $t_{DHZ}$       |     |     | 100  | ns   | See Figure 10                                                                      |
| Enable Time from Shutdown to High                       | $t_{DZH}(SHDN)$ |     |     | 5500 | ns   | See Figure 10                                                                      |
| Enable Time from Shutdown to Low                        | $t_{DZL}(SHDN)$ |     |     | 5500 | ns   | See Figure 11                                                                      |
| <b>RECEIVER</b>                                         |                 |     |     |      |      |                                                                                    |
| Maximum Data Rate                                       |                 | 250 |     |      | kbps |                                                                                    |
| Propagation Delay, Low-to-High Level                    | $t_{RPLH}$      |     |     | 200  | ns   | $C_L = 15 \text{ pF}$ (see Figure 12 and Figure 13)                                |
| Propagation Delay, High-to-Low Level                    | $t_{RPHL}$      |     |     | 200  | ns   | $C_L = 15 \text{ pF}$ (see Figure 12 and Figure 13)                                |
| $ t_{RPLH} - t_{RPHL} $ Output Skew                     | $t_{RSKEW}$     |     |     | 30   | ns   | $C_L = 15 \text{ pF}$ (see Figure 12 and Figure 13)                                |
| Enable to Output High                                   | $t_{RZH}$       |     |     | 50   | ns   | See Figure 14                                                                      |
| Enable to Output Low                                    | $t_{RZL}$       |     |     | 50   | ns   | See Figure 14                                                                      |
| Disable Time from Low                                   | $t_{RLZ}$       |     |     | 50   | ns   | See Figure 14                                                                      |
| Disable Time from High                                  | $t_{RHZ}$       |     |     | 50   | ns   | See Figure 14                                                                      |
| Enable Time from Shutdown to High                       | $t_{RZH}(SHDN)$ |     |     | 4000 | ns   | See Figure 14                                                                      |
| Enable Time from Shutdown to Low                        | $t_{RZL}(SHDN)$ |     |     | 4000 | ns   | See Figure 14                                                                      |
| TIME TO SHUTDOWN                                        | $t_{SHDN}$      | 50  | 200 | 600  | ns   |                                                                                    |

<sup>1</sup>  $V_{CC} = 3.3 \text{ V}$ .

# ADM3070E/ADM3071E/ADM3072E/ADM3073E/ADM3074E/ADM3075E/ADM3076E/ADM3077E/ADM3078E

## TIMING SPECIFICATIONS—ADM3073E/ADM3074E/ADM3075E

$V_{CC} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 4.

| Parameter                                               | Symbol          | Min | Typ | Max  | Unit | Test Conditions/Comments                                              |
|---------------------------------------------------------|-----------------|-----|-----|------|------|-----------------------------------------------------------------------|
| <b>DRIVER</b>                                           |                 |     |     |      |      |                                                                       |
| Maximum Data Rate                                       |                 | 500 |     |      | kbps |                                                                       |
| Propagation Delay, Low-to-High Level                    | $t_{DPLH}$      | 180 |     | 800  | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9) |
| Propagation Delay, High-to-Low Level                    | $t_{DPLH}$      | 180 |     | 800  | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9) |
| Rise Time/Fall Time                                     | $t_{DR}/t_{DF}$ | 200 |     | 800  | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9) |
| $ t_{DPLH} - t_{DPLH} $ Differential Driver Output Skew | $t_{DSKEW}$     |     |     | 100  | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9) |
| Enable to Output High                                   | $t_{DZH}$       |     |     | 2500 | ns   | See Figure 10                                                         |
| Enable to Output Low                                    | $t_{DZL}$       |     |     | 2500 | ns   | See Figure 11                                                         |
| Disable Time from Low                                   | $t_{DLZ}$       |     |     | 100  | ns   | See Figure 11                                                         |
| Disable Time from High                                  | $t_{DHZ}$       |     |     | 100  | ns   | See Figure 10                                                         |
| Enable Time from Shutdown to High                       | $t_{DZH}(SHDN)$ |     |     | 4500 | ns   | See Figure 10                                                         |
| Enable Time from Shutdown to Low                        | $t_{DZL}(SHDN)$ |     |     | 4500 | ns   | See Figure 11                                                         |
| <b>RECEIVER</b>                                         |                 |     |     |      |      |                                                                       |
| Maximum Data Rate                                       |                 | 500 |     |      | kbps |                                                                       |
| Propagation Delay, Low-to-High Level                    | $t_{RPLH}$      |     |     | 200  | ns   | $C_L = 15 \text{ pF}$ (see Figure 12 and Figure 13)                   |
| Propagation Delay, High-to-Low Level                    | $t_{RPHL}$      |     |     | 200  | ns   | $C_L = 15 \text{ pF}$ (see Figure 12 and Figure 13)                   |
| $ t_{RPLH} - t_{RPHL} $ Output Skew                     | $t_{RSKEW}$     |     |     | 30   | ns   | $C_L = 15 \text{ pF}$ (see Figure 12 and Figure 13)                   |
| Enable to Output High                                   | $t_{RZH}$       |     |     | 50   | ns   | See Figure 14                                                         |
| Enable to Output Low                                    | $t_{RZL}$       |     |     | 50   | ns   | See Figure 14                                                         |
| Disable Time from Low                                   | $t_{RLZ}$       |     |     | 50   | ns   | See Figure 14                                                         |
| Disable Time from High                                  | $t_{RHZ}$       |     |     | 50   | ns   | See Figure 14                                                         |
| Enable Time from Shutdown to High                       | $t_{RZH}(SHDN)$ |     |     | 4000 | ns   | See Figure 14                                                         |
| Enable Time from Shutdown to Low                        | $t_{RZL}(SHDN)$ |     |     | 4000 | ns   | See Figure 14                                                         |
| TIME TO SHUTDOWN                                        | $t_{SHDN}$      | 50  | 200 | 600  | ns   |                                                                       |

# TIMING SPECIFICATIONS—ADM3076E/ADM3077E/ADM3078E

$V_{CC} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 5.

| Parameter                                               | Symbol          | Min | Typ  | Max  | Unit | Test Conditions/Comments                                              |
|---------------------------------------------------------|-----------------|-----|------|------|------|-----------------------------------------------------------------------|
| <b>DRIVER</b>                                           |                 |     |      |      |      |                                                                       |
| Maximum Data Rate                                       |                 | 16  |      |      | Mbps |                                                                       |
| Propagation Delay, Low-to-High Level                    | $t_{DPLH}$      |     |      | 50   | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9) |
| Propagation Delay, High-to-Low Level                    | $t_{DPLH}$      |     |      | 50   | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9) |
| Rise Time/Fall Time                                     | $t_{DR}/t_{DF}$ |     |      | 15   | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9) |
| $ t_{DPLH} - t_{DPLH} $ Differential Driver Output Skew | $t_{DSKEW}$     |     |      | 8    | ns   | $C_L = 50 \text{ pF}$ , $R_L = 54 \Omega$ (see Figure 8 and Figure 9) |
| Enable to Output High                                   | $t_{DZH}$       |     |      | 150  | ns   | See Figure 10                                                         |
| Enable to Output Low                                    | $t_{DZL}$       |     |      | 150  | ns   | See Figure 11                                                         |
| Disable Time from Low                                   | $t_{DLZ}$       |     |      | 100  | ns   | See Figure 11                                                         |
| Disable Time from High                                  | $t_{DZH}$       |     |      | 100  | ns   | See Figure 10                                                         |
| Enable Time from Shutdown to High                       | $t_{DZH(SHDN)}$ |     | 1250 | 1800 | ns   | See Figure 10                                                         |
| Enable Time from Shutdown to Low                        | $t_{DZL(SHDN)}$ |     | 1250 | 1800 | ns   | See Figure 11                                                         |
| <b>RECEIVER</b>                                         |                 |     |      |      |      |                                                                       |
| Maximum Data Rate                                       |                 | 16  |      |      | Mbps |                                                                       |
| Propagation Delay, Low-to-High Level                    | $t_{RPLH}$      |     | 40   | 75   | ns   | $C_L = 15 \text{ pF}$ (see Figure 12 and Figure 13)                   |
| Propagation Delay, High-to-Low Level                    | $t_{RPHL}$      |     | 40   | 75   | ns   | $C_L = 15 \text{ pF}$ (see Figure 12 and Figure 13)                   |
| $ t_{RPLH} - t_{RPHL} $ Output Skew                     | $t_{RSKEW}$     |     |      | 8    | ns   | $C_L = 15 \text{ pF}$ (see Figure 12 and Figure 13)                   |
| Enable to Output High                                   | $t_{RZH}$       |     |      | 50   | ns   | See Figure 14                                                         |
| Enable to Output Low                                    | $t_{RZL}$       |     |      | 50   | ns   | See Figure 14                                                         |
| Disable Time from Low                                   | $t_{RLZ}$       |     |      | 50   | ns   | See Figure 14                                                         |
| Disable Time from High                                  | $t_{RHZ}$       |     |      | 50   | ns   | See Figure 14                                                         |
| Enable Time from Shutdown to High                       | $t_{RZH(SHDN)}$ |     |      | 1800 | ns   | See Figure 14                                                         |
| Enable Time from Shutdown to Low                        | $t_{RZL(SHDN)}$ |     |      | 1800 | ns   | See Figure 14                                                         |
| TIME TO SHUTDOWN                                        | $t_{SHDN}$      | 50  | 200  | 600  | ns   |                                                                       |

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 6.**

| Parameter                                                | Rating                        |
|----------------------------------------------------------|-------------------------------|
| $V_{CC}$ to GND                                          | –0.3 V to +6 V                |
| Digital Input/Output Voltage (DE, $\overline{RE}$ , DI)  | –0.3 V to +6 V                |
| Receiver Output Voltage (RO)                             | –0.3 V to ( $V_{CC} + 0.3$ V) |
| Driver Output (A, B, Y, Z)/Receiver Input (A, B) Voltage | –8 V to +13 V                 |
| Driver Output Current                                    | $\pm 250$ mA                  |
| Operating Temperature Range                              |                               |
| ADM307xEA                                                | –40°C to +85°C                |
| ADM307xEY                                                | –40°C to +125°C               |
| Storage Temperature Range                                | –65°C to +150°C               |
| $\theta_{JA}$ Thermal Impedance                          |                               |
| 8-Lead SOIC_N                                            | 158°C/W                       |
| 14-Lead SOIC_N                                           | 120°C/W                       |
| Lead Temperature, Soldering (20 sec)                     | 260°C                         |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



#### **ESD (electrostatic discharge) sensitive device.**

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

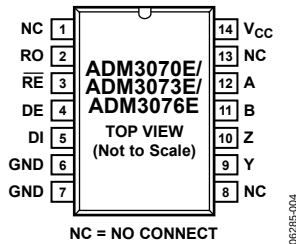


Figure 4. ADM3070E/ADM3073E/ADM3076E Pin Configuration

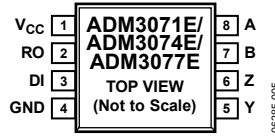


Figure 5. ADM3071E/ADM3074E/ADM3077E Pin Configuration

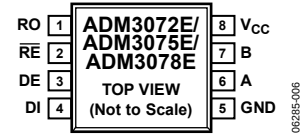


Figure 6. ADM3072E/ADM3075E/ADM3078E Pin Configuration

Table 7. Pin Function Descriptions

| ADM3070E/<br>ADM3073E/<br>ADM3076E<br>Pin No. | ADM3071E/<br>ADM3074E/<br>ADM3077E<br>Pin No. | ADM3072E/<br>ADM3075E/<br>ADM3078E<br>Pin No. | Mnemonic               | Description                                                                                                                                                                                                                                                                                         |
|-----------------------------------------------|-----------------------------------------------|-----------------------------------------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2                                             | 2                                             | 1                                             | RO                     | Receiver Output. When enabled, if $(A - B) \geq -50$ mV, RO is high. If $(A - B) \leq -200$ mV, RO is low.                                                                                                                                                                                          |
| 3                                             | N/A                                           | 2                                             | $\overline{\text{RE}}$ | Receiver Output Enable. A low level enables the receiver output. A high level places it in a high impedance state. If RE is high and DE is low, the device enters a low power shutdown mode.                                                                                                        |
| 4                                             | N/A                                           | 3                                             | DE                     | Driver Output Enable. A high level enables the driver differential A and B outputs. A low level places it in a high impedance state. If RE is high and DE is low, the device enters a low power shutdown mode.                                                                                      |
| 5                                             | 3                                             | 4                                             | DI                     | Driver Input. With a half-duplex part when the driver is enabled, a logic low on DI forces A low and B high; a logic high on DI forces A high and B low. With a full-duplex part when the driver is enabled, a logic low on DI forces Y low and Z high; a logic high on DI forces Y high and Z low. |
| 6, 7                                          | 4                                             | 5                                             | GND                    | Ground.                                                                                                                                                                                                                                                                                             |
| 9                                             | 5                                             | N/A                                           | Y                      | Noninverting Driver Output.                                                                                                                                                                                                                                                                         |
| N/A                                           | N/A                                           | 6                                             | A                      | Noninverting Receiver Input A and Noninverting Driver Output A.                                                                                                                                                                                                                                     |
| 12                                            | 8                                             | N/A                                           | A                      | Noninverting Receiver Input A.                                                                                                                                                                                                                                                                      |
| 10                                            | 6                                             | N/A                                           | Z                      | Inverting Driver Output.                                                                                                                                                                                                                                                                            |
| N/A                                           | N/A                                           | 7                                             | B                      | Inverting Receiver Input B and Inverting Driver Output B.                                                                                                                                                                                                                                           |
| 11                                            | 7                                             | N/A                                           | B                      | Inverting Receiver Input B.                                                                                                                                                                                                                                                                         |
| 14                                            | 1                                             | 8                                             | V <sub>CC</sub>        | Power Supply, 3.3 V $\pm$ 10%. Bypass V <sub>CC</sub> to GND with a 0.1 $\mu$ F capacitor.                                                                                                                                                                                                          |
| 1, 8, 13                                      | N/A                                           | N/A                                           | NC                     | No Connect. Not internally connected; can be connected to GND.                                                                                                                                                                                                                                      |

## TEST CIRCUITS AND SWITCHING CHARACTERISTICS

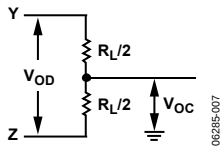


Figure 7. Driver DC Test Load

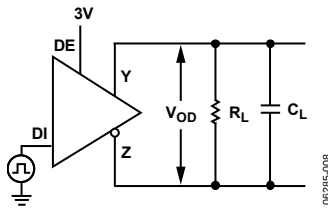


Figure 8. Driver Timing Test Circuit

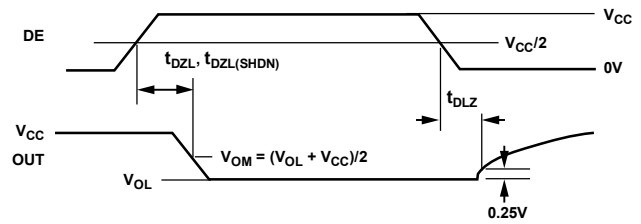
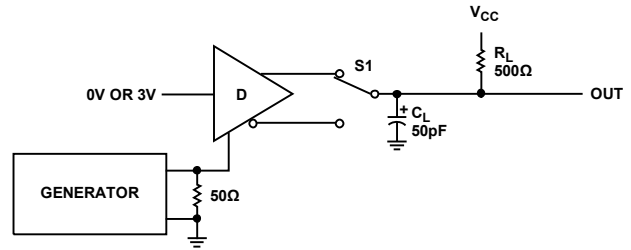


Figure 11. Driver Enable and Disable Times ( $t_{DZL}$ ,  $t_{DZL(SHDN)}$ ,  $t_{DLZ}$ )

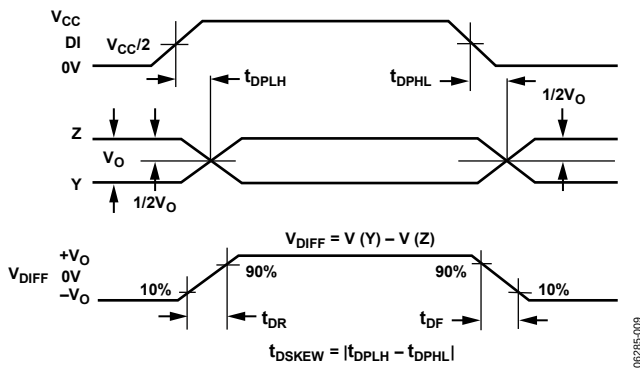


Figure 9. Driver Propagation Delays

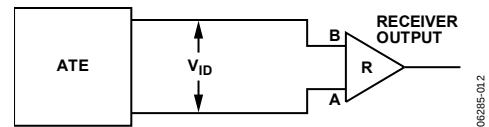


Figure 12. Receiver Propagation Delay Test Circuit

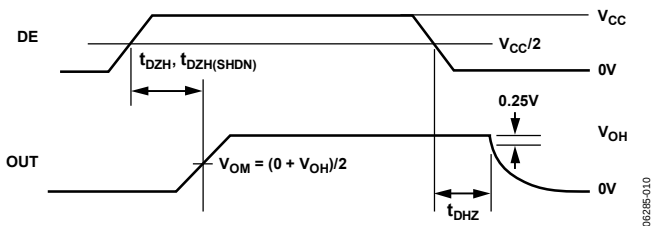
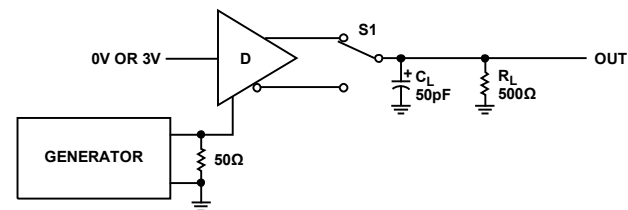
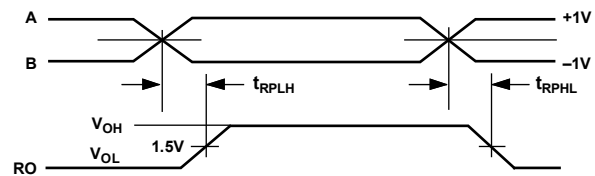


Figure 10. Driver Enable and Disable Times ( $t_{DZH}$ ,  $t_{DZH(SHDN)}$ ,  $t_{DHZ}$ )



NOTES  
1. THE RISE TIME AND FALL TIME OF INPUT A AND INPUT B < 4ns.

Figure 13. Receiver Propagation Delays

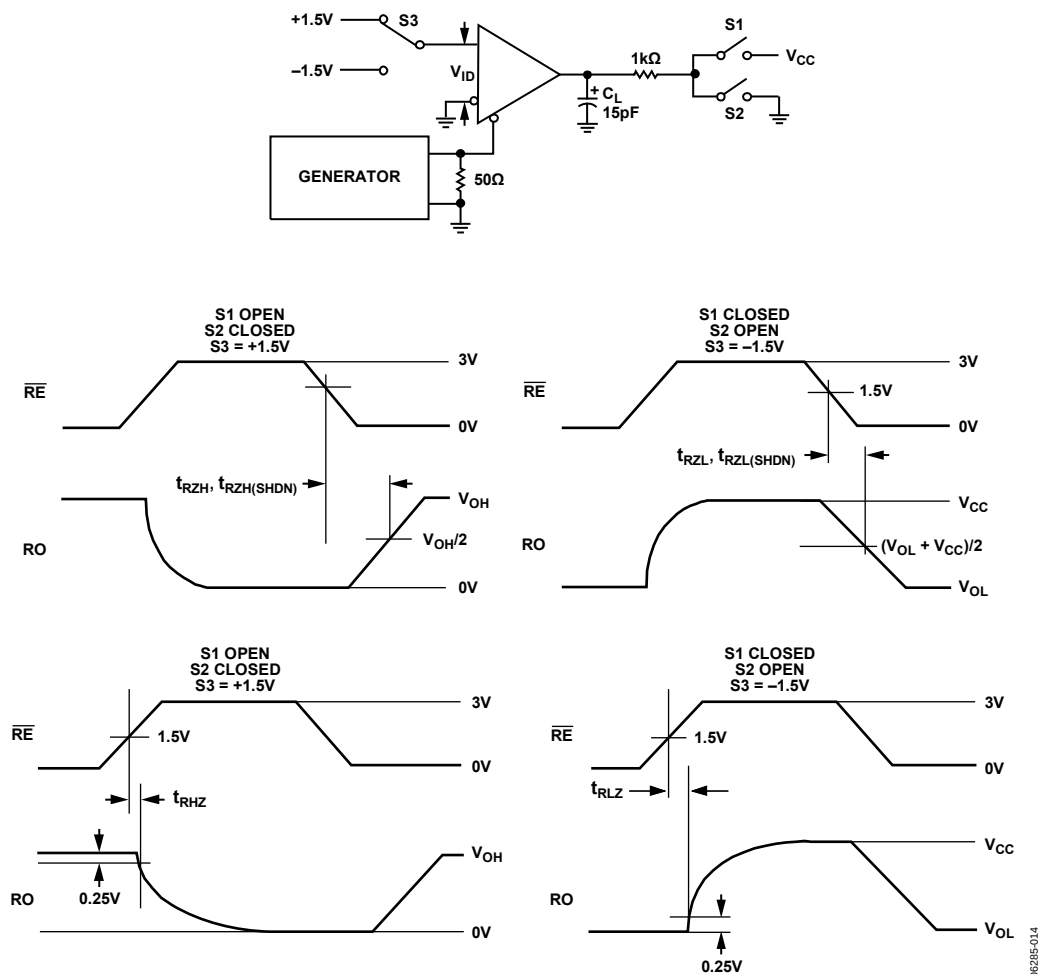


Figure 14. Receiver Enable and Disable Times

00285-014

## TYPICAL PERFORMANCE CHARACTERISTICS

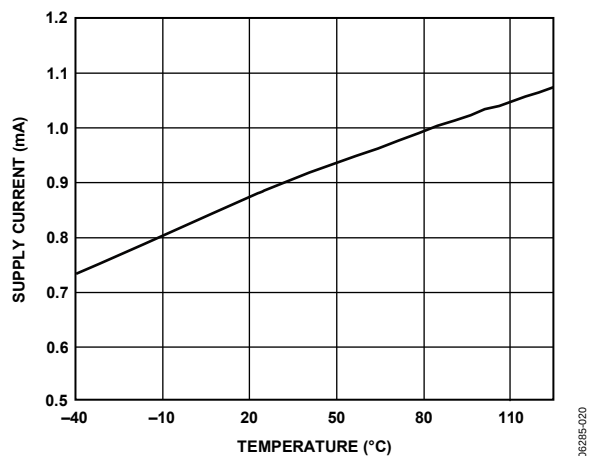


Figure 15. Supply Current vs. Temperature

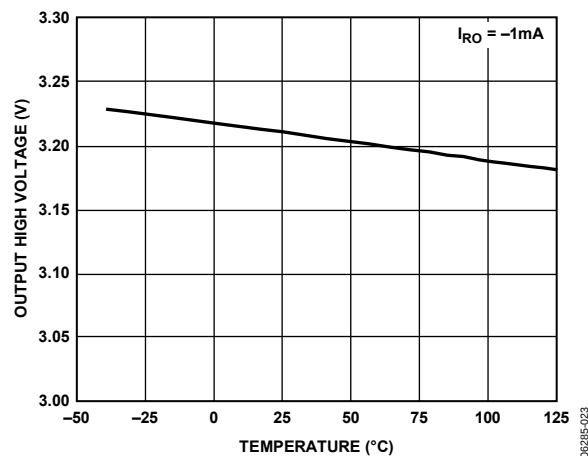


Figure 18. Receiver Output High Voltage vs. Temperature

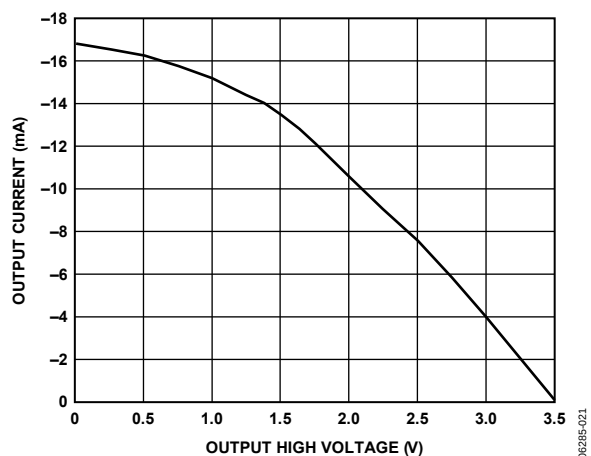


Figure 16. Output Current vs. Receiver Output High Voltage

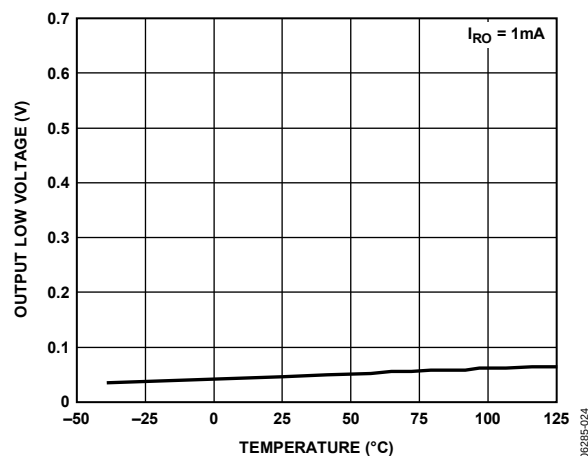


Figure 19. Receiver Output Low Voltage vs. Temperature

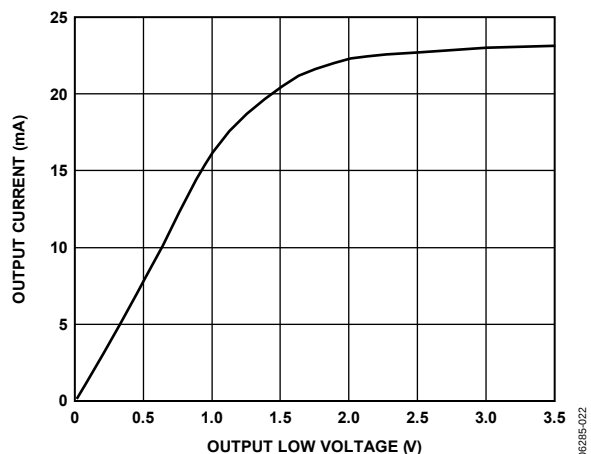


Figure 17. Output Current vs. Receiver Output Low Voltage

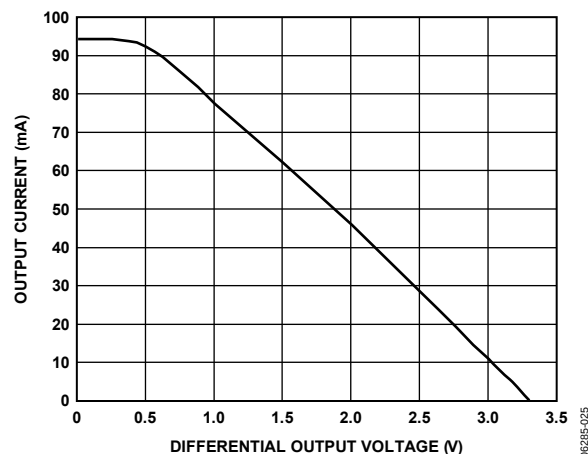


Figure 20. Driver Output Current vs. Differential Output Voltage

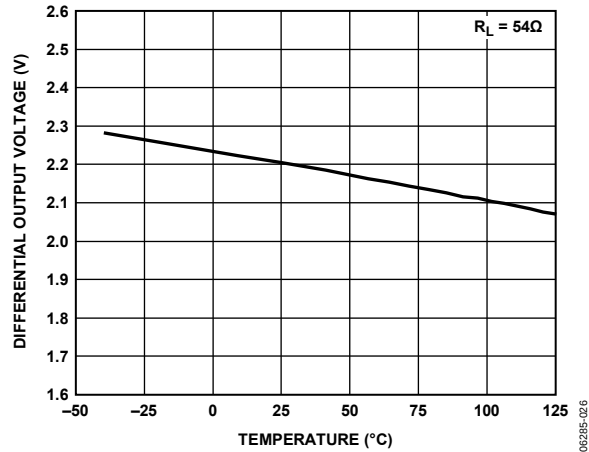


Figure 21. Driver Differential Output Voltage vs. Temperature

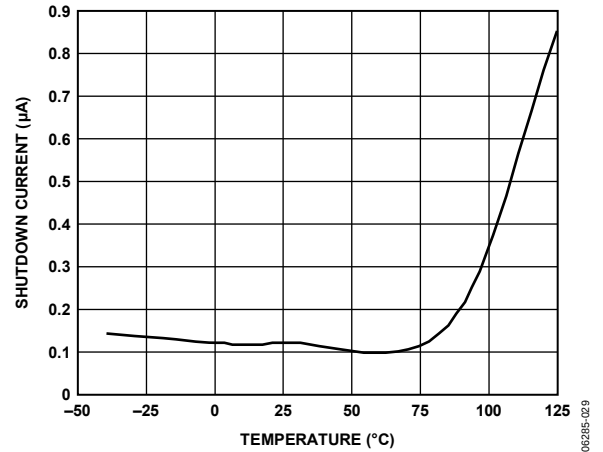


Figure 24. Shutdown Current vs. Temperature

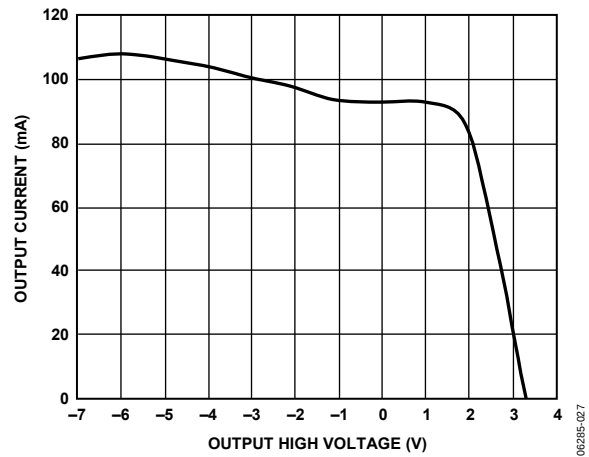


Figure 22. Output Current vs. Driver Output High Voltage

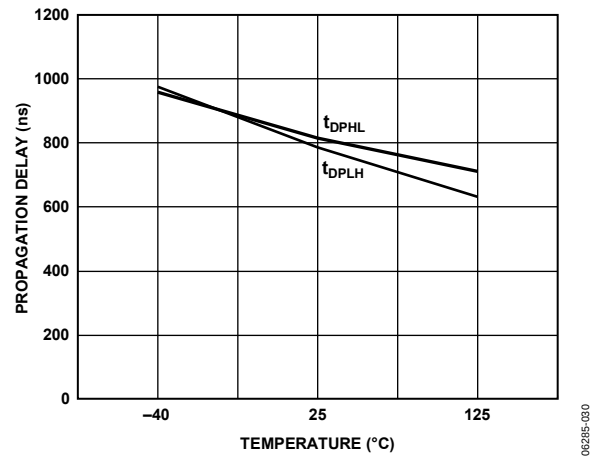


Figure 25. ADM3070E/ADM3071E/ADM3072E Driver Propagation Delay vs. Temperature (250 kbps)

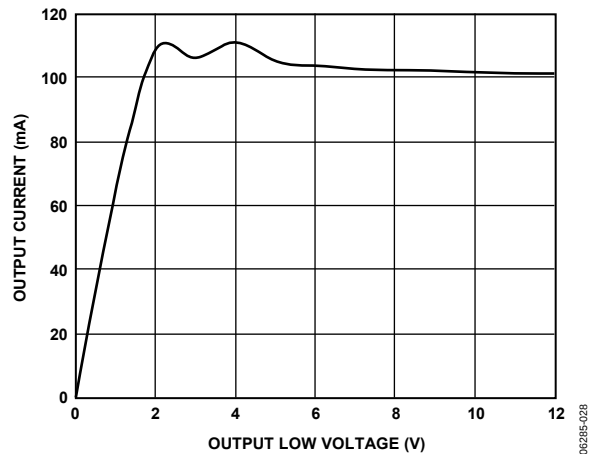


Figure 23. Output Current vs. Driver Output Low Voltage

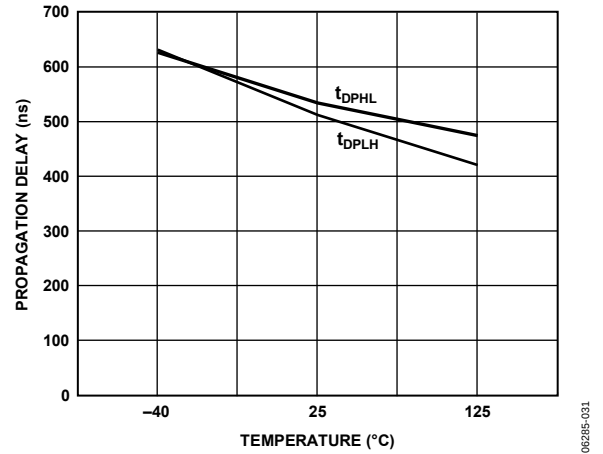


Figure 26. ADM3073E/ADM3074E/ADM3075E Driver Propagation Delay vs. Temperature (500 kbps)

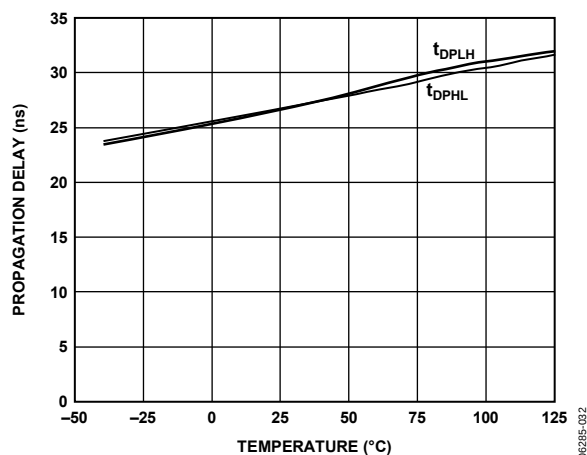


Figure 27. ADM3076E/ADM3077E/ADM3078E Driver Propagation Delay vs. Temperature (16 Mbps)

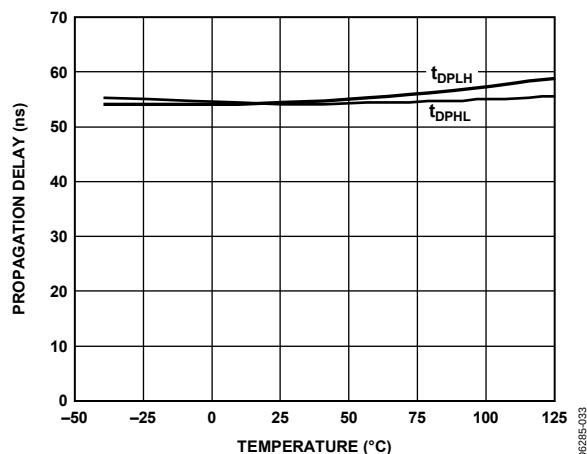


Figure 28. Receiver Propagation Delay vs. Temperature

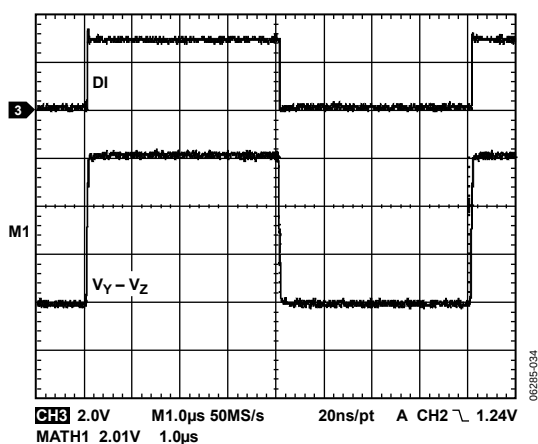


Figure 29. ADM3070E/ADM3071E/ADM3072E Driver Propagation Delay (250 kbps)

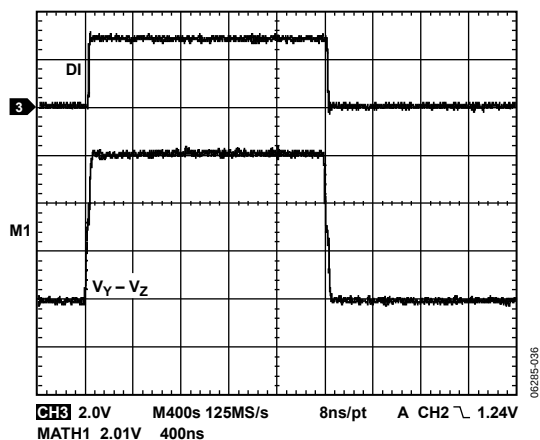


Figure 30. ADM3073E/ADM3074E/ADM3075E Driver Propagation Delay (500 kbps)

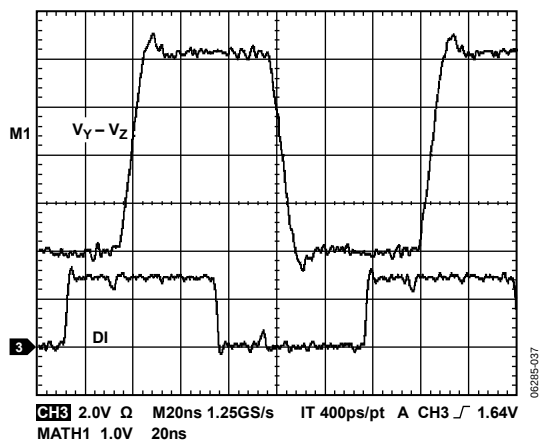


Figure 31. ADM3076E/ADM3077E/ADM3078E Driver Propagation Delay (16 Mbps)

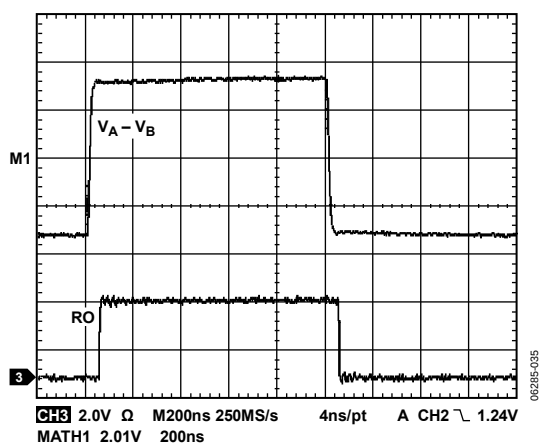


Figure 32. Receiver Propagation Delay

## CIRCUIT DESCRIPTION

The ADM307xE series are high speed transceivers for RS-485 and RS-422 communications. Each device contains one driver and one receiver. All devices feature fail-safe circuitry, which guarantees a logic high receiver output when the receiver inputs are open or shorted or when they are connected to a terminated transmission line with all drivers disabled (see the Receiver Fail-Safe section). The ADM307xE also feature a hot-swap capability, allowing line insertion without erroneous data transfer (see the Hot-Swap Capability section). The ADM3070E/ADM3071E/ADM3072E feature reduced slew rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing for error-free data transmission at rates up to 250 kbps.

The ADM3073E/ADM3074E/ADM3075E also offer slew rate limits, allowing transmit speeds up to 500 kbps. The ADM3076E/ADM3077E/ADM3078E driver slew rates are not limited, making possible transmit speeds of up to 16 Mbps. The ADM3072E/ADM3075E/ADM3078E are half-duplex transceivers; the ADM3070E/ADM3071E/ADM3073E/ADM3074E/ADM3076E/ADM3077E are each full-duplex transceivers. All devices operate from a single 3.3 V supply. Drivers are output short-circuit current limited, and thermal shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal shutdown circuitry places the driver outputs into a high impedance state.

## FUNCTION TABLES

### ADM3070E/ADM3073E/ADM3076E

Table 8. Transmitting Truth Table

| Transmitting Inputs |    |                | Transmitting Outputs |                     |
|---------------------|----|----------------|----------------------|---------------------|
| RE                  | DE | DI             | Y                    | Z                   |
| X <sup>1</sup>      | 1  | 1              | 1                    | 0                   |
| X <sup>1</sup>      | 1  | 0              | 0                    | 1                   |
| 0                   | 0  | X <sup>1</sup> | High-Z <sup>2</sup>  | High-Z <sup>2</sup> |
| 1                   | 0  | X <sup>1</sup> | Shutdown             | Shutdown            |

<sup>1</sup> X = don't care.

<sup>2</sup> High-Z = high impedance.

Table 9. Receiving Truth Table

| Receiving Inputs |                | Receiving Outputs |                     |
|------------------|----------------|-------------------|---------------------|
| RE               | DE             | A – B             | RO                  |
| 0                | X <sup>1</sup> | ≥ –50 mV          | 1                   |
| 0                | X <sup>1</sup> | ≤ –200 mV         | 0                   |
| 0                | X <sup>1</sup> | Open/shorted      | 1                   |
| 1                | 1              | X <sup>1</sup>    | High-Z <sup>2</sup> |
| 1                | 0              | X <sup>1</sup>    | Shutdown            |

<sup>1</sup> X = don't care.

<sup>2</sup> High-Z = high impedance.

### ADM3071E/ADM3074E/ADM3077E

Table 10. Transmitting Truth Table

| Transmitting Input | Transmitting Outputs |   |
|--------------------|----------------------|---|
| DI                 | Y                    | Z |
| 1                  | 1                    | 0 |
| 0                  | 0                    | 1 |

Table 11. Receiving Truth Table

| Receiving Input | Receiving Output |
|-----------------|------------------|
| A – B           | RO               |
| ≥ –50 mV        | 1                |
| ≤ –200 mV       | 0                |
| Open/shorted    | 1                |

### ADM3072E/ADM3075E/ADM3078E

Table 12. Transmitting Truth Table

| Transmitting Inputs |    |                | Transmitting Outputs |                     |
|---------------------|----|----------------|----------------------|---------------------|
| RE                  | DE | DI             | A, Y                 | B, Z                |
| X <sup>1</sup>      | 1  | 1              | 1                    | 0                   |
| X <sup>1</sup>      | 1  | 0              | 0                    | 1                   |
| 0                   | 0  | X <sup>1</sup> | High-Z <sup>2</sup>  | High-Z <sup>2</sup> |
| 1                   | 0  | X <sup>1</sup> | Shutdown             | Shutdown            |

<sup>1</sup> X = don't care.

<sup>2</sup> High-Z = high impedance.

Table 13. Receiving Truth Table

| Receiving Inputs |    |                | Receiving Output    |
|------------------|----|----------------|---------------------|
| RE               | DE | A – B          | RO                  |
| 0                | 0  | ≥ –50 mV       | 1                   |
| 0                | 0  | ≤ –200 mV      | 0                   |
| 0                | 0  | Open/shorted   | 1                   |
| 1                | 1  | X <sup>1</sup> | High-Z <sup>2</sup> |
| 1                | 0  | X <sup>1</sup> | Shutdown            |

<sup>1</sup> X = don't care.

<sup>2</sup> High-Z = high impedance.

## RECEIVER FAIL-SAFE

The ADM307xE family guarantees a logic high receiver output when the receiver inputs are shorted, open, or connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver input threshold between –50 mV and –200 mV. If the differential receiver input voltage (A – B) is greater than or equal to –50 mV, RO is logic high. If A – B is less than or equal to –200 mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver differential input voltage is pulled to 0 V by the termination. With the receiver thresholds of the ADM307xE family, this results in a logic high with a 50 mV minimum noise margin.

## HOT-SWAP CAPABILITY

(ALL EXCEPT ADM3071E/ADM3074E/ADM3077E)

### Hot-Swap Inputs

When a circuit board is inserted into a hot (or powered) back-plane, differential disturbances to the data bus can lead to data errors. During this period, processor logic output drivers are high impedance and are unable to drive the DE and RE inputs of the RS-485 transceivers to a defined logic level. Leakage currents up to  $\pm 10 \mu\text{A}$  from the high impedance state of the processor logic drivers can cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit board capacitance can cause coupling of  $V_{CC}$  or GND to the enable inputs. Without the hot-swap capability, these factors can improperly enable the driver or receiver of the transceiver. When  $V_{CC}$  rises, an internal pull-down circuit holds DE low and RE high. After the initial power-up sequence, the pull-down circuit becomes transparent, resetting the hot-swap tolerable input.

## LINE LENGTH vs. DATA RATE

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, Figure 37 illustrates an example line repeater.

## $\pm 15 \text{ kV}$ ESD PROTECTION

Two coupling methods are used for ESD testing: contact discharge and air-gap discharge. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage but does not make direct contact with the test unit. With air-gap discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, thus the term air-gap discharge. This method is influenced by humidity, temperature, barometric pressure, distance, and rate of closure of the discharge gun. The contact discharge method, while less realistic, is more repeatable and is gaining acceptance and preference over the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time, coupled with high voltages, can cause failures in unprotected semiconductors. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device can suffer from parametric degradation that can result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

Input/output lines are particularly vulnerable to ESD damage. Simply touching or connecting an input/output cable can result in a static discharge that damages or completely destroys the interface product connected to the input/output port. It is extremely important, therefore, to have high levels of ESD protection on the input/output lines.

The ESD discharge can induce latch-up in the device under test, so it is important that ESD testing on the input/output pins be

carried out while device power is applied. This type of testing is more representative of a real-world input/output discharge, which occurs when equipment is operating normally.

The transmitter outputs and receiver inputs of the ADM307xE family are characterized for protection to a  $\pm 15 \text{ kV}$  limit using the human body model.

## HUMAN BODY MODEL

Figure 33 shows the human body model and the current waveform it generates when discharged into low impedance. This model consists of a 100 pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5 k $\Omega$  resistor.

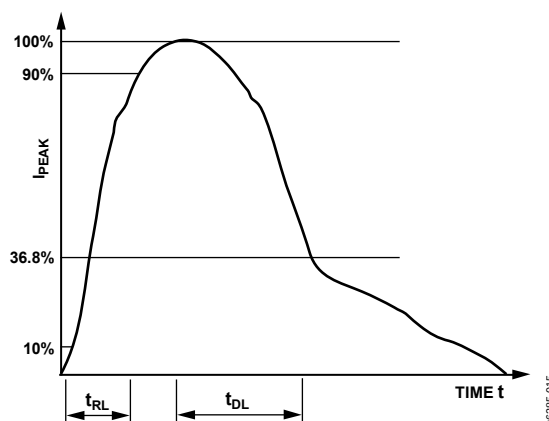
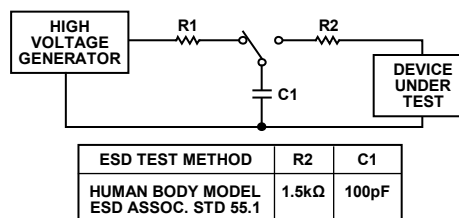


Figure 33. Human Body Model and Current Waveform

## 256 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12 k $\Omega$  (1 unit load), and the standard driver can drive up to 32 unit loads. The ADM307xE family of transceivers has a  $\frac{1}{8}$  unit load receiver input impedance (96 k $\Omega$ ), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices and other RS-485 transceivers with a total of 32 unit loads or fewer can be connected to the line.

## REDUCED EMI AND REFLECTIONS

The ADM3070E/ADM3071E/ADM3072E feature reduced slew rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing for error-free data transmission at rates up to 250 kbps. The ADM3073E/ADM3074E/ADM3075E offer higher driver output slew rate limits, allowing for transmit speeds of up to 500 kbps.

## LOW POWER SHUTDOWN MODE (ALL EXCEPT ADM3071E/ADM3074E/ADM3077E)

Low power shutdown mode is initiated by bringing both  $\overline{RE}$  high and DE low. In shutdown mode, the device draws less than 1  $\mu A$  of supply current.  $\overline{RE}$  and DE can be driven simultaneously, but the parts are guaranteed not to enter shutdown if  $\overline{RE}$  is high and DE is low for fewer than 50 ns. If the inputs are in this state for 600 ns or more, the parts are guaranteed to enter shutdown. Enable times  $t_{ZH}$  and  $t_{ZL}$  assume that the part was not originally in a low power shutdown state (see the Test Circuits and Switching Characteristics section). Enable times ( $t_{ZH(SHDN)}$  and  $t_{ZL(SHDN)}$ ) assume that the part was originally shut down. It takes drivers and receivers longer to become enabled from low power shutdown mode ( $t_{ZH(SHDN)}$ ,  $t_{ZL(SHDN)}$ ) than from driver/receiver disable mode ( $t_{ZH}$ ,  $t_{ZL}$ ).

## DRIVER OUTPUT PROTECTION

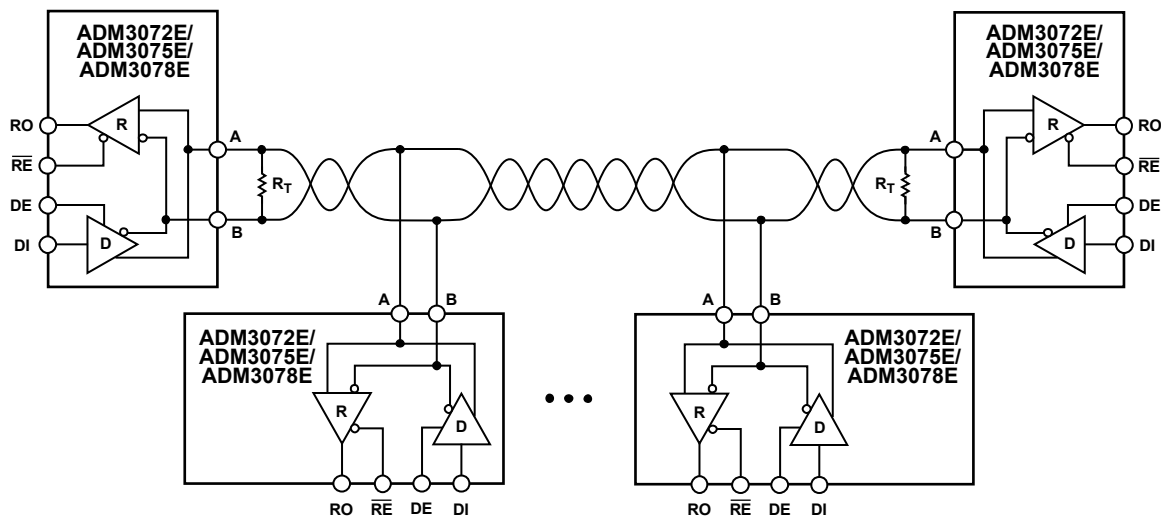
The ADM307xE family features two methods to prevent excessive output current and power dissipation caused by faults or by bus contention. Current limit protection on the

output stage provides immediate protection against short circuits over the whole common-mode voltage range (see Figure 22 and Figure 23). In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively.

## TYPICAL APPLICATIONS

The ADM3072E/ADM3075E/ADM3078E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 34 shows a typical network applications circuit. The ADM3071E/ADM3074E/ADM3077E transceivers are designed for point-to-point transmission lines (see Figure 35). The ADM3070E/ADM3073E/ADM3076E transceivers are designed for full-duplex RS-485 networks (see Figure 36).

To minimize reflections, terminate the line at both ends with a termination resistor (the value of the termination resistor should be equal to the characteristic impedance of the cable used) and keep stub lengths off the main line as short as possible.



- NOTES  
1. MAXIMUM NUMBER OF NODES: 256.  
2.  $R_T$  IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 34. ADM3072E/ADM3075E/ADM3078E Typical Half-Duplex RS-485 Network

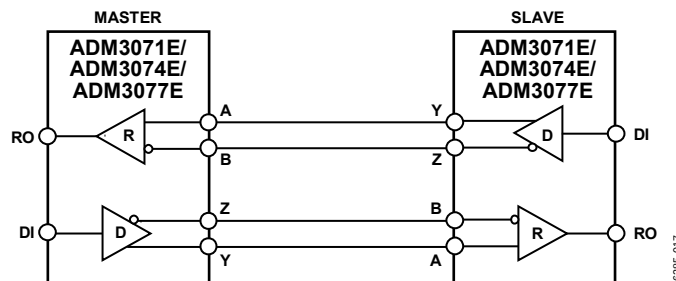
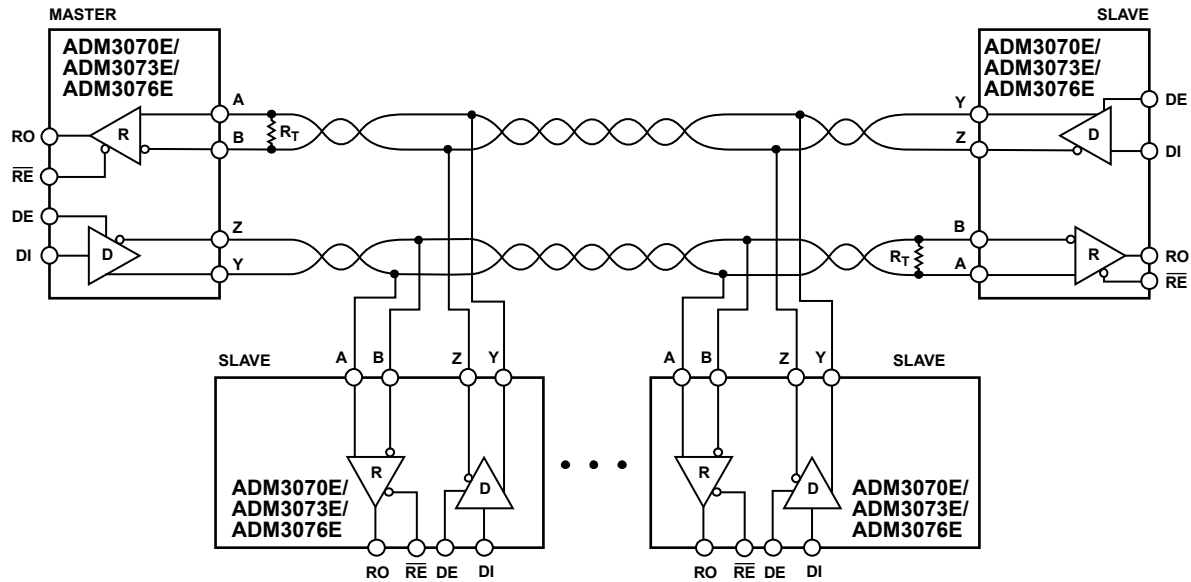


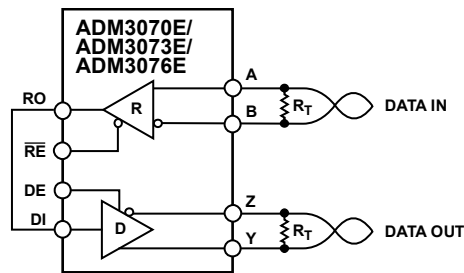
Figure 35. ADM3071E/ADM3074E/ADM3077E Full-Duplex Point-to-Point Applications



NOTES

1. MAXIMUM NUMBER OF NODES: 256.
2.  $R_T$  IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 36. ADM3070E/ADM3073E/ADM3076E Full-Duplex RS-485 Network

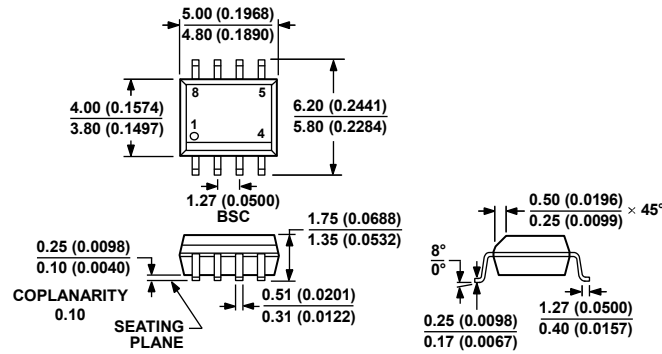


NOTES

1.  $R_T$  IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 37. Line Repeater for ADM3070E/ADM3073E/ADM3076E

## OUTLINE DIMENSIONS

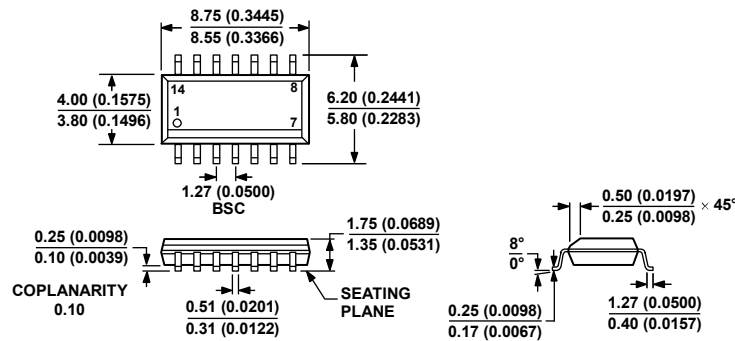


COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 38. 8-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
(R-8)

Dimensions shown in millimeters and (inches)

012407-A



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 39. 14-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
(R-14)

Dimensions shown in millimeters and (inches)

060606-A

# ADM3070E/ADM3071E/ADM3072E/ADM3073E/ADM3074E/ADM3075E/ADM3076E/ADM3077E/ADM3078E

## ORDERING GUIDE

| Model                          | Temperature Range | Package Description                             | Package Option | Ordering Quantity |
|--------------------------------|-------------------|-------------------------------------------------|----------------|-------------------|
| ADM3070EARZ <sup>1</sup>       | –40°C to +85°C    | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           | 1,000             |
| ADM3070EARZ-REEL7 <sup>1</sup> | –40°C to +85°C    | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           |                   |
| ADM3070EYRZ <sup>1</sup>       | –40°C to +125°C   | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           |                   |
| ADM3070EYRZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           |                   |
| ADM3071EARZ <sup>1</sup>       | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            | 1,000             |
| ADM3071EARZ-REEL7 <sup>1</sup> | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3071EYRZ <sup>1</sup>       | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3071EYRZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3072EARZ <sup>1</sup>       | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            | 1,000             |
| ADM3072EARZ-REEL7 <sup>1</sup> | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3072EYRZ <sup>1</sup>       | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3072EYRZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3073EARZ <sup>1</sup>       | –40°C to +85°C    | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           | 1,000             |
| ADM3073EARZ-REEL7 <sup>1</sup> | –40°C to +85°C    | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           |                   |
| ADM3073EYRZ <sup>1</sup>       | –40°C to +125°C   | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           |                   |
| ADM3073EYRZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           |                   |
| ADM3074EARZ <sup>1</sup>       | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            | 1,000             |
| ADM3074EARZ-REEL7 <sup>1</sup> | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3074EYRZ <sup>1</sup>       | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3074EYRZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3075EARZ <sup>1</sup>       | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            | 1,000             |
| ADM3075EARZ-REEL7 <sup>1</sup> | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3075EWYRZ <sup>1</sup>      | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3075EWYRZ-RL7 <sup>1</sup>  | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3075EYRZ <sup>1</sup>       | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            | 1,000             |
| ADM3075EYRZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3076EARZ <sup>1</sup>       | –40°C to +85°C    | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           | 1,000             |
| ADM3076EARZ-REEL7 <sup>1</sup> | –40°C to +85°C    | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           |                   |
| ADM3076EYRZ <sup>1</sup>       | –40°C to +125°C   | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           |                   |
| ADM3076EYRZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 14-Lead Standard Small Outline Package (SOIC_N) | R-14           |                   |
| ADM3077EARZ <sup>1</sup>       | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            | 1,000             |
| ADM3077EARZ-REEL7 <sup>1</sup> | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3077EYRZ <sup>1</sup>       | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3077EYRZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3078EARZ <sup>1</sup>       | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            | 1,000             |
| ADM3078EARZ-REEL7 <sup>1</sup> | –40°C to +85°C    | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3078EYRZ <sup>1</sup>       | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |
| ADM3078EYRZ-REEL7 <sup>1</sup> | –40°C to +125°C   | 8-Lead Standard Small Outline Package (SOIC_N)  | R-8            |                   |

<sup>1</sup> Z = RoHS Compliant Part.