# Low Cost µP Supervisory Circuits

# ADM705/ADM706/ADM707/ADM708

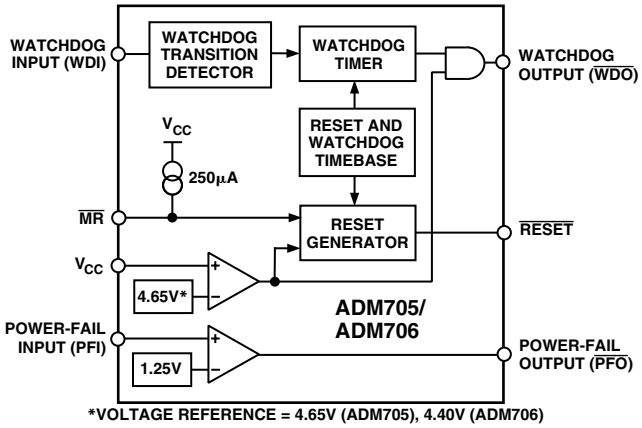
## FEATURES

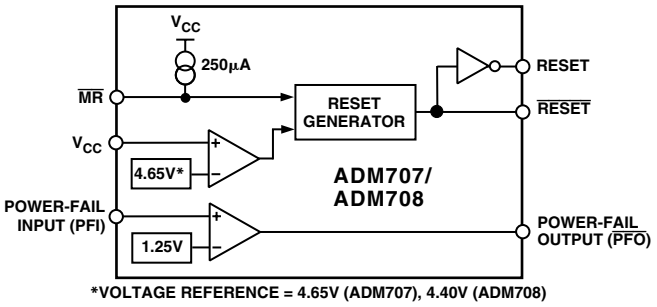
**Guaranteed $\overline{\text{RESET}}$ Valid with $V_{CC}$ = 1 V**
**190 µA Quiescent Current**
**Precision Supply-Voltage Monitor**
**4.65 V (ADM705/ADM707)**
**4.40 V (ADM706/ADM708)**
**200 ms Reset Pulsewidth**
**Debounced TTL/CMOS Manual Reset Input ($\overline{\text{MR}}$)**
**Independent Watchdog Timer—1.6 sec Timeout (ADM705/ADM706)**
**Active High Reset Output (ADM707/ADM708)**
**Voltage Monitor for Power-Fail or Low Battery Warning**
**Superior Upgrade for MAX705–MAX708**

## APPLICATIONS

**Microprocessor Systems**
**Computers**
**Controllers**
**Intelligent Instruments**
**Critical µP Monitoring**
**Automotive Systems**
**Critical µP Power Monitoring**

## FUNCTIONAL BLOCK DIAGRAMS




## GENERAL DESCRIPTION

The ADM705/ADM706/ADM707/ADM708 are low cost µP supervisory circuits. They are suitable for monitoring the 5 V power supply/battery and can also monitor microprocessor activity.

The ADM705/ADM706 provide the following functions:

1. Power-on reset output during power-up, power-down, and brownout conditions. The $\overline{\text{RESET}}$ output remains operational with $V_{CC}$ as low as 1 V.
2. Independent watchdog timeout, $\overline{\text{WDO}}$, that goes low if the watchdog input has not been toggled within 1.6 seconds.
3. A 1.25 V threshold detector for power-fail warning, low battery detection, or to monitor a power supply other than 5 V.
4. An active low debounced manual reset input ($\overline{\text{MR}}$).

The ADM707/ADM708 differ in that:

1. A watchdog timer function is not available.
2. An active high reset output in addition to the active low output is available.

Two supply-voltage monitor levels are available. The ADM705/ADM707 generate a reset when the supply voltage falls below 4.65 V, while the ADM706/ADM708 require that the supply fall below 4.40 V before a reset is issued.

All parts are available in 8-lead DIP and SOIC packages.

REV. C



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# ADM705–ADM708–SPECIFICATIONS ($V_{CC}$ = 4.75 V to 5.5 V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| $V_{CC}$ Operating Voltage Range | 1.0 | | 5.5 | V | |
| Supply Current | | 190 | 250 | µA | |
| Reset Threshold | 4.5 | 4.65 | 4.75 | V | ADM705, ADM707 |
| | 4.25 | 4.40 | 4.50 | V | ADM706, ADM708 |
| Reset Threshold Hysteresis | | 40 | | mV | |
| Reset Pulsewidth | 160 | 200 | 280 | ms | |
| $\overline{\text{RESET}}$ Output Voltage | $V_{CC}$ – 1.5 | | | V | $I_{SOURCE}$ = 800 µA |
| | | | 0.4 | V | $I_{SINK}$ = 3.2 mA |
| | | | 0.3 | V | $V_{CC}$ = 1 V, $I_{SINK}$ = 50 µA |
| | | | 0.3 | V | $V_{CC}$ = 1.2 V, $I_{SINK}$ = 100 µA |
| RESET Output Voltage | $V_{CC}$ – 1.5 | | | V | ADM707, ADM708, $I_{SOURCE}$ = 800 µA |
| | | | 0.4 | V | ADM707, ADM708, $I_{SINK}$ = 1.2 mA |
| Watchdog Timeout Period ($t_{WD}$) | 1.00 | 1.60 | 2.25 | sec | |
| WDI Pulsewidth ($t_{WP}$) | 50 | | | ns | $V_{IL}$ = 0.4 V, $V_{IH}$ = $V_{CC}$ ×0.8 |
| WDI Input Threshold | | | | | |
| Logic Low | | | 0.8 | V | |
| Logic High | 3.5 | | | V | |
| WDI Input Current | | 50 | 150 | µA | WDI = $V_{CC}$ |
| | –150 | –50 | | µA | WDI = 0 V |
| $\overline{\text{WDO}}$ Output Voltage | $V_{CC}$ – 1.5 | | | V | $I_{SOURCE}$ = 800 µA |
| | | | 0.4 | V | $I_{SINK}$ = 1.2 mA |
| $\overline{\text{MR}}$ Pull-Up Current | 100 | 250 | 600 | µA | $\overline{\text{MR}}$ = 0 V |
| $\overline{\text{MR}}$ Pulsewidth | 150 | | | ns | |
| $\overline{\text{MR}}$ Input Threshold | | | 0.8 | V | |
| | 2.0 | | | V | |
| $\overline{\text{MR}}$ to Reset Output Delay | | | 250 | ns | |
| PFI Input Threshold | 1.2 | 1.25 | 1.3 | V | |
| PFI Input Current | –25 | +0.01 | +25 | nA | |
| PFO Output Voltage | $V_{CC}$ – 1.5 | | | V | $I_{SOURCE}$ = 800 µA |
| | | | 0.4 | V | $I_{SINK}$ = 3.2 mA |

Specifications subject to change without notice.

### ABSOLUTE MAXIMUM RATINGS*

($T_A$ = 25°C, unless otherwise noted.)

$V_{CC}$ ..... –0.3 V to +6 V
All Other Inputs ..... –0.3 V to $V_{CC}$ + 0.3 V
Input Current
  $V_{CC}$ ..... 20 mA
  GND ..... 20 mA
Digital Output Current ..... 20 mA
Power Dissipation, N-8 DIP ..... 727 mW
  $\theta_{JA}$ Thermal Impedance ..... 135°C/W
Power Dissipation, SO-8 SOIC ..... 470 mW
  $\theta_{JA}$ Thermal Impedance ..... 110°C/W
Operating Temperature Range
  Industrial (A Version) ..... –40°C to +85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
  Vapor Phase (60 sec) ..... 215°C
  Infrared (15 sec) ..... 220°C
Storage Temperature Range ..... –65°C to +150°C
ESD Rating ..... >5 kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

### ORDERING GUIDE

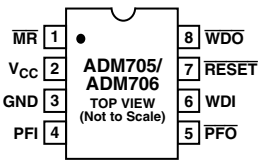
| Model | Temperature Range | Package Option |
|---|---|---|
| ADM705AN | –40°C to +85°C | N-8 |
| ADM705AR | –40°C to +85°C | SO-8 |
| ADM706AN | –40°C to +85°C | N-8 |
| ADM706AR | –40°C to +85°C | SO-8 |
| ADM707AN | –40°C to +85°C | N-8 |
| ADM707AR | –40°C to +85°C | SO-8 |
| ADM708AN | –40°C to +85°C | N-8 |
| ADM708AR | –40°C to +85°C | SO-8 |

## PIN FUNCTION DESCRIPTIONS

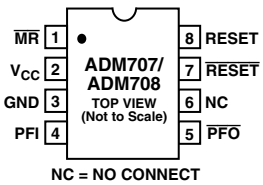
| Mnemonic | Pin Number: ADM705 ADM706 DIP, SOIC | Pin Number: ADM707 ADM708 DIP, SPOC | Function |
|---|---|---|---|
| $\overline{MR}$ | 1 | 1 | Manual Reset Input. When taken below 0.8 V, a RESET is generated. $\overline{MR}$ can be driven from TTL, CMOS logic, or from a manual reset switch as it is internally debounced. An internal 250 μA pull-up current holds the input high when floating. |
| $V_{CC}$ | 2 | 2 | 5 V Power Supply Input |
| GND | 3 | 3 | 0 V. Ground reference for all signals |
| PFI | 4 | 4 | Power-Fail Input. PFI is the noninverting input to the power-fail comparator. When PFI is less than 1.25 V, $\overline{PFO}$ goes low. If unused, PFI should be connected to GND or $V_{CC}$. |
| $\overline{PFO}$ | 5 | 5 | Power-Fail Output. $\overline{PFO}$ is the output from the power-fail comparator. It goes low when PFI is less than 1.25 V. |
| WDI | 6 | N/A | Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, the watchdog output $\overline{WDO}$ goes low. The timer resets with each transition at the WDI input.<br>Either a high-to-low or a low-to-high transition will clear the counter. The internal timer is also cleared whenever reset is asserted. The watchdog timer is disabled when WDI is left floating or connected to a three-state buffer. |
| NC | N/A | 6 | No Connect |
| $\overline{RESET}$ | 7 | 7 | Logic Output. $\overline{RESET}$ goes low for 200 ms when triggered. It can be triggered either by $V_{CC}$ being below the reset threshold or by a low signal on the manual reset ($\overline{MR}$) input. $\overline{RESET}$ will remain low whenever $V_{CC}$ is below the reset threshold (4.65 V in ADM705, 4.4 V in ADM706). It remains low for 200 ms after $V_{CC}$ goes above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$. |
| $\overline{WDO}$ | 8 | N/A | Logic Output. The Watchdog Output, $\overline{WDO}$, goes low if the internal watchdog timer times out as a result of inactivity on the WDI input. It remains low until the watchdog timer is cleared. $\overline{WDO}$ also goes low during low line conditions. Whenever $V_{CC}$ is below the reset threshold, $\overline{WDO}$ remains low. As soon as $V_{CC}$ goes above the reset threshold, $\overline{WDO}$ goes high immediately. |
| RESET | N/A | 8 | Logic Output. RESET is an active high output suitable for systems that use active high RESET logic. It is the inverse of $\overline{RESET}$. |

## PIN CONFIGURATIONS

**DIP, SOIC**




**DIP, SOIC**



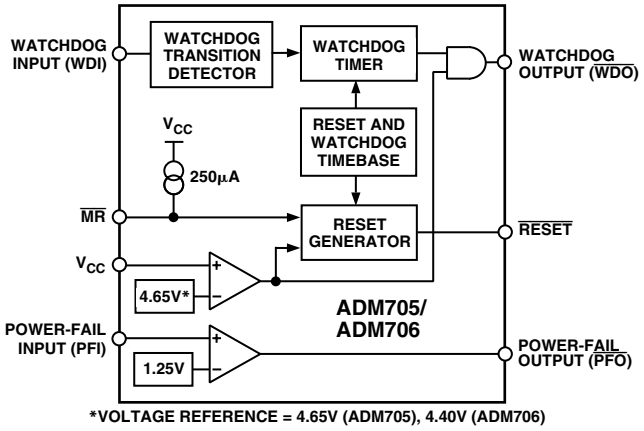



*Figure 1. ADM705/ADM706 Functional Block Diagram*

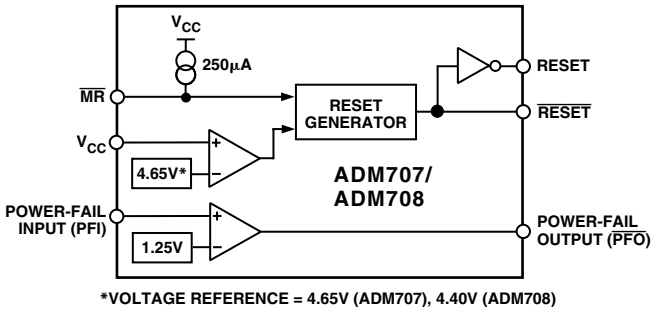



*Figure 2. ADM707/ADM708 Functional Block Diagram*

## CIRCUIT INFORMATION

### Power-Fail RESET Output

RESET is an active low output that provides a RESET signal to the microprocessor whenever the $V_{CC}$ input is below the reset threshold. An internal timer holds RESET low for 200 ms after the voltage on $V_{CC}$ rises above the threshold. This is intended as a power-on RESET signal for the microprocessor. It allows time for both the power supply and the microprocessor to stabilize after power-up. The RESET output is guaranteed to remain valid (low) with $V_{CC}$ as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply voltage ramps up.

In addition to RESET, an active high RESET output is also available on the ADM707/ADM708. This is the complement of RESET and is useful for processors requiring an active high RESET signal.

### Manual Reset (ADM707/ADM708)

The manual reset input (MR) allows other reset sources, such as a manual reset switch, to generate a processor reset. The input is effectively debounced by the timeout period (200 ms typical). The MR input is TTL/CMOS compatible, so it may also be driven by any logic reset output.

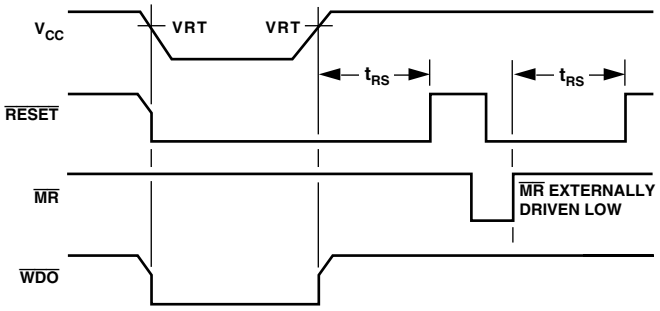



*Figure 3. RESET, MR, and WDO Timing*

### Watchdog Timer (ADM705/ADM706)

The watchdog timer circuit may be used to monitor the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the Watchdog Input (WDI) line. If this line is not toggled within the timeout period (1.6 sec), the watchdog output (WDO) goes low. The WDO output may be connected to a nonmaskable interrupt (NMI) on the processor; therefore, if the watchdog timer times out, an interrupt is generated. The interrupt service routine should then be used to rectify the problem.

If a RESET signal is required when a timeout occurs, the WDO output should be connected to the manual reset input (MR).

The watchdog timer is cleared by either a high-to-low or by a low-to-high transition on WDI. It is also cleared by RESET going low; therefore, the watchdog timeout period begins after RESET goes high.

When $V_{CC}$ falls below the reset threshold, WDO is forced low whether or not the watchdog timer has timed out. Normally, this would generate an interrupt, but it is overridden by RESET going low.

The watchdog monitor can be deactivated by floating the Watchdog Input (WDI). The WDO output can now be used as a low line output since it will only go low when $V_{CC}$ falls below the reset threshold.

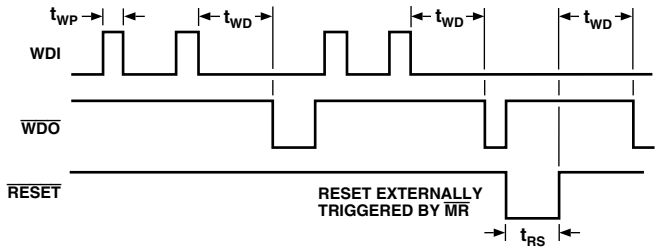



*Figure 4. Watchdog Timing*

**Power-Fail Comparator**

The power-fail comparator is an independent comparator that may be used to monitor the input power supply. The comparator's inverting input is internally connected to a 1.25 V reference voltage. The noninverting input is available at the PFI input. This input may be used to monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25 V, the comparator output ($\overline{PFO}$) goes low, indicating a power failure. For early warning of power failure, the comparator may be used to monitor the preregulator input simply by choosing an appropriate resistive divider network. The $\overline{PFO}$ output can be used to interrupt the processor so that a shutdown procedure is implemented before the power is lost.

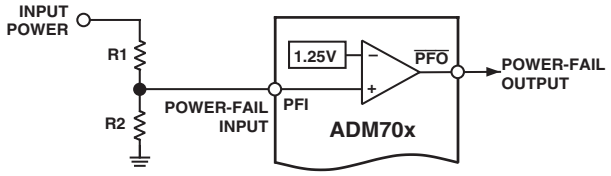



*Figure 5. Power-Fail Comparator*

**Adding Hysteresis to the Power-Fail Comparator**

For increased noise immunity, hysteresis may be added to the power-fail comparator. Since the comparator circuit is noninverting, hysteresis can be added simply by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 6. When $\overline{PFO}$ is low, Resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, Resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity may be achieved by connecting a capacitor between PFI and GND.

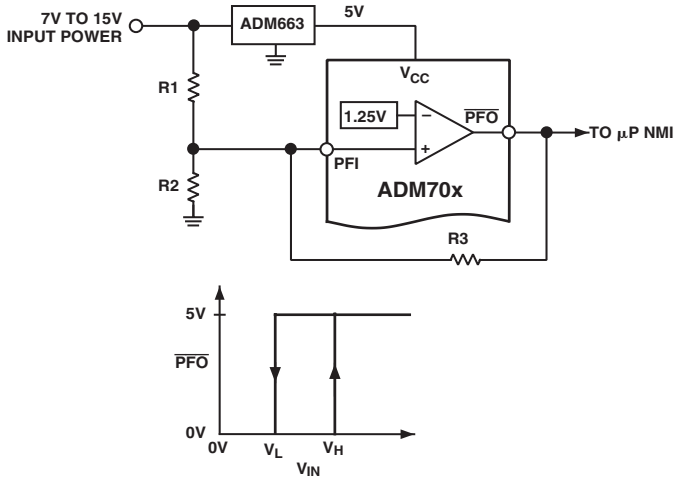



*Figure 6. Adding Hysteresis to the Power-Fail Comparator*

$$V_H = 1.25\left[1 + \left(\frac{R2 + R3}{R2 \times R3}\right)R1\right]$$

$$V_L = 1.25 + R1\left(\frac{1.25}{R2} - \frac{V_{CC} - 1.25}{RE}\right)$$

$$V_{MID} = 1.25\left(\frac{R1 + R2}{R2}\right)$$

**Valid $\overline{RESET}$ Below 1 V $V_{CC}$**

The ADM70x family of products is guaranteed to provide a valid reset level with $V_{CC}$ as low as 1 V; please refer to the Typical Performance Characteristics. As $V_{CC}$ drops below 1 V, the internal transistor will not have sufficient drive to hold it ON so the voltage on $\overline{RESET}$ will no longer be held at 0 V. A pull-down resistor as shown in Figure 7 may be connected externally to hold the line low if it is required.

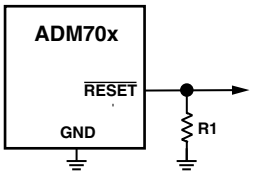
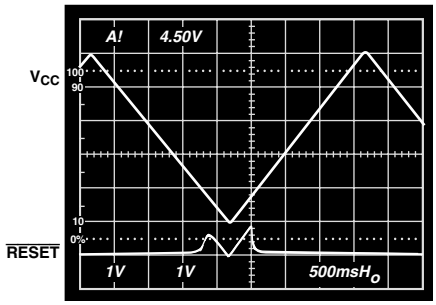
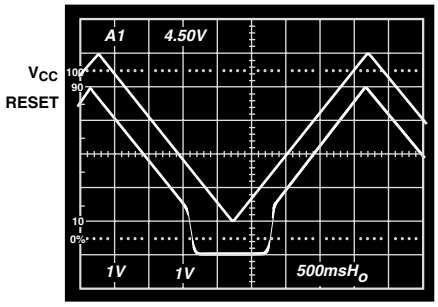



*Figure 7. $\overline{RESET}$ Valid Below 1 V*

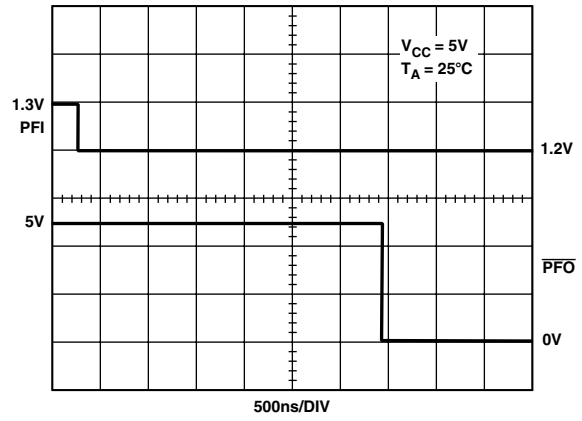
# ADM705–ADM708–Typical Performance Characteristics



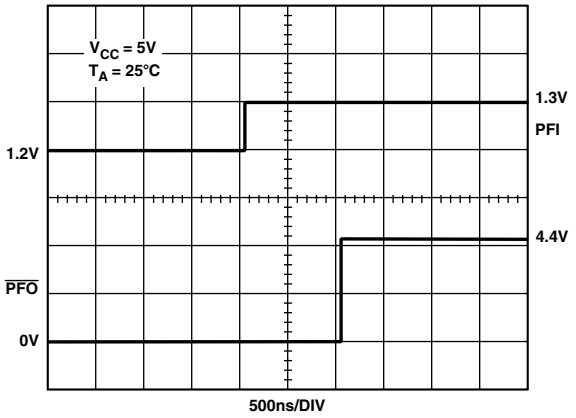

*TPC 1. $\overline{RESET}$ Output Voltage vs. Supply Voltage*



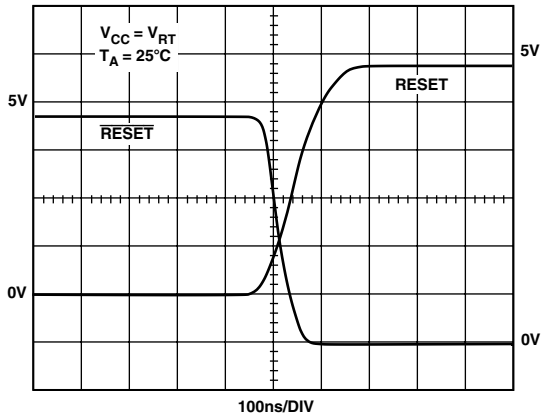

*TPC 2. ADM707/ADM708 RESET Output Voltage vs. Supply Voltage*



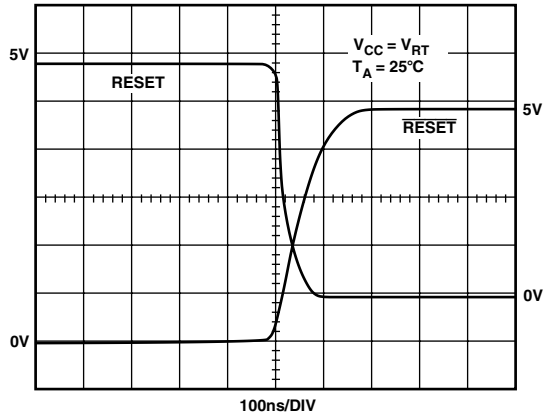

*TPC 3. PFI Comparator Assertion Response Time*



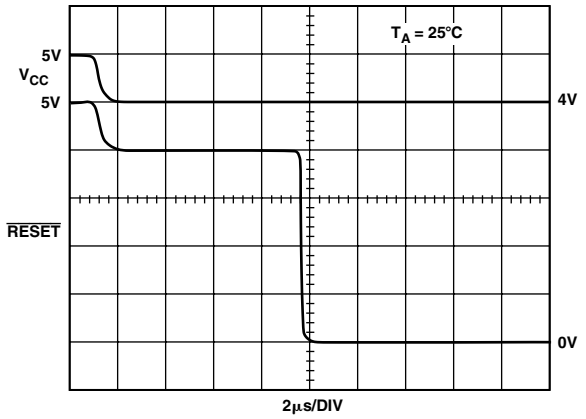

*TPC 4. PFI Comparator Deassertion Response Time*




*TPC 5. $\overline{RESET}$, RESET Assertion*




*TPC 6. $\overline{RESET}$, RESET Deassertion*




*TPC 7. ADM705/ADM707 $\overline{RESET}$ Response Time*

## APPLICATIONS

A typical operating circuit is shown in Figure 8. The unregulated dc input supply is monitored using the PFI input via the resistive divider network. Resistors R1 and R2 should be selected so that when the supply voltage drops below the desired level (e.g., 8 V), the voltage on PFI drops below the 1.25 V threshold thereby generating an interrupt to the µP. Monitoring the preregulator input gives additional time to execute an orderly shutdown procedure before power is lost.

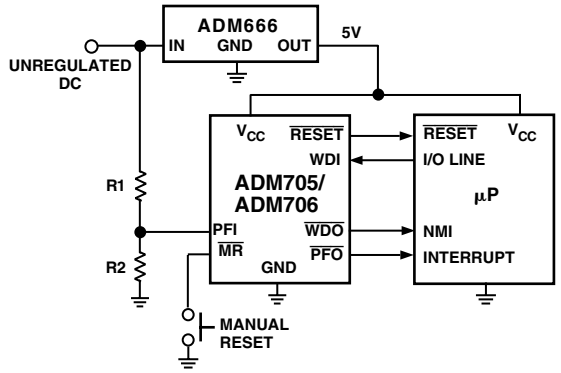



*Figure 8. Typical Application Circuit*

Microprocessor activity is monitored using the WDI input. This is driven using an output line from the processor. The software routines should toggle this line at least once every 1.6 seconds. If a problem occurs and this line is not toggled, $\overline{WDO}$ goes low and a nonmaskable interrupt is generated. This interrupt routine may be used to clear the problem.

If, in the event of inactivity on the WDI line, a system reset is required, the $\overline{WDO}$ output should be connected to the $\overline{MR}$ input as shown in Figure 9.

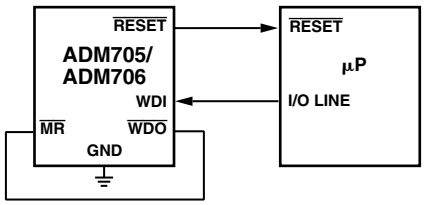



*Figure 9. $\overline{RESET}$ from $\overline{WDO}$*

**Monitoring Additional Supply Levels**

It is possible to use the power-fail comparator to monitor a second supply as shown in Figure 10. The two sensing resistors, R1 and R2, are selected so that the voltage on PFI drops below 1.25 V at the minimum acceptable input supply. The $\overline{PFO}$ output may be connected to the $\overline{MR}$ input so that a RESET is generated when the supply drops out of tolerance. In this case, if either supply drops out of tolerance, a $\overline{RESET}$ will be generated.

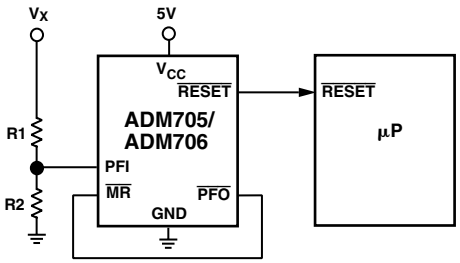



*Figure 10. Monitoring 5 V and an Additional Supply, $V_X$*

**µPs with Bidirectional $\overline{RESET}$**

In order to prevent contention for microprocessors with a bidirectional reset line, a Current Limiting Resistor should be inserted between the ADM70x $\overline{RESET}$ output pin and the µP reset pin. This will limit the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7 kΩ. If the reset output is required for other uses, it should be buffered as shown in Figure 11.

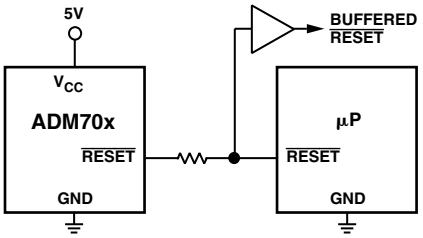
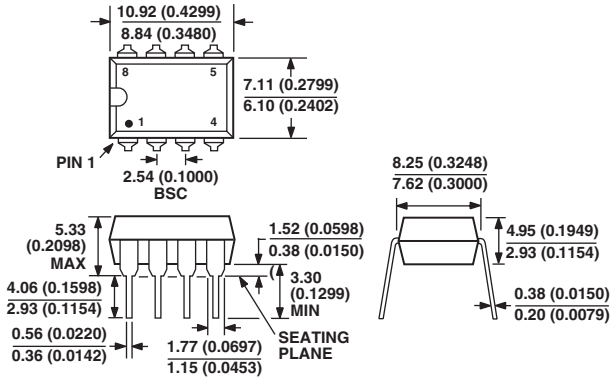



*Figure 11. Bidirectional I-O $\overline{RESET}$*

## OUTLINE DIMENSIONS

### 8-Lead Plastic Dual-in-Line Package [PDIP]
### (N-8)

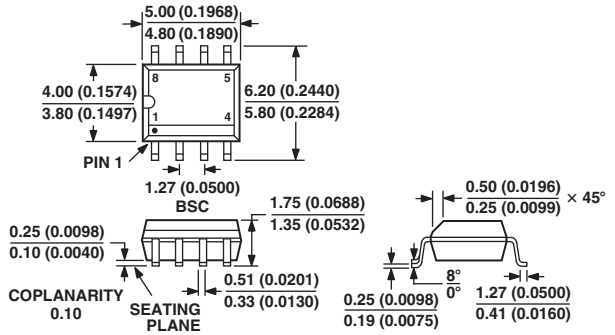
Dimensions shown in millimeters and (inches)




CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

### 8-Lead Small Outline Package [SOIC]
### (R-8)

Dimensions shown in millimeters and (inches)




CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

COMPLIANT TO JEDEC STANDARDS MS-012AA

C00088–0–8/02 (C)

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# Revision History

| Location | Page |
|---|---|
| **8/02—Data Sheet changed from REV. B to REV. C.** | |
| Removed RM-8 (μSOIC) Package | Universal |
| Updated N-8 and R-8 Packages | 8 |