

FEATURES

High Accuracy Over Line and Load:
 $\pm 0.8\%$ @ $+25^\circ\text{C}$, $\pm 1.4\%$ Over Temperature
Ultralow Dropout Voltage: 150 mV Typical @ 200 mA
Requires Only $C_O = 1 \mu\text{F}$ for Stability
anyCAP = Stable with All Types of Capacitors
 (Including MLCC)
Current and Thermal Limiting
Low Noise
Dropout Detector
Low Shutdown Current: $1 \mu\text{A}$
3.2 V to 12 V Supply Range
Adjustable 2.2 V to 10 V Output Range
 -20°C to $+85^\circ\text{C}$ Ambient Temperature Range
Thermally Enhanced TSSOP-14 Package

APPLICATIONS

Cellular Telephones
 Notebook, Palmtop Computers
 Battery Powered Systems
 Portable Instruments
 Post Regulator for Switching Supplies
 Bar Code Scanners

FUNCTIONAL BLOCK DIAGRAM

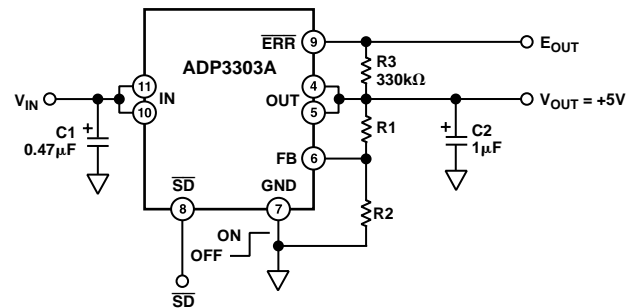
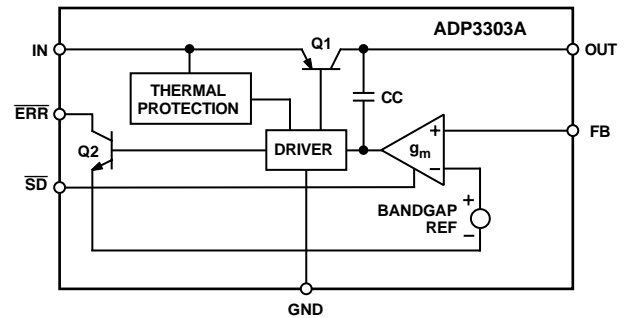


Figure 1. Typical Application Circuit

GENERAL DESCRIPTION

The ADP3303A is a member of the ADP330x family of precision low dropout anyCAP voltage regulators. The ADP3303A stands out from conventional LDOs with a novel architecture, an enhanced process and a new package. Its patented design requires only a $1 \mu\text{F}$ output capacitor for stability. This device is insensitive to output capacitor ESR (Equivalent Series Resistance), and is stable with any good quality capacitor, including ceramic types (MLCC) for space restricted applications. The ADP3303A achieves exceptional accuracy of $\pm 0.8\%$ at room temperature and $\pm 1.4\%$ overall accuracy over temperature, line and load variations. The dropout voltage of the ADP3303A is only 150 mV (typical) at 200 mA.

In addition to the new architecture and process, ADI's new proprietary thermally enhanced package (Thermal Coastline) can handle 1 W of power dissipation without an external heat sink or large copper surface on the PC board. This keeps PC board real estate to a minimum and makes the ADP3303A very attractive for use in portable equipment.

The ADP3303A operates over an input voltage range of 3.2 V to 12 V and delivers a load current in excess of 200 mA. The output voltage can be adjusted from 2.2 V to 10 V using an external resistor divider. It also features an error flag that signals when the device is about to lose regulation or when the short circuit or thermal overload protection is activated. Other features include shutdown and optional noise reduction capabilities.

anyCAP is a trademark of Analog Devices Inc.

REV. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

ADP3303A—SPECIFICATIONS (@ $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = 7\text{ V}$, $C_{IN} = 0.47\ \mu\text{F}$, $C_{OUT} = 1\ \mu\text{F}$, unless otherwise noted)¹

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | |
|---|------------------------------------|--|------|-------|------|-------------------|-------------------|
| OUTPUT VOLTAGE ^{2, 3, 4} ACCURACY | V_{OUT} | $V_{IN} = \text{Nom } V_{OUT} + 0.5\text{ V to } +12\text{ V}$ $I_L = 1.0\text{ mA to } 200\text{ mA}$ $T_A = +25^\circ\text{C}$ | -0.8 | | +0.8 | % | |
| | | $V_{IN} = \text{Nom } V_{OUT} + 0.5\text{ V to } +12\text{ V}$ $I_L = 1.0\text{ mA to } 200\text{ mA}$ | -1.4 | | +1.4 | % | |
| LINE REGULATION | $\frac{\Delta V_O}{\Delta V_{IN}}$ | $V_{IN} = \text{Nom } V_{OUT} + 0.5\text{ V to } +12\text{ V}$ $T_A = +25^\circ\text{C}$ | | 0.01 | | mV/V | |
| LOAD REGULATION | $\frac{\Delta V_O}{\Delta I_L}$ | $I_L = 1.0\text{ mA to } 200\text{ mA}$ $T_A = +25^\circ\text{C}$ | | 0.005 | | mV/mA | |
| GROUND CURRENT ⁵ | I_{GND} | $I_L = 200\text{ mA}$ | | 2.0 | 4 | mA | |
| | | $I_L = 1.0\text{ mA}$ | | 0.35 | 0.6 | mA | |
| GROUND CURRENT ⁵ IN DROPOUT | I_{GND} | $V_{IN} = 2.5\text{ V}$, $V_{OUT} = 5.0\text{ V}$ $I_L = 1.0\text{ mA}$ | | 1.9 | 3.0 | mA | |
| DROPOUT VOLTAGE | V_{DROP} | $V_{OUT} \leq 98\%$ of V_O Nominal $I_L = 200\text{ mA}$ $I_L = 10\text{ mA}$ $I_L = 1\text{ mA}$ | | 0.15 | 0.4 | V | |
| | | | | | 0.02 | 0.07 | V |
| | | | | 0.003 | 0.03 | V | |
| | | | | | | | |
| SHUTDOWN THRESHOLD | V_{THSD} | ON | 2.0 | 0.9 | | V | |
| | | OFF | | 0.9 | 0.3 | V | |
| SHUTDOWN PIN INPUT CURRENT | I_{SDIN} | $0\text{ V} < V_{SD} \leq 5\text{ V}$ | | | 1 | μA | |
| | | $5\text{ V} \leq V_{SD} \leq 12\text{ V}$ @ $V_{IN} = 12\text{ V}$ | | | 22 | μA | |
| GROUND CURRENT IN ⁵ SHUTDOWN MODE | I_Q | $V_{SD} = 0$, $V_{IN} = 12\text{ V}$ $T_A = +25^\circ\text{C}$ | | | 1 | μA | |
| | | $V_{SD} = 0\text{ V}$, $V_{IN} = 12\text{ V}$ $T_A = +85^\circ\text{C}$ | | | 5 | μA | |
| OUTPUT CURRENT IN SHUTDOWN MODE | I_{OSD} | $T_A = +25^\circ\text{C}$ @ $V_{IN} = 12\text{ V}$ | | | 2.5 | μA | |
| | | $T_A = +85^\circ\text{C}$ @ $V_{IN} = 12\text{ V}$ | | | 4 | μA | |
| ERROR PIN OUTPUT LEAKAGE | I_{EL} | $V_{EO} = 5\text{ V}$ | | | 13 | μA | |
| ERROR PIN OUTPUT “LOW” VOLTAGE | V_{EOL} | $I_{SINK} = 400\ \mu\text{A}$ | | 0.15 | 0.3 | V | |
| PEAK LOAD CURRENT | I_{LDPK} | $V_{IN} = \text{Nom } V_{OUT} + 1\text{ V}$ | | 300 | | mA | |
| OUTPUT NOISE @ 5 V OUTPUT | V_{NOISE} | $f = 10\text{ Hz} - 100\text{ kHz}$ $C_{NR} = 0$ $C_{NR} = 10\text{ nF}$, $C_L = 10\ \mu\text{F}$ | | 100 | | $\mu\text{V rms}$ | |
| | | | | | 30 | | $\mu\text{V rms}$ |

NOTES

¹Ambient temperature of $+85^\circ\text{C}$ corresponds to a typical junction temperature of $+125^\circ\text{C}$ under typical full load test conditions. The formula for Nom V_{OUT} is found in the Output Voltage Selection section.

²Accuracy guaranteed using external trim pots.

³For 2.7 V output, the minimum V_{IN} is 3.2 V.

⁴Guaranteed by design and characterization.

⁵Ground currents include the current through R1, R2.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

| | |
|---|--------------------|
| Input Supply Voltage | −0.3 V to +16 V |
| Shutdown Input Voltage | −0.3 V to +16 V |
| Error Flag Output Voltage | −0.3 V to +16 V |
| Noise Bypass Pin Voltage | −0.3 V to +5 V |
| Power Dissipation | Internally Limited |
| Operating Ambient Temperature Range | −55°C to +125°C |
| Operation Junction Temperature Range | −55°C to +125°C |
| θ_{JA} | 96°C/W |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature Range (Soldering 10 sec) | +300°C |
| Vapor Phase (60 sec) | +215°C |
| Infrared (15 sec) | +220°C |

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

Other Members of anyCAP Family¹

| Model | Output Current | Package Options ² | Comments |
|---------|----------------|------------------------------|---------------|
| ADP3300 | 50 mA | SOT-23-6 | High Accuracy |
| ADP3301 | 100 mA | SO-8 | High Accuracy |
| ADP3302 | 100 mA | SO-8 | Dual Output |
| ADP3307 | 100 mA | SOT-23-6 | High Accuracy |
| ADP3308 | 50 mA | SOT-23-5 | High Accuracy |
| ADP3309 | 100 mA | SOT-23-5 | High Accuracy |

NOTES

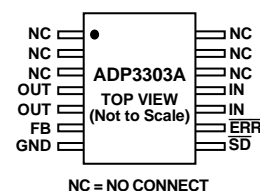
¹See individual data sheets for detailed ordering information.

²SO = Small Outline, SOT = Surface Mount Outline.

PIN FUNCTION DESCRIPTIONS

| Pin | Mnemonic | Function |
|---------|------------------|---|
| 1–3 | NC | No Connect. |
| 4 & 5 | OUT | Output of the Regulator. Bypass to ground with a 1 μ F or larger capacitor. Pins 4 and 5 must be connected together for proper operation. |
| 6 | FB | Feedback. Connect to an external resistor divider that sets the output voltage. |
| 7 | GND | Ground. |
| 8 | \overline{SD} | Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, this pin should be connected to the input pin. |
| 9 | \overline{ERR} | Open Collector Output that goes low to indicate that the output is about to go out of regulation. |
| 10 & 11 | IN | Regulator Input. Pins 10 and 11 must be connected together for proper operation. |
| 12–14 | NC | No Connect. |

PIN CONFIGURATION



ORDERING GUIDE

| Model | Voltage Output | Package Description | Package Option |
|------------------|----------------|---|----------------|
| ADP3303AARU-Reel | ADJ | Thin Shrink Small Outline Package (TSSOP) | TSSOP-14 |

NOTES

All devices operate over the ambient temperature range of −20°C to +85°C.

Contact the factory for the availability of other output voltage options.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3303A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADP3303A—Typical Performance Characteristics

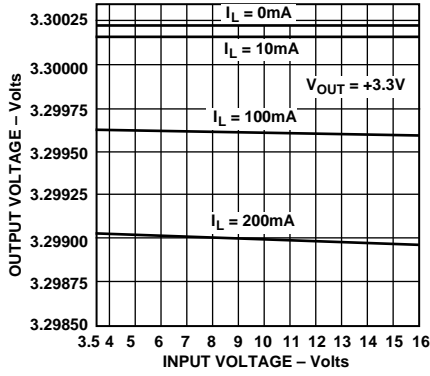


Figure 2. Line Regulation: Output Voltage vs. Supply Voltage

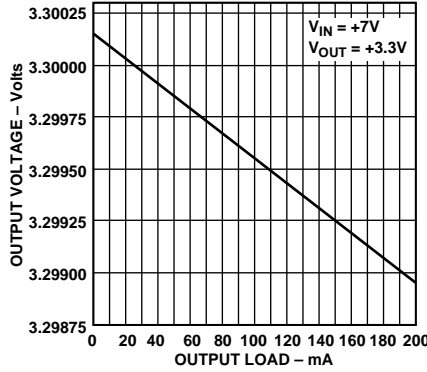


Figure 3. Output Voltage vs. Load Current

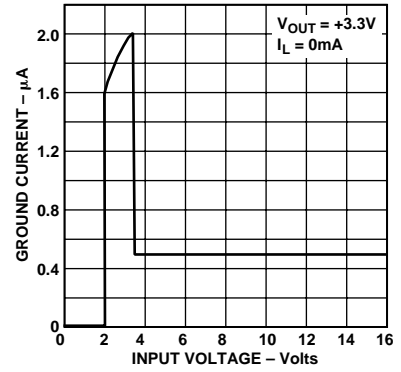


Figure 4. Quiescent Current vs. Supply Voltage

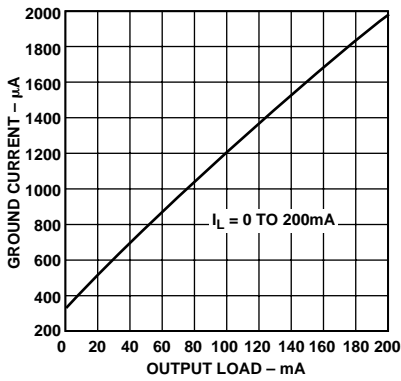


Figure 5. Quiescent Current vs. Load Current

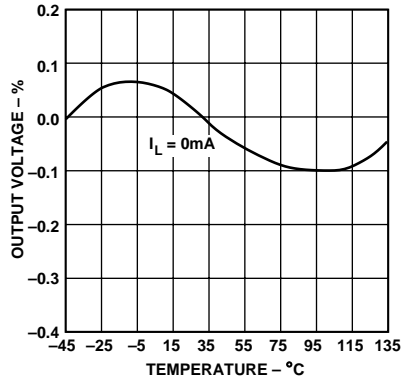


Figure 6. Output Voltage Variation % vs. Temperature

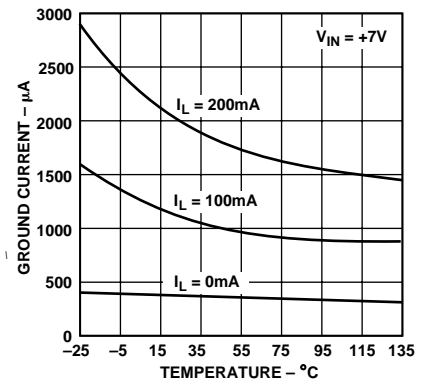


Figure 7. Quiescent Current vs. Temperature

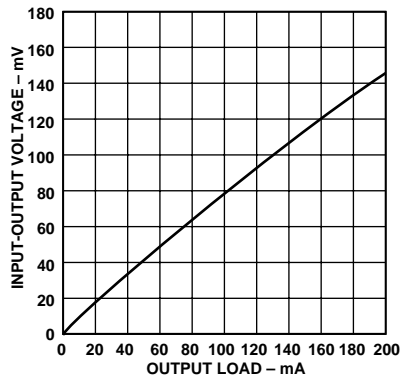


Figure 8. Dropout Voltage vs. Output Current

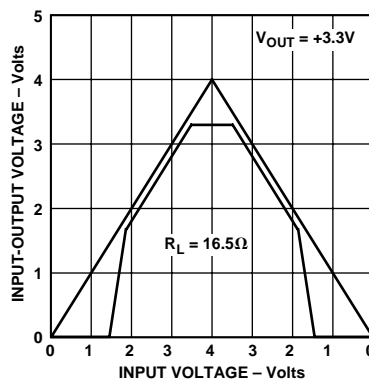


Figure 9. Power-Up/Power-Down

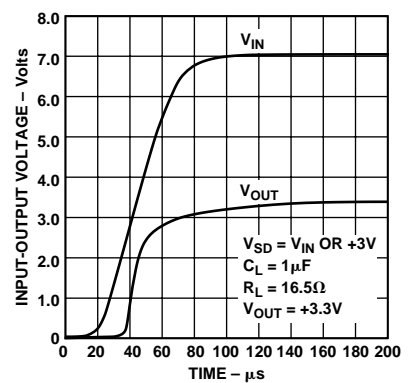


Figure 10. Power-Up Transient

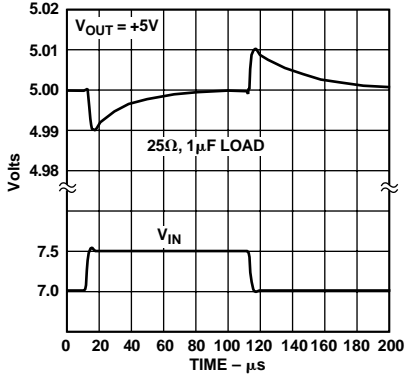


Figure 11. Line Transient Response

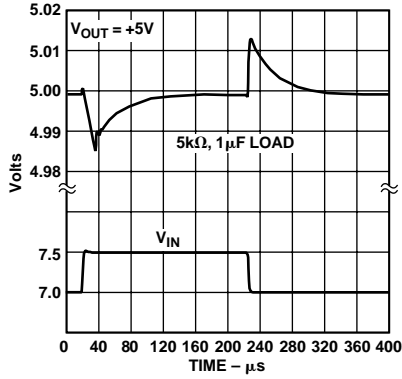


Figure 12. Line Transient Response

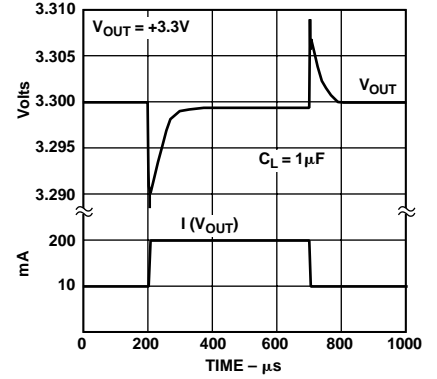


Figure 13. Load Transient for 10 mA to 200 mA Pulse

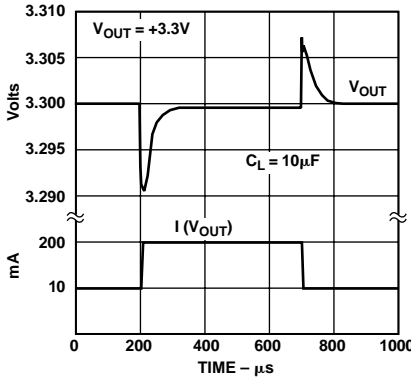


Figure 14. Load Transient for 10 mA to 200 mA Pulse

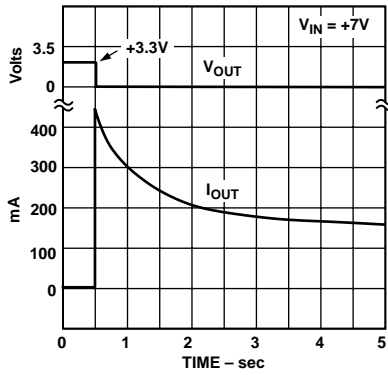


Figure 15. Short Circuit Current

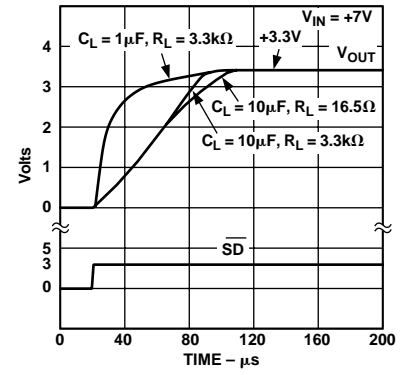


Figure 16. Turn On

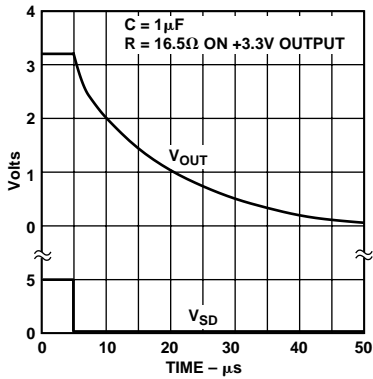


Figure 17. Turn Off

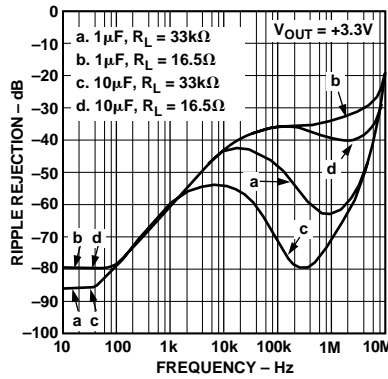


Figure 18. Power Supply Ripple Rejection

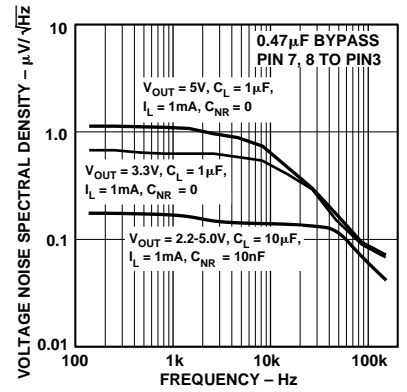


Figure 19. Output Noise Density

ADP3303A

THEORY OF OPERATION

The new anyCAP LDO ADP3303A uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2, which is varied to provide the available output voltage options. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

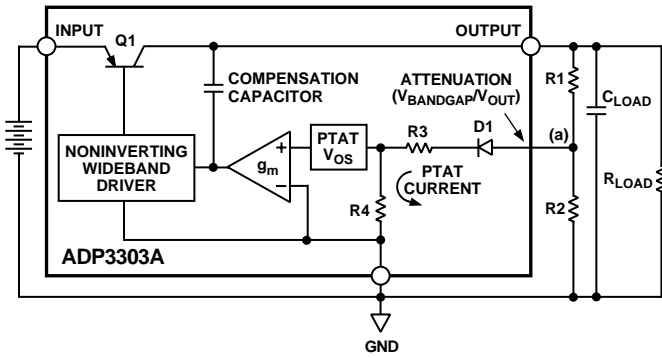


Figure 20. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that at equilibrium it produces a large, temperature proportional input “offset voltage” that is repeatable and very well controlled. The temperature-proportional offset voltage is combined with the complementary diode voltage to form a “virtual bandgap” voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the bandgap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the diode D1, and a second divider consisting of R3 and R4, the values are chosen to produce a temperature stable output. This unique arrangement specifically corrects for the loading of the divider so that the error resulting from base current loading in conventional circuits is avoided.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole splitting arrangement to achieve reduced sensitivity to the value, type and ESR of the load capacitance.

Most LDOs place strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value, required to keep conventional LDOs stable, changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

This is no longer true with the ADP3303A anyCAP LDO. It can be used with virtually any capacitor, with no constraint on the minimum ESR. The innovative design allows the circuit to be stable with just a small 1 μF capacitor on the output. Additional advantages of the pole splitting scheme include superior line

noise rejection and very high regulator gain, which leads to excellent line and load regulation. An impressive $\pm 1.4\%$ accuracy is guaranteed over line, load and temperature.

Additional features of the circuit include current limit, thermal shutdown and noise reduction. Compared to standard solutions that give warning after the output has lost regulation, the ADP3303A provides improved system performance by enabling the $\overline{\text{ERR}}$ Pin to give warning before the device loses regulation.

As the chip’s temperature rises above 165°C , the circuit activates a soft thermal shutdown, indicated by a signal low on the $\overline{\text{ERR}}$ Pin, to reduce the current to a safe level.

APPLICATION INFORMATION

The ADP3303A is very easy to use. The only external component required for stability is a small 1 μF bypass capacitor on the output. If the shutdown feature is not used, the shutdown pin (Pin 8) should be tied to the input pin.

CAPACITOR SELECTION

Bypass Capacitor (C1): connecting a 0.47 μF capacitor from the IN pins (Pins 10 and 11) to ground greatly improves its line transient response and reduces the circuit’s sensitivity to PC board layout. A larger capacitor could be used if line transients of longer duration are expected.

Output Capacitor (C2): as will all members of the anyCAP low dropout regulator family, the ADP3303A is stable with any type of output capacitor down to zero ESR. A small 1 μF output capacitor is required for stability. Larger capacitors with low ESR are recommended for improved load transient response.

For space limited applications, Multilayer Ceramic Capacitors (MLCC) are a good choice. For low temperature operations OS-CON capacitors offer better performance.

Noise Reduction Capacitor (CNR): to reduce the ADP3303A’s low output noise by 6 dB–10 dB, a noise gain limiting capacitor can be connected between the feedback (FB) pin (Pin 6) and the OUT pins as shown in Figure 21. Low leakage capacitors in the 100 pF–500 pF range provide the best performance. Larger capacitors will slow down the output transient response. CNR is not needed in low noise applications where fast load transients are not expected.

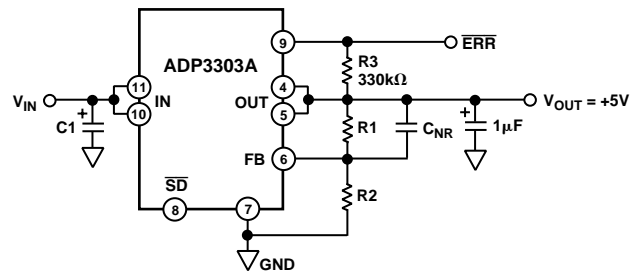


Figure 21. Noise Reduction Circuit

OUTPUT VOLTAGE SELECTION

The ADP3303A is characterized by having the output voltage divider placed externally. The output voltage will be divided by R1 and R2 and fed back to the FB pin.

In order to have the lowest possible sensitivity of output voltage versus any temperature variation, it is important that the parallel resistance of R1 and R2 is always 44 k Ω .

The proper formula to compute R1 and R2 is:

$$R1 = \frac{44 \text{ k}\Omega \times V_{SEL}}{1.189}, R2 = \left(\frac{44 \text{ k}\Omega}{1 - \frac{1.189}{V_{SEL}}} \right)$$

Where V_{SEL} is the desired output voltage.

The output voltage can be selected from 2.2 V to 10 V. R1 is connected from the OUT pin to the FB pin and R2 is connected from the FB pin to GND. As an example, the Feedback Resistor Selection Table shows the feedback resistor values for 3 V and 5 V output voltages.

Table I. Feedback Resistor Selection Table

| V_{OUT} | R1 (1% Resistor) | R2 (1% Resistor) |
|-----------|---------------------|---------------------|
| 3 V | 110 k Ω | 73.2 k Ω |
| 5 V | 187 k Ω | 57.6 k Ω |

OUTPUT CURRENT LIMITING

Short circuit protection is provided by limiting the pass transistors base drive current. Maximum output current is limited to 200 mA.

THERMAL OVERLOAD PROTECTION

The ADP3303A is protected against damage due to excessive power dissipation by its thermal overload protection circuit, which limits the die temperature to a maximum of 165°C. Under extreme conditions (i.e., high ambient temperature and power dissipation), where die temperature starts to rise above 165°C, the output current is reduced until the die temperature has dropped to a safe level. The output current is restored when the die temperature is reduced.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed 125°C.

CALCULATING JUNCTION TEMPERATURE

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT}) I_{LOAD} + (V_{IN}) I_{GND}$$

Where I_{LOAD} and I_{GND} are load current and ground current, V_{IN} and V_{OUT} are input and output voltages, respectively.

Assuming $I_{LOAD} = 200 \text{ mA}$, $I_{GND} = 4 \text{ mA}$, $V_{IN} = 5.5 \text{ V}$ and $V_{OUT} = 3.0 \text{ V}$, device power dissipation is:

$$P_D = (5.5 \text{ V} - 3.0 \text{ V}) 0.2 + 5.5 \times 0.004 = 0.522 \text{ W}$$

The proprietary thermal coastline TSSOP-14 package of the ADP3303A, in conjunction with the recommended PCB layout shown in Figure 21, yields a thermal resistance of 96°C/W. As a result, the die temperature rise for the example circuit is:

$$\Delta T = T_J - T_A = P_D \times \theta_{JA} = 0.522 \times 96 = 50.1^\circ\text{C}$$

If the maximum ambient temperature is 50°C, this yields a maximum junction temperature of $T_{JMAX} = 100.1^\circ\text{C}$, which is below the 125°C maximum operating junction temperature rating.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATION

The rate at which heat is transferred is directly proportional to the temperature differential between the die and PC board. Once heat is transferred to the PC board, it should be dissipated to the air or other medium.

Surface mount components rely on the conductive traces or pads to transfer heat away from the device. Appropriate PC board layout technique should be used to remove heat from immediate vicinity of the package.

The following general guidelines will be helpful when designing a board layout:

1. PC board traces with larger cross section areas will remove more heat. For optimum results, use PC's with thicker copper and or wider traces.
2. Increase the surface area exposed to open air so heat can be removed by convection or forced air flow.
3. Do not solder mask or silk screen the heat dissipating traces. Black anodizing will significantly improve heat reduction by means of increased radiation.

Figure 22 shows the recommended board layout for the ADP3303A. Although it is not critical, make sure R1 is connected right at the pin or the point you want to regulate in order to realize a proper kelvin connection. This will improve overall precision and stability. The same consideration is valid for the R2 connection to the ground pin, but a short connection is strongly suggested. No other components can be connected to the FB pin except an optional 10 nF–100 nF capacitor (C_{NR}) in parallel to R1 that serves as a noise reduction capacitor.

SHUTDOWN MODE

Applying a TTL high signal to the shutdown pin, or tying it to the input pin, will turn the output ON. Pulling the shutdown pin down to 0.3 V or below, or tying it to ground, will turn the output OFF. In shutdown mode, quiescent current is reduced to less than 1 μA .

INPUT-OUTPUT DROPOUT VOLTAGE AND DROPOUT DETECTOR

The ADP3303A maintains a regulated output with an input voltage as low as 150 mV above the nominal output voltage. Input voltage falling below this level will generate an error signal indicating that the error amplifier output is reaching its saturated state and will not be able to drive the pass transistor any harder. Lowering the input voltage any further will result in output voltage reduction and loss of regulation.

The input voltage threshold which generates the error output signal depends on the load current. At the rated output current, it is slightly lower than the nominal output voltage plus the dropout voltage. However, the threshold is much lower at lighter loads.

APPLICATION CIRCUITS

Crossover Switch

The circuit in Figure 23 shows that two ADP3303As can be used to form a mixed supply voltage system. The output switches between two different levels selected by an external digital input. Output voltages can be any combination of voltages from the Ordering Guide.

ADP3303A

Higher Output Current

The ADP3303A can source up to 200 mA without any heatsink or pass transistor. If higher current is needed, an appropriate pass transistor can be used, as in Figure 24, to increase the output current to 1 A.

Constant Dropout Post Regulator

The circuit in Figure 25 provides high precision with low dropout for any regulated output voltage. It significantly reduces the ripple from a switching regulator while providing a constant dropout voltage, which limits the power dissipation of the LDO to 60 mW. The ADP3000 used in this circuit is a switching regulator in the step-up configuration.

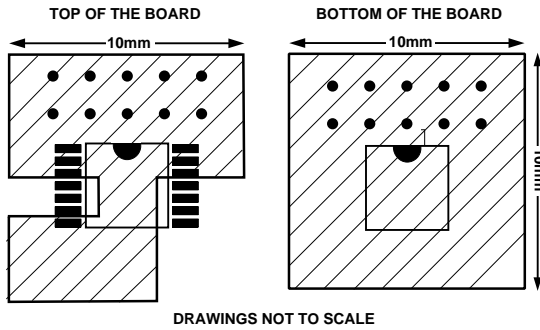


Figure 22. ADP3303A (TSSOP-14) Recommended Board Layout

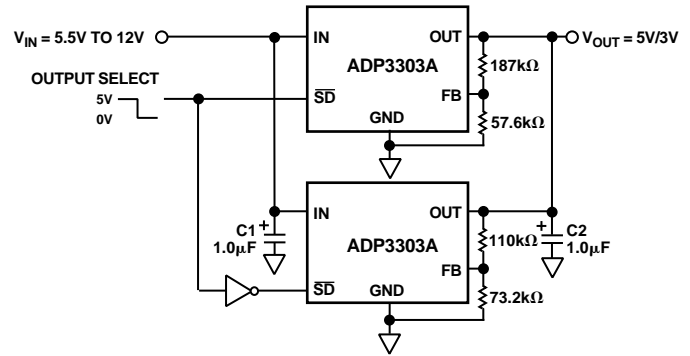


Figure 23. Crossover Switch

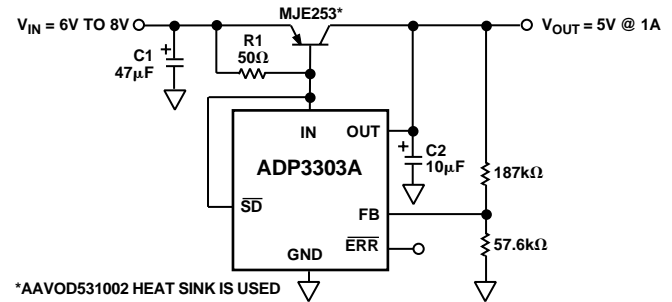


Figure 24. High Output Current Linear Regulator

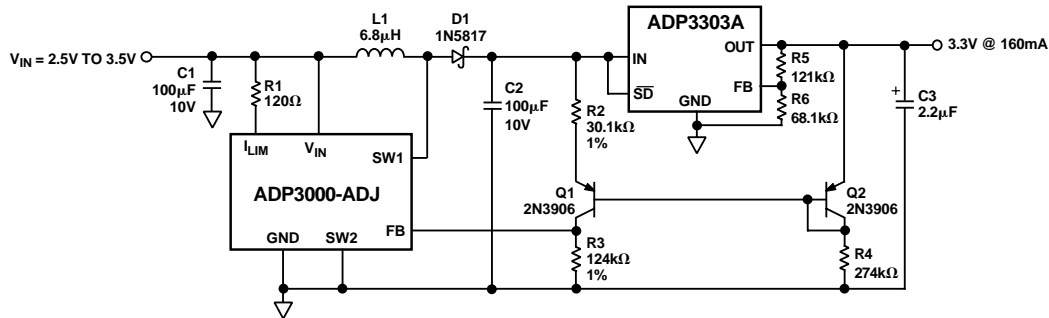


Figure 25. Constant Dropout Post Regulator

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Thin Shrink Small Outline Package (TSSOP) (RU-14)

